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FABRICATION AND CHARACTERIZATION OF MEMRISTIVE DEVICES FOR BIOINSPIRED APPLICATIONS

EVRIPIDES KYRIAKIDES

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Evripides Kyriakides

Evripides Kyriakides

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Doctoral Candidate: Evripides Kyriakides

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The present Doctorate Dissertation was submitted in partial fulfillment of the requirements for the Degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering, and was approved on May 18th, 2016 by the members of the Examination Committee.

Examination Committee:

Committee Chair ______________________
Constantinos Pitris, Ph.D., M.D.

Research Supervisor ______________________
Georgios Ellinas, Ph.D.

Committee Member ______________________
Stavros Iezekiel, Ph.D.

Committee Member ______________________
Matthew Zervos, Ph.D.

Committee Member ______________________
Shahar Kvatinsky, Ph.D.

Evripides Kyriakides

Evripides Kyriakides

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Evripides Kyriakides

Evripides Kyriakides

Περίληψη

Οι συσκευές μνημοαντίστασης προτάθηκαν αξιωματικά το 1971 και απαντήθηκαν για πρώτη φορά το 2008, παρόλο που έχουν υπάρξει για πολύ μεγαλύτερο χρονικό διάστημα. Κυκλώματα προσομοίωσης συσκευών μνημοαντίστασης είχαν χτιστεί και στο παρελθόν, αλλά υπέφεραν είτε από μεγάλες τοπολογίες ή από υπερβολικές απαιτήσεις σε χώρο και ισχύ. Οι χαρακτηριστικές ιδιότητες των μονολιθικών συσκευών μνημοαντίστασης, όμως, υπόσχονται σημαντικές βελτιώσεις σε διάφορους τομείς της μικροηλεκτρονικής. Στο πλαίσιο της αρχιτεκτονικής υπολογιστών von Neumann, προσφέρουν σημαντικά πλεονεκτήματα που θα μπορούσαν να αποδειχθούν ζωτικής σημασίας για τη συνέχιση των σημερινών τάσεων κλιμάκωσης. Με την προσθήκη τους στην εργαλειοθήκη των ηλεκτρονικών συσκευών, νέες εφαρμογές - ή βελτιώσεις υφισταμένων - προτείνονται. Αλλά κυρίως, μπορούν να χρησιμοποιηθούν για την υλοποίηση ηλεκτρονικών συνάψεων, που παρουσιάζουν πλαστικότητα και μάθηση.

Η μελέτη αυτή έχει ως στόχο την μοντελοποίηση, την κατασκευή και τον χαρακτηρισμό των εν λόγω συσκευών μνημοαντίστασης και την ενσωμάτωσή τους σε πρωτότυπες βιομιμητικές εφαρμογές. Για το σκοπό αυτό, περιγράφεται ο σχεδιασμός και η κατασκευή νέων συσκευών μνημοαντίστασης: μία συσκευή μνημοαντίστασης έξυπνου κράματος νικελίου-τιτανίου (NiTi) και μία μνημοαντίσταση χαλκού/πεντοξειδίου τανταλίου (Cu/Ta_2O_5). Είναι εντός του πεδίου εφαρμογής της παρούσας εργασίας η αξιολόγηση των χαρακτηριστικών αυτών των συσκευών και η εξαγωγή μοντέλων συμπεριφοράς για να καταστεί δυνατή η ένταξή τους στο σχεδιασμό κυκλωμάτων. Ως εκ τούτου, ο εκτεταμένος χαρακτηρισμός και μοντελοποίηση που εκτελέστηκαν σε αυτές τις δομές παρουσιάζονται ενδελεχώς. Αυτό περιλαμβάνει θερμική προσομοίωση, εκτός από θερμικές και ηλεκτρικό χαρακτηρισμό, για τη συσκευή NiTi. Ο ηλεκτρικός χαρακτηρισμός για τη συσκευή Cu/Ta_2O_5 περιλαμβάνει καθεστώτα συνεχούς ρεύματος, εναλλασσόμενου ρεύματος, και παλμού. Μοντέλα προσομοίωσης κατασκευάστηκαν για κάθε συσκευή και υλοποιήθηκαν σε Hardware Description Language (HDL). Τα μοντέλα ταιριάζουν με επιτυχία με τις μετρήσεις μέσω προσομοιώσεων, επιτρέποντας την ένταξή τους σαν ενότητες σε κυκλώματα. Τέλος, η μελέτη αυτή εμπεριέχει την κατασκευή εφαρμογών κυκλωμάτων που εκμεταλλεύονται τις ιδιότητες μνημοαντίστασης. Αρχικά, παρουσιάζεται ένας ταλαντωτής χαμηλής συχνότητας που βασίζεται σε συσκευή μνημοαντίστασης και που απευθύνεται

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στον παράγοντα του χώρου. Στη συνέχεια, ένα νευρομορφικό σύστημα που ενσωματώνει τις κατασκευασμένες μνημοαντιστάσεις Cu/Ta_2O_5 φτιάχνεται για να διερευνήσει τη δυνατότητα της πλαστικότητα και της μάθησης και χρησιμοποιώντας μνημοαντιστάσεις. Τα κυκλώματα που είναι σχεδιασμένα για αυτό το σκοπό αναλύονται και το δίκτυο αξιολογείται.

Κατά τη διαδικασία της παρούσας διατριβής, συσκευές μνημοαντίστασης, τα βασικά δομικά στοιχεία της βιοεμπνευσμένης αρχιτεκτονικής, κατασκευάζονται και μελετούνται. Οι μοναδικές τους ιδιότητες στοιχειοθετούνται και μοντελοποιούνται. Ακολούθως, ενσωματώνονται στο σχεδιασμό και την κατασκευή νέων βιοεμπνευσμένων εφαρμογών.

Επισκόπηση κεφαλαίων

Το Κεφάλαιο 1 καθορίζει το κίνητρο για την εργασία αυτή. Οι όροι «βιοεμπνευσμένο κύκλωμα» και «συσκευή μνημοαντίστασης» εισάγονται και διηγείται συνοπτικά η κατάσταση των εν λόγω τεχνολογιών. Ακολούθως, αναθεωρείται η τρέχουσα τεχνολογία υπολογιστών, ενώ τα πλεονεκτήματα της βιοεμπνευσμένης αρχιτεκτονικής αναλύονται και οι λόγοι για την επιλογή μνημοαντιστάσεων ως βασικό δομικό στοιχείο εξηγείται. Τέλος, ορίζονται οι στόχοι της έρευνας.

Το Κεφάλαιο 2 ξεκινά με μια ιστορική προοπτική για το βιοεμπνευσμένο σχεδιασμό, εντοπίζοντας τα βιολογικά θεμέλια της νευρομορφικής αρχιτεκτονικής. Στη συνέχεια, παρέχει μια λεπτομερή περιγραφή των συσκευών μνημοαντίστασης και αναλύει τις μοναδικές τους ιδιότητες. Προχωρά με την κατάσταση της τεχνολογίας στην συσκευές μνημοαντίστασης, κατηγοριοποιώντας και απαριθμώντας τα είδη των συσκευών που απαντώνται στη βιβλιογραφία, καθώς και αναλύοντας το μηχανισμό που προκαλεί τη συμπεριφορά μνημοαντίστασης. Κατά τη διαδικασία αυτή, οι δομές των διατάξεων αποκαλύπτονται σε συνδυασμό με τις αντίστοιχες διαδικασίες κατασκευής τους.

Το Κεφάλαιο 3 παρουσιάζει την πρώτη επιλογή δομής για αυτή την έρευνα. Η διάταξη, στη βάση NiTi, περιγράφεται λεπτομερώς. Μετά από εξέταση των μεθόδων παραγωγής που χρησιμοποιούνται, καλύπτονται οι μεθοδολογίες χαρακτηρισμού και προσομοίωσης. Ακολούθως, αναφέρονται οι μέθοδοι που χρησιμοποιούνται για την μοντελοποίηση των

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κατασκευασμένων συσκευών NiTi. Τα προκύπτοντα μοντέλα αντιπροσωπεύονται σε Verilog-A και συγκρίνονται με τα αντίστοιχα αποτελέσματα χαρακτηρισμού.

Το Κεφάλαιο 4 παρουσιάζει τη δεύτερη επιλογή δομής για αυτή την έρευνα. Η συσκευή, που βασίζεται σε Cu/Ta_2O_5, περιγράφεται λεπτομερώς. Μετά από μία επανεξέταση των τεχνικών κατασκευής ημιαγωγών, παρουσιάζεται η κατασκευή της δομής σε cleanroom. Οι διαδικασίες ηλεκτρικού χαρακτηρισμού και τα συναφή αποτελέσματα για την κατασκευασμένη συσκευή καλύπτονται στη συνέχεια. Ακολούθως, αναφέρονται οι μέθοδοι που χρησιμοποιούνται για την μοντελοποίηση των κατασκευασμένων συσκευών Cu/Ta_2O_5. Τα προκύπτοντα μοντέλα αντιπροσωπεύονται σε Verilog-A και συγκρίνονται με τα αντίστοιχα αποτελέσματα χαρακτηρισμού.

Το Κεφάλαιο 5 παρουσιάζει τα κυκλώματα στη βάση συσκευών μνημοαντίστασης που σχεδιάζονται και κατασκευάζονται στα πλαίσια της παρούσας διατριβής. Καταρχάς, αναλύει ένα σχέδιο ταλαντωτή χαλάρωσης και παραθέτει τα συγκριτικά του πλεονεκτήματα. Ακολούθως, περιγράφει λεπτομερώς το σχεδιασμό και τη λειτουργικότητα ενός δικτύου εκμάθησης. Το σχέδιο υλοποιείται σε Cadence Virtuoso και οι ενότητές του παρουσιάζονται χωριστά. Μετέπειτα, η συμπεριφορά του κατασκευασμένου κυκλώματος επιβεβαιώνεται και συγκρίνεται με τη σχετική βιβλιογραφία.

Το Κεφάλαιο 6 συνοψίζει το έργο που επιτελέστηκε σε αυτή τη διατριβή. Οι συσκευές μνημοαντίστασης και οι εφαρμογές εξετάζονται, τονίζοντας τα βασικά τους αποτελέσματα. Στη συνέχεια, παρατίθενται οι συνεισφορές αυτής της μελέτης και προτείνονται μελλοντικές κατευθύνσεις έρευνας στους τομείς των συσκευών μνημοαντίστασης και των βιοεμπνευσμένων εφαρμογών.

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Abstract

Memristive devices were postulated in 1971 and identified in 2008, even though they have existed for much longer. Memristive-device-emulating circuits had been built in the past, but suffered from either large topologies or excessive area and power requirements. The distinctive properties of monolithic memristive devices, however, hold promise for significant improvements in various areas of microelectronics. In the framework of von Neumann computer architecture, they offer significant advantages that could prove crucial in continuing current scaling trends. With their addition to the toolbox of electronic devices, novel applications - or improvements to existing ones - are being proposed. But most significantly, they can be used for implementing electronic synapses, exhibiting plasticity and learning.

This thesis is aimed at modeling, fabricating and characterizing such memristive devices and incorporating them in prototype bioinspired applications. To that end, the design and fabrication of novel memristive devices is reported: a nickel titanium (NiTi) smart alloy memristive device and copper/tantalum pentoxide (Cu/Ta_2O_5) memristor. It is within the scope of this work to evaluate the characteristics of these devices and extract behavioral models to enable their integration into circuit design. Therefore, the extensive characterization and modeling performed on these structures is comprehensively presented. This includes thermal simulation, in addition to thermal and electrical characterization, for the NiTi device. Electrical characterization for the Cu/Ta_2O_5 device includes DC, AC, and pulse regimes. Behavioral models were constructed for each device and implemented in Hardware Description Language (HDL). The models were successfully matched to measurements through simulations, enabling their inclusion as modules in circuits. Finally, this study encompasses constructing circuit applications exploiting memristive properties. First, a low-frequency memristor-based oscillator addressing space considerations is presented. Next, a neuromorphic system incorporating the fabricated Cu/Ta_2O_5 memristors is built to investigate the possibility of plasticity and learning using memristors. The circuits designed for this purpose are thus analyzed and the network evaluated.

In the process of this thesis, memristive devices, the basic building blocks of bioinspired architecture, are built and studied. Their unique properties are established and modeled. Subsequently, they are incorporated in the fabrication of novel bioinspired applications.

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Overview of chapters

Chapter 1 establishes the motivation for this thesis. The terms "bioinspired circuit" and "memristive device" are introduced and a concise account of their state-of-the-art is narrated. Subsequently, current computing technology is reviewed, whereas the merits of bioinspired architecture are analyzed and the reasons for choosing memristive devices as the basic building block are explained. Finally, the research objectives are laid out.

Chapter 2 starts with a historical perspective on bioinspired design, tracing the biological foundations of neuromorphic architecture. It then provides a detailed description of memristive devices and analyzes their unique properties. It proceeds with the state-of-the-art in memristive devices, grouping and enumerating the types of devices encountered in the literature, as well as analyzing the specific mechanism that causes memristive behavior. In the process, memristive structures are revealed in tandem with their respective fabrication procedures.

Chapter 3 presents the first choice of structure for this research. The device, based on NiTi, is described in detail. Following an examination of the manufacturing methods utilized, the characterization and simulation methodologies are covered. Subsequently, the methods used for modeling the fabricated NiTi devices are reported. The resulting models are represented in Verilog-A and compared to the respective characterization results.

Chapter 4 presents the second choice of structure for this research. The device, based on Cu/Ta_2O_5, is described in detail. Following a review of semiconductor fabrication techniques, the cleanroom fabrication of the structure is presented. The electrical characterization procedures and associated results for the fabricated device are then covered. Subsequently, the methods used for modeling the fabricated Cu/Ta_2O_5 devices are reported. The resulting models are represented in Verilog-A and compared to the respective characterization results.

Chapter 5 introduces the memristive-device-based circuits designed and fabricated as part of this thesis. At first, it analyzes a relaxation oscillator design and lists its comparative advantages. Then, it details the design and functionality of a learning network. The design is implemented in Cadence Virtuoso and the modules are separately presented. The behavior of the fabricated circuit is then established and compared to the pertinent literature.

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Chapter 6 summarizes the work done in this thesis. The memristive devices and applications are reviewed, with their key results highlighted. It goes on to list the contributions of this study and propose future directions of research in the fields of memristive devices and bioinspired applications.

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List of Acronyms and Abbreviations

3D IC	Three-Dimensional Integrated Circuit
a-Si	Amorphous Silicon
AC	Alternating Current
ADC	Analogue-to-Digital Converter
AHDL	Analog Hardware Descriptive Language
ALD	Atomic Layer Deposition
ASIC	Application Specific Integrated Circuit
ASIP	Application-Specific Instruction-Set Processor
BRAIN	Brain Research through Advancing Innovative Neurotechnologies
CMOS	Complementary Metal-Oxide Semiconductor
CL	Current Limiter
CMP	Chemical Mechanical Polishing
CNT	Carbon Nanotube
CPU	Central Processing Unit
DC	Direct Current
DMM	Digital Multimeter
DRAM	Dynamic Random Access Memory
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
E-beam	Electron beam
EBL	Electron Beam Lithography
FESEM	Field Emission Scanning Electron Microscope
FET	Field-Effect Transistor
FIB	Focused Ion Beam
FLOPS	Floating-Point Operations per Second
FPGA	Field-Programmable Gate Array
G-O	Graphene Oxide
GPU	Graphics Processing Unit
HDL	Hardware Description Language
HRS	High Resistance State
IC	Integrated Circuit

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ILP	Instruction Level Parallelism
IMT	Insulator-Metal Transition
IPA:MIBK	Isopropanol:methyl-isobutyl-ketone
LB	Langmuir-Blodgett
LF	Low Frequency
LIF	Leaky Integrate-and-Fire
LOR	Lift-Off Resist
LPCVD	Low-Pressure Chemical Vapor Deposition
LRS	Low Resistance State
LTD	Long-Term Depression
LTO	Low Temperature Oxide
LTP	Long-Term Potentiation
MIM	Metal-Insulator-Metal
MMA/MAA	Methyl-methacrylate/methacrylic-acid
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MRAM	Magnetoresistive Random-Access Memory
NA	Acceptor Concentration
NiTi	Nickel Titanium
NMP	N-Methyl-2-Pyrrolidone
p-Si	p-type Silicon
PANI	Polyaniline
PCB	Printed Circuit Board
PCM	Phase-Change Memory
PCMO	Pr1-xCaxMnO3
PEB	Post Exposure Bake
PEO	Polyethylene Oxide
PLD	Pulsed Laser Deposition
PMMA	Poly(methyl-methacrylate)
poly-Si	poly-crystalline Silicon
PR	Photoresist
PTFE	Polytetrafluoroethylene
RF	Radio Frequency
RIE	Reactive Ion Etchant
RRAM	Resistive Random-Access Memory
SEM	Scanning Electron Microscopy
SMA	Shape Memory Alloy

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SMU	Source Measurement Unit
SOG	Spin-on Glass
SOI	Silicon on Insulator
STDP	Spike-Timing-Dependent Plasticity
TRIS	Tris(hydroxymethyl)aminomethane
TSV	Through-Silicon Via
UV	Ultraviolet
XRD	X-Ray Diffraction

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Chapter 1

Introduction

1.1 Why bioinspired systems?

The evolution of modern microelectronics is nothing short of a collective feat for humanity. Starting from the advent of the mechanical computer by Charles Babbage in 1822, the evolution of computing has been astounding. Beginning with mechanical components and moving from vacuum tubes to transistors and then on to Integrated Circuits (ICs), computers became physically smaller, faster, and with more memory capacity. The enhancement in these metrics happened at a very fast pace, colloquially known as “Moore’s Law” [1]. Computer architecture and software promptly followed this evolution to make the most out of available computing hardware. The most recent performance milestone was set in June 2013 by the Tianhe-2, a supercomputer able to reach 33.86 peta Floating-Point Operations per Second (FLOPS) [2].

It is evident that computers have excelled in what they were developed for. Be it tabulation, data manipulation, task automation, mathematical computations, or iterative calculations, current computing systems perform extremely well. But when it comes to making unsupervised intelligent decisions they have yet to deliver significant results.

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1.2 Current computing technology

There have been attempts at mimicking human intelligence using current complementary metal-oxide semiconductor (CMOS) technology. These attempts have had some limited success, but at a great expense. IBM’s Deep Blue computer set a world-first by becoming

the first machine to beat the reigning world champion, Garry Kasparov, at a chess game. However, this machine had a volume of approximately 2000 times that of the human brain and consumed about 15 kW, compared to the brain's roughly 20 W. Watson was another supercomputer built by IBM to compete in a televised quiz show called "Jeopardy!". In 2011 it competed in the show claiming the first prize against two former winners. Watson was reported as having the size of a master bedroom and consuming 80 kW of power.

If the aforementioned machines are to match the cognitive abilities of biological organisms, they need to match the associated metrics. But plans to make these machines smaller and less power consuming face the danger of running into a "Brick Wall" [3]. This notion is composed of three insurmountable obstacles to the enhancement, scaling, and curbing of power consumption of electronics: (a) The "Power Wall" - faster computation results in more heat emission, (b) The "Memory Wall" - CPU on-board memory is limited because of the difficulty of routing too many pins, and (c) The "Instruction Level Parallelism (ILP) Wall" - the deeper the instruction pipeline, the deeper the power hole.

This is exemplified in the breakdown of "Dennard Scaling" [4]. "Dennard Scaling" states that Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) power density stays constant with decreasing transistor size. Therefore, transistor voltage and current decrease proportionally to the transistor scaling factor, meaning power use decreases proportionally to the square of the scaling factor. Evaluating "Dennard Scaling" in contradistinction to "Moore's Law", it becomes clear that although "Moore's Law" has proven consistent through the years - with minor adjustments - "Dennard Scaling" appears to have broken down circa 2005, as illustrated in Fig. 1.1. The reasons for that are the - originally unaccounted for - current leakage and thermal runaway at these dimensions, which are approximating atomic scales. The result is that the improved performance expected by "Moore's Law" has not materialize over recent years.

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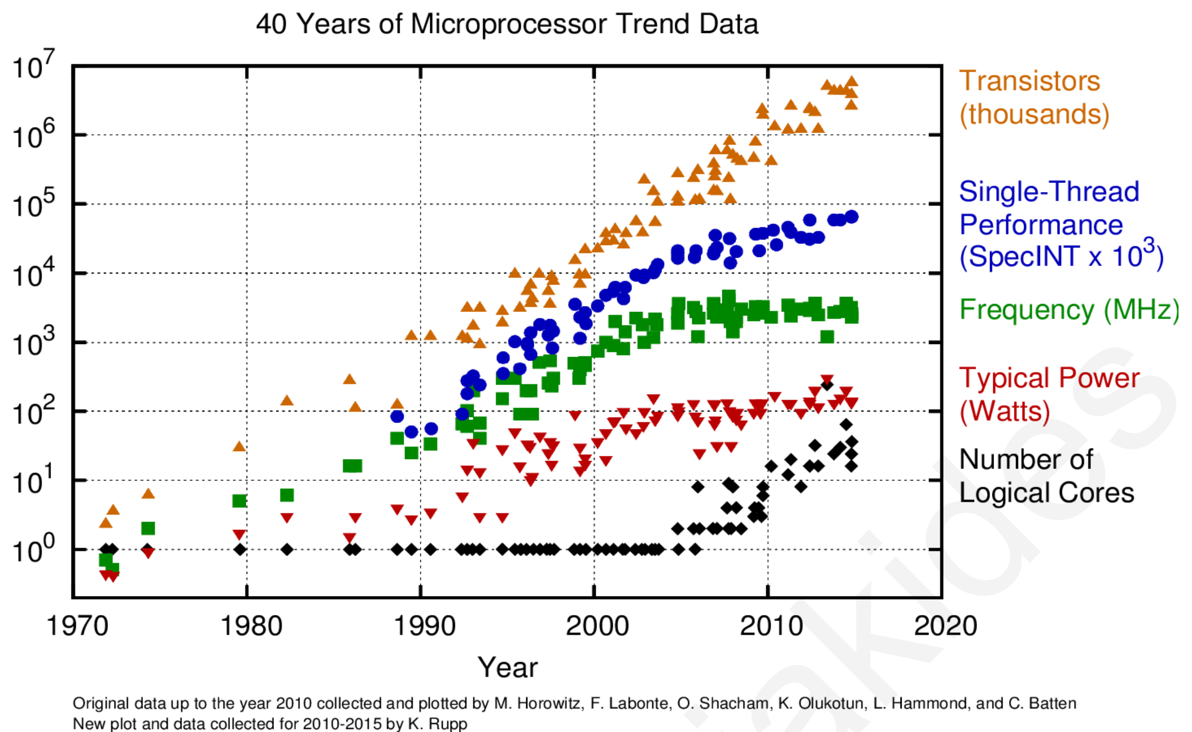

Figure 1.1: Evolution of microprocessor data over 40 years.

The microelectronics industry has proposed solutions to circumvent the "Brick Wall" [6]. One such innovation is Dynamic Voltage Scaling. In order to reduce power consumption and curb heat emission, i.e. the "Power Wall", the Central Processing Unit (CPU) can have independent power supplies for each of its components. In this way, each of the CPU's components can be operating at a different voltage level or even be powered off, depending on predefined strategies. This solution is used by both Intel and AMD. However, due to the large cache size on modern microprocessors, it can only produce a fractional impact. A similar approach involves Dynamic Frequency Scaling. But the frequency's effect on power dissipation is only linear. It is static - rather than dynamic - power consumption that dominates in modern CPUs.

CPU on DRAM is a solution proposed for the "Memory Wall". This solution is aiming to increase the memory bandwidth by bringing the CPU and memory physically closer. The cost of placing the memory and cache closer to the CPU has been too high to lead to commercialization [7]. Conversely, moving the CPU closer to the memory provided better results. A simplified CPU with three metal layers added to a Dynamic Random Access Memory (DRAM) has been demonstrated [8], however this necessitated a simplified CPU and resulted in a slower execution, as DRAM transistors are about 20% slower.

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A well-established architecture optimization approach involves the use of specialized microprocessors. These microprocessors trade flexibility for efficiency. A Graphics Processing Unit (GPU) specializes in graphics manipulation. It utilizes parallelism and proves very efficient when working with large chunks of independent data, i.e. graphics. Application Specific Integrated Circuits (ASICs) follow the same model in optimizing ICs for specific tasks. This specialization, though, comes at the cost of flexibility. Field-Programmable Gate Arrays (FPGAs) come to balance the trade-offs between specialization and flexibility. They are more efficient than CPUs with more flexibility than GPUs and ASICs. Another intermediary solution proposed is the application-specific instruction-set processor (ASIP). As a component in a system-on-a-chip, ASIP is based on an instruction set specifically designed to suit a specific application. However, it has been shown that system flexibility, short development time, and low technology cost eventually result in decreased performance [9].

The Three-Dimensional Integrated Circuit (3D IC) approach involves stacked wafers or dies, interconnected vertically using Through-Silicon Vias (TSVs) to behave as a unitary IC. Otherwise, a monolithic 3D IC can be manufactured in layers on a single wafer without the need for interconnections. The advantages stemming from this architecture include shorter wiring length, higher bandwidth, smaller footprint and lower power consumption. However, this design suffers from the innate difficulty of working with inner layers, design complexity, and heat dissipation [10].

In summary, it is evident that despite the immense improvement in microelectronics and computer architecture, current CMOS-based systems would require vast enhancements if they are to match biological neural organisms' performance. And it is becoming increasingly challenging to improve performance with the rates that have been recorded so far. The "Brick Wall" signals the difficulty in improving current CMOS technology, which might be reaching its limits. Further improvements will focus on carefully balancing the three aforementioned tradeoffs instead of simultaneously improving all of its characteristics. If our aim is to accomplish nature's performance in intelligence then we need some radically different foundations to build upon.

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1.3 Bioinspired design

A fly's nervous system consists of no more than a few hundred cells. Yet it can perform functions and flying maneuvers that not even the most advanced military aircraft can. Despite their immense onboard processing power, digital electronics with billions of transistors and more than a century of evolution, today's cutting-edge aircraft cannot mimic a biological system as simple as a fly. The versatility of the fly's organism, that can also feed itself, avoid danger, procreate, etc., make the comparison even more comprehensive. What might appear as a paradox at first, is in fact nothing more than nature's work over millions of years. Through the process of evolution, nature progressively eliminates organisms' less advantageous characteristics over others that provide them more chances of survival [11]. This is a continuous process that helps organisms adapt in an ever-changing environment and gain comparative advantages over competing species. Therefore, what we regard today as "intelligence" is nature's most powerful tool gifted to organisms for survival. Hence, if our aim is to mimic biological intelligence, then learning from nature and developing bioinspired solutions is a task worth pursuing.

Realizing this, the E.U. and U.S. have initiated two flagship projects. The first of these is the Human Brain Project. The Human Brain Project is a 10-year E.U.-funded project. Established in 2013 and with a budget estimated to exceed €1 billion, it aims to bring together all existing knowledge about the human brain and reconstruct it in a supercomputer simulation. Although predominantly a neuroscience project, aiming to find the connection between "genes, molecules and cells to human cognition and behavior" [12], it also aims to develop new platforms for neuromorphic computing. In the same vein as the Human Brain Project, the BRAIN (Brain Research through Advancing Innovative Neurotechnologies) Initiative was instigated by the U.S. government in 2013. Based on the Human Genome Project, the initiative aims to assemble a complete map of neurons in the human brain. BRAIN is planned to receive more than $3 billion in funding over the next 10 years. These projects approach the matter from the neuroscience perspective, while another significant project took a different approach; U.S.'s DARPA has initiated the SyNAPSE program to develop "cognitive computers" or "brains-on-chips". A key element to the success of such a venture is the ability to develop compact synapses on chips.

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1.4 Memristive Devices

In 1971 Professor Leon Chua of the University of California at Berkeley published his seminal paper on the theoretical prediction of a fourth fundamental circuit device [13]. The paper postulated that besides the resistor, inductor and capacitor, a fourth fundamental circuit element would relate charge with magnetic flux (see Fig. 1.2). This element which he called a memory resistor, or memristor, would in effect vary its resistance according to the supplied input. It would also maintain its state in the absence of applied bias. Although devices exhibiting memristive behavior appeared numerous times in the literature in the meantime [14, 15, 16, 17], they were not identified as such. It was not until 2008 - 37 years after Chua's prediction - that HP Labs succeeded in fabricating and proving the function of a memristor. This was accomplished using a $Pt/TiO_2/Pt$ sandwich device [18]. At the time, it was also established that a memristance effect arises naturally in nanoscale systems, in which solid-state electronic and ionic transport are coupled under an external bias voltage [18]. Since then, memristance effects have been demonstrated in organic [19], polymeric [20] silicon [21], and graphene-based [22] devices, among others. Furthermore, since the original definition, memristor devices have been included in a broader class of memristive devices (see Chapter 2).

Prototypes and applications based on memristive devices have already been presented. Chu et al. have demonstrated a hardware system for visual pattern recognition [23]. Using PCMO memristors, the system has been shown to successfully recognize number images. Suri et al. have implemented a visual pattern extraction system [24]. This was accomplished using three different types of memristive devices: $Ge_2Sb_2Te_5$, Ag/GeS_2-based, and HfO_x-based. The fastest memristive device to reach the market is anticipated to be in the form of Phase-Change Memory (PCM). Western Digital have announced a PCM solid-state drive with random read access latency of 1.5 μs [25]. That is claimed to be two orders of magnitude smaller than the fastest NAND flash drive available on the market. More recently, IBM claim to have made significant progress in storage reliability and data retention with an array of 64,000 3-bit PCM cells [26]. Notably, this was achieved at elevated temperatures and following one million endurance cycles.

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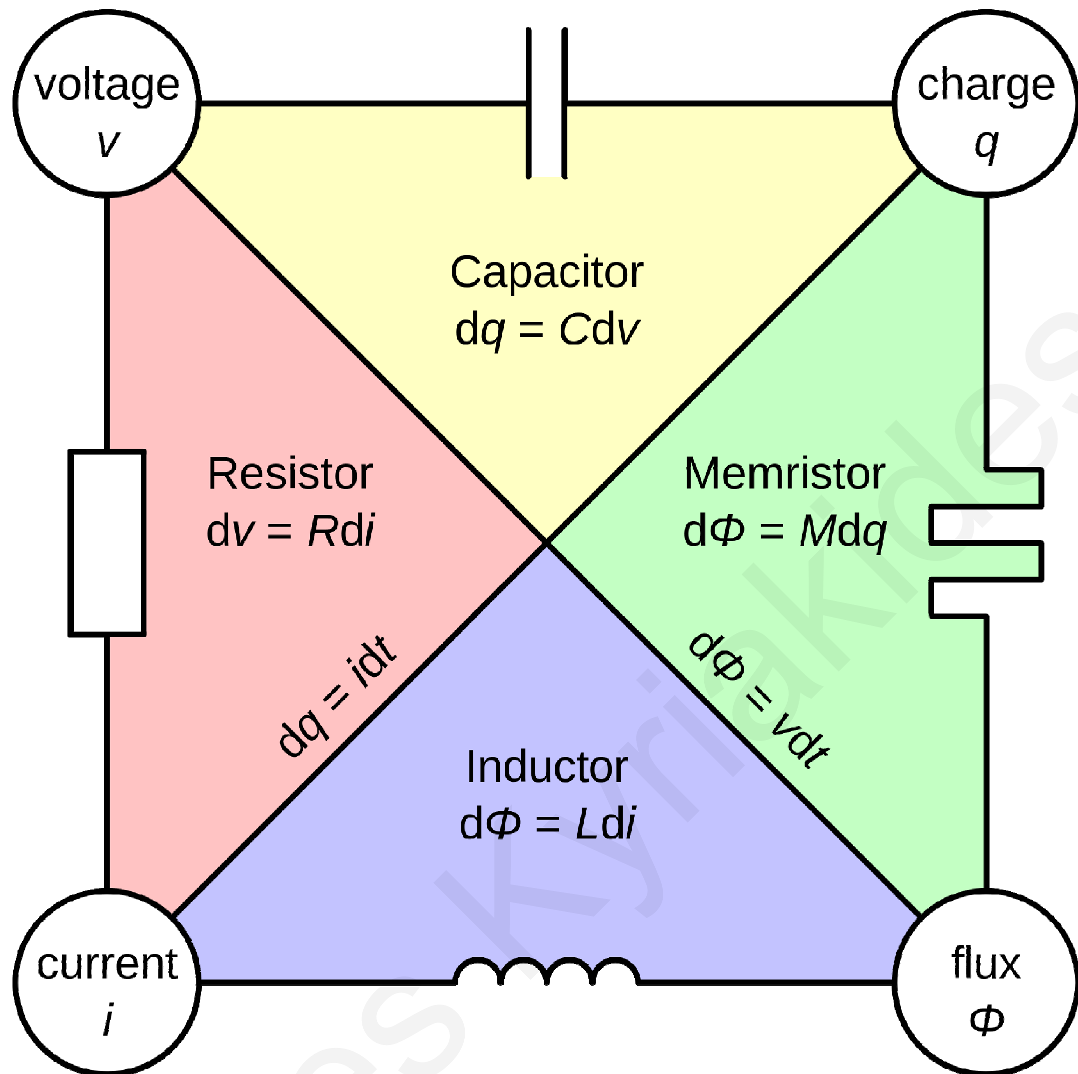

Figure 1.2: The four fundamental circuit elements.

It is thus apparent that the discovery of the memristor has opened a new domain to the semiconductor industry. The behavior of a memristor can be emulated by an impractically large circuit [28], however, as a single device, the memristor can significantly impact the future of computing.

Memristive devices may prove to be the technology of choice for the next generation of non-volatile memory. Most importantly, they appear to be the ideal way to simulate the function of synapses, the basic building block of the mammalian nervous system.

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1.5 Research objectives

The first memristive devices have already been fabricated. Nevertheless, two important steps have yet to be taken. Firstly, the physical mechanisms behind memristance have not been conclusively explained or proven, and secondly, memristive devices have not yet been used in applications where their unique properties will be fully utilized. The objective of this study is to aid towards tackling these two issues and also add to the general body of knowledge on memristive devices.

HP Labs' TiO_2-based device is only one of the possible methods to implement a memristor. However, since the device concept has been proven and the first memristors have been shown to conform to Chua's prediction, new types of memristive devices are expected to surface. Contributing to that cause, the aim of this study is to design and build new memristive devices. This is both necessary, since memristive devices are not commercially available, and desirable, since it enables device parameter variation analysis.

There is an ever-broadening bibliography on nanostructures exhibiting memristive behavior. Drawing from previously acquired expertise, novel memristive devices are proposed in the form of NiTi and Cu/Ta_2O_5 devices. Literature review, solid state analysis and modeling enable the investigation of the properties of the most appropriate of these devices and find correlations between the device characteristics and output function. The results provide the means to control the device structure, layer properties, and fabrication steps to achieve the required response. Furthermore, fabricating components that can be integrated into ICs is one of the primary constraints being pursued. This necessitates all devices to be CMOS-process-compatible, thereby significantly decreasing system footprint, manufacturing costs and power consumption - the comparative advantages over current state-of-the-art memristor-emulating circuits.

The ensuing fabrication process and the challenges in order to reach the required profile are presented. The most important aspect of memristive behavior under investigation is the exhibited hysteresis. Hysteresis results in the typical bow-tie loop in the I-V plot. It is this attribute that facilitates the desired non-linear conductance. This is the key trait for the design of bioinspired architecture and neural circuits, since it can be correlated with plasticity and memory effects.

Memristive devices, with their unique properties, can become the stepping stone for a paradigm shift in many areas of analog design, embedded systems and neural networks.

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This work is targeted towards proposing new systems that exploit memristance to that effect. Thus, following device fabrication, the focus of this study shifts to the use of memristors in an integrated circuit and thus demonstrating the most important step in memristor evolution: Designing a neural circuit implementing a biomimetic function, using memristors. This will provide a proof-of-concept in the effort to make neural circuits smaller, faster and more cost-effective to build.

1.6 Synopsis

Initially, a set of devices based on NiTi alloy are investigated. NiTi-based devices offer the potential for multi-time-scale volatility. Resistance measurements performed on the devices exhibit the desired hysteresis. Multi-physics platform simulations are used to quantify their cooling process. To enable their use in circuit design, behavioral modeling is carried out based on a synthesis of ab initio calculations and simulation results. The potential for exploitation in emulating neural dynamics is investigated.

Subsequently, a set of Cu/Ta_2O_5-based devices are fabricated. Extensive measurements lead to the definition of two regions of operation. The underlying physical mechanisms are evaluated and verified ex situ. Through the process, they are shown to replicate memristor criteria. Physics-based mathematical modeling is successful in correlating their operation with diffusion-based principles.

Next, a memristor-based oscillator circuit is presented. Its novel topology utilizes memristors and features no active components. The oscillator can yield significant improvements in footprint - an issue of low-frequency oscillators. The memristor-based oscillator can emulate the function of neurons in spiking neural networks.

Lastly, a learning system implementation is presented. It illustrates the potential use of memristors as synaptic emulators. The fabricated chip is composed of the modules necessary to implement a bioinspired learning network. With the integration of memristors, the network functionality is explored and shown adept at emulating synaptic plasticity and implementing learning behavior.

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Chapter 2

Background

2.1 Introduction

This chapter introduces the two central terms of this thesis: bioinspired design and memristive devices.

The chapter begins with an introduction to bioinspired design. A brief historical review is followed by an explanation of the basic concepts that constitute the bioinspired framework, namely the structure and functionality of neurons and synapses. Further insight is provided by the Hodgkin-Huxley equations, leading to the prevalent rules of learning.

The chapter then proceeds with an overview of memristor theory. The basic theoretical formulations governing memristor functionality are presented and memristor behavioral characteristics are explained. Following the background behind the first identification of a memristor, the state-of-the-art in memristive devices, including fabrication procedures and memristance mechanisms, is recounted and summarized.

2.2 Bioinspired design

Bioinspired or neuromorphic design refers to an emerging computer architecture paradigm inspired by biological organisms' nervous system. It is an inherently interdisciplinary field, encompassing principles from neurobiology, computer architecture, computer science, electrochemistry, and device physics. The marked distinction between bioinspired architecture and the currently ubiquitous von Neumann architecture is the treatment of

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information. In von Neumann-type systems the information is processed and stored separately. In bioinspired systems the information storage and processing happens at the same node. For the reasons documented in previous sections and others promptly explored, bioinspired systems compare advantageously to alternative prospects for the next generation of computing.

The field of bioinspired design is constantly evolving and so are the potential applications being proposed [24]. Applications such as pattern recognition, classification, machine learning and optimization are already being realized in software. Natural language processing and data mining are also being investigated in software implementations. Emerging applications include big-data analytics, autonomous systems and robotics. Security-related applications such as cryptography have also been proposed. In a more innovative yet distant scenario, bioinspired systems are touted as potential candidates for future prosthetics and brain-machine interfaces.

2.2.1 Historical review

The roots of bioinspired architecture trace back to the efforts of deciphering and modeling biological neurons. In 1953 Hodgkin and Huxley's measurements on the giant axon of the squid yielded a mathematical model of the chemical process for signal propagation between biological neurons [29]. The model, referred to as the Hodgkin-Huxley model, consists of four ordinary differential equations. The originality and significance of this work led to a Nobel Prize. FitzHugh and Nagumo created a widely used neuron model with a simplified version of the Hodgkin-Huxley model [30, 31]. In 1981 Morris and Lecar combined the two aforementioned models into a model that reproduced the oscillatory behavior of the giant barnacle muscle fiber with a system of two nonlinear differential equations [32]. In 1984 Hindmarsh and Rose proposed a model based on the FitzHugh–Nagumo model comprising three coupled first order differential equations [33].

The first artificial neuron model preceded its biological counterpart. A computational model was first proposed by McCulloch and Pitts in 1943 [34]. It outputs a binary value from the weighted sum of the inputs using threshold logic. In the 1940s Hebb's learning hypothesis was put forth [35]. Based on the mechanism of neural plasticity - what is now known as Hebbian learning - it set the foundations for unsupervised learning rules. The

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perceptron, developed by Rosenblatt [36], was a pioneering algorithm implemented initially in software and later in hardware, which enabled pattern recognition. However, as a result of some erroneous predictions and hardware limitations, the momentum in the field was lost in the 1970s. A resurgence in the field took place in the 1980s. This was the result of several factors: The incorrect deductions that neural networks could not handle XOR functions were corrected, computing power increased, and the backpropagation algorithm proposed by Werbos [37] provided the solution to the XOR problem. It was in this period that efficient simulation of neural processes through parallel distributed processing, also known as connectionism, took place. In the 1990s Mead's work led to the advent of neuromorphic electronics [38] and the incorporation of MOS transistors in learning applications and storage for neuromorphic circuits. In the meantime, new implementations of bioinspired systems were developed, such as Intel's ETANN (Electrically Trainable Artificial Neural Network) and IBM's ZISC (Zero Instruction Set Computer).

Most recently though, a major momentum in the field is palpable. This has been heavily affected by the advent of the memristor and its potential applicability to Spike-Timing-Dependent Plasticity (STDP) learning. Flagship projects have been initiated, such as the E.U.'s Human Brain Project and the U.S.'s BRAIN Initiative. These have succeeded other major projects, such as the SyNAPSE program, funded by U.S.'s DARPA, the BrainScaleS, funded by E.U.'s FP7, and the Human Connectome Project, funded by U.S.'s NIH.

2.2.2 Bioinspired design framework

This section reviews the necessary concepts of neurobiology that define the framework for bioinspired architecture. An overview of neuron operation covers their basic characteristics and leads to the functionality of synapses. The Hodgkin-Huxley equations are presented, being the prevalent model of neuron response. Finally, the reasonably-established role of synapses in cognition and proposed biological learning algorithms, are examined.

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Neurons

Neurons are a type of electrically excitable cell found in eumetozoans that processes and transmits information through electrical and chemical signals. Neurons, along with glial cells, whose purpose is to give neurons structural and metabolic support, constitute an organism's nervous system.

Barring some exceptions, the majority of neurons consist of a cell body (called soma), dendrites, and an axon. As shown in Fig. 2.1, the soma is a compact structure, whereas the dendrites and axon have a filamentary shape. The dendrites and axon extrude from the soma. Dendrites branch extensively, creating dendritic trees. The axon is connected to the soma through the axon hillock. Although the axon branches, similar to dendrites, the difference is that its diameter remains approximately constant.

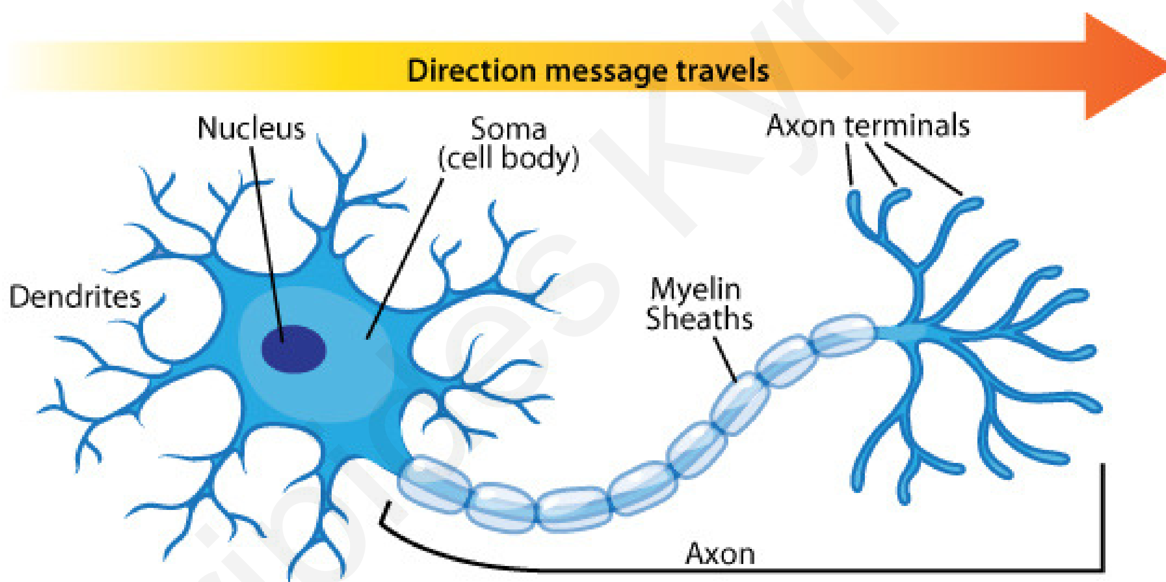

Figure 2.1: The anatomy of the biological neuron showing the direction of signal transmission.

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Neurons are connected between them through their dendrites and axon. The axon's branches terminate on the soma or the dendrites of other neurons. This connection between neurons is called a synapse. The human nervous system is a network of about 100 billion neurons, with each neuron connecting to about 10^3 - 10^4 other neurons. Thus, the brain has about 10^{14} - 10^{15} synapses.

Like all cells, neurons are enclosed by a membrane. However, the membrane of neurons has protein structures embedded in it, forming ion gates and ion channels. The variation of ion concentrations, such as Na^{+}, K^{+}, Cl^{-}, and Ca^{+2}, generates a potential difference across the membrane, i.e. between the cell and the extracellular medium, called the interstitial fluid. This enables the signal generation and transmission across the neuron.

Synapses

The key to analyzing signal transmission is found at the synapse and axon hillock. Synapses can be one of two types: chemical or electrical (Fig. 2.2). Electrical synapses are channels that form at narrow gaps between two neurons, known as a gap junctions. Electrical synapses are common in parts of the nervous system that require fast response, such as the reflexes. Their transmission time is approximately 0.2 ms [40].

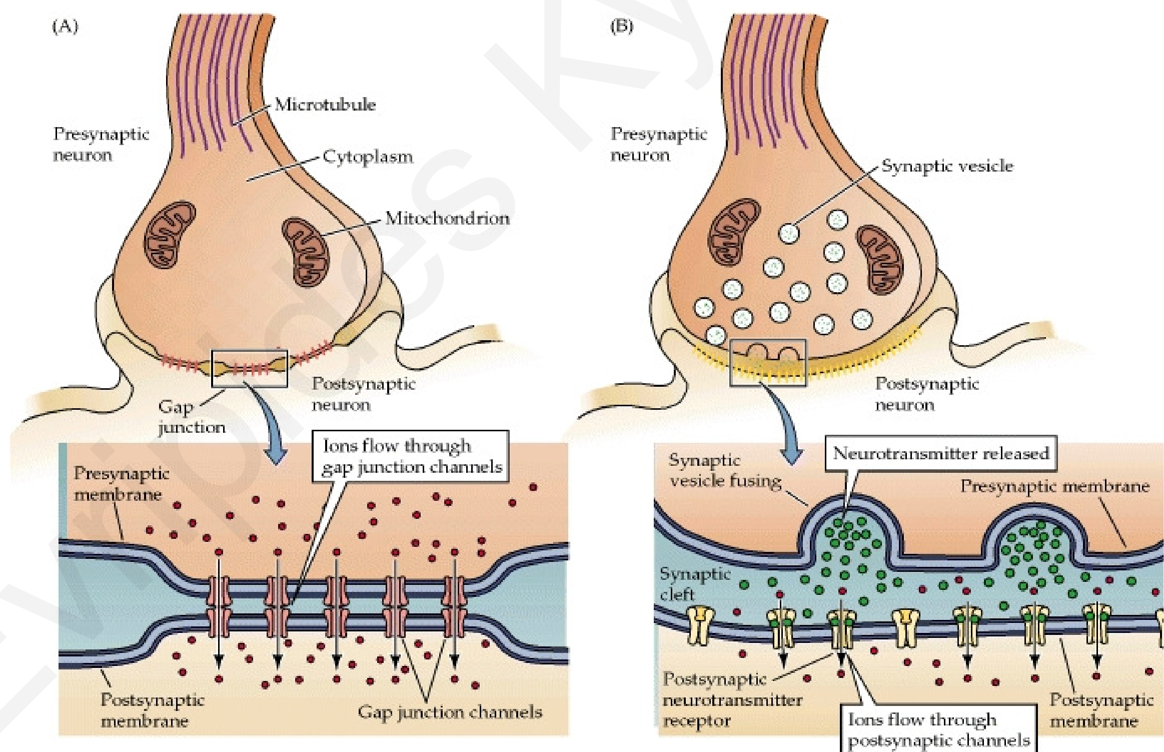

Figure 2.2: Comparison of electrical and chemical synapses.

Chemical synapses are slower. Their transmission time is approximately 2 ms [40]. Chemical synapses have a more profound role to play in the nervous system, believed to be

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responsible for cognitive functions. They form between the axon of one neuron (called presynaptic neuron) and dendrites of another (called postsynaptic neuron). When a signal arrives at the synapse from the presynaptic neuron, a sequence is initiated. Chemicals called neurotransmitters are released from synaptic vesicles of the presynaptic neuron into the synaptic gap, known as synaptic cleft. These bind to receptor molecules in the postsynaptic neuron that open or close postsynaptic ion channels. The effect is a change in the membrane potential of the postsynaptic neuron. If the postsynaptic potential is depolarized (i.e. increased), the potential becomes excitatory, whereas, if the postsynaptic potential is hyperpolarized (i.e. decreased), it becomes inhibitory. Depolarizing the postsynaptic potential from the resting potential of -70 mV can have two results. If the potential is smaller than the axon hillock's threshold (-55 mV) no signal is transmitted. If, however, the potential surpasses the axon hillock's threshold, a signal, known as an action potential, is transmitted from the axon hillock down the axon. This action is known as firing and constitutes the signal transmission mechanism of neurons [42]. An action potential has a roughly triangular shape reaching approximately 40 mV and lasts approximately 2 ms. It is followed by a refractory period during which no firing can take place. The process is illustrated in Fig. 2.3.

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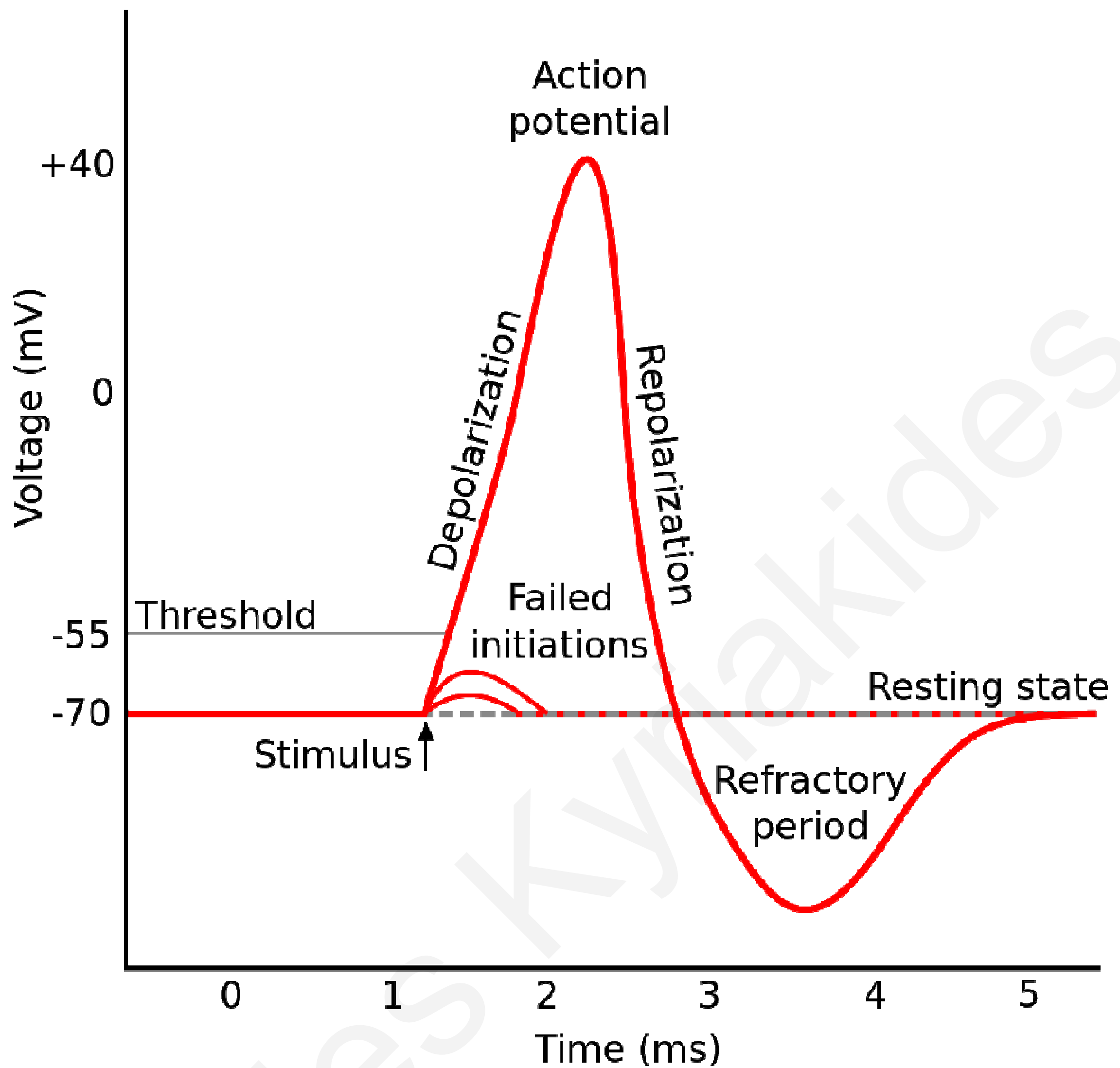

Figure 2.3: Action potential generation.

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Hodgkin-Huxley model

The most accurate quantitative treatment of the membrane potential is found in the Hodgkin-Huxley model. The model describes the chemical interaction taking place at the membrane, which is governed by ion concentrations; K^+ and large organic A^- ions inside and mainly Cl^- and Na^+ ions outside the neurons. The cell membrane is impermeable to A^- ions. At the resting state, the membrane is only permeable to K^+ and Cl^- ions. Due to the high concentration of K^+ ions inside, they diffuse to the outside. The opposite is true for the Cl^- ions. The result is an electric field across the membrane. The sustained potential difference is the resting potential shown in the previous segment and is approximately 70

mV when measured inside with respect to the outside. When above-threshold depolarization takes place, an action potential is generated, as discussed above. The cell membrane then becomes permeable to the Na^+ ions outside the cell. This causes a flow of Na^+ ions inwards. The membrane potential is thus temporarily increased, producing the action potential. The resting potential is restored by a subsequent outward flow of K^+ ions. Finally, a process involving organic molecules pumps the Na^+ and K^+ ions to restore their concentrations.

The equivalent circuit of the Hodgkin-Huxley model contains three voltage-gated ion channels that define the movement of ions across the membrane. Their conductance is a function of membrane potential. The channels are treated as gates with a probability of being open (denoted by n, m, h) or closed. The transition between open and closed states is governed by rate constants; α for the transition from closed to open, and β from open to closed.

The whole system, shown in Fig. 2.4, can thus be described in terms of four ordinary differential equations.

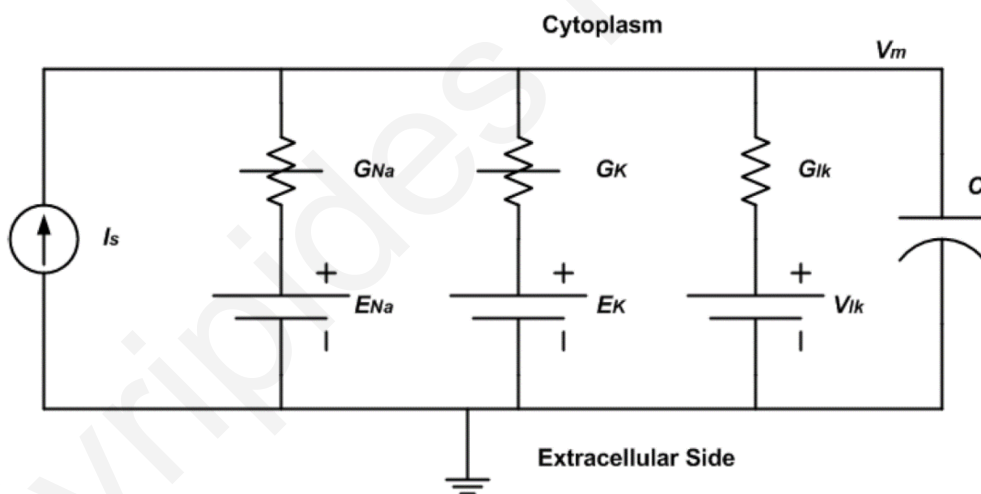

Figure 2.4: General Hodgkin-Huxley model with external stimulus.

With V_m the membrane potential, C the membrane capacitance, and I_s the external stimulus, and with Na, K, and lk denoting the sodium, potassium and leakage channels, respectively, the equations are [44]:

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$$\frac{dV_m}{dt} = -\frac{1}{\tau_{Na}}(V_m - E_{Na}) - \frac{1}{\tau_K}(V_m - E_k) - \frac{1}{\tau_{lk}}(V_m - V_{lk}) + \frac{1}{C} I_s(t) \tag{2.1}$$

$$\frac{dn}{dt} = -(\alpha_n + \beta_n)\, n + \alpha_n \tag{2.2}$$

$$\frac{dm}{dt} = -(\alpha_m + \beta_m)\, m + \alpha_m \tag{2.3}$$

$$\frac{dh}{dt} = -(\alpha_h + \beta_h)\, h + \alpha_h \tag{2.4}$$

where E_{Na}, E_K, V_{lk} are extracted parameters, and τ_{Na}, τ_K, and τ_{lk} are defined as:

$$\tau_{Na} = \frac{C}{G_{Na}} \tag{2.5}$$

$$\tau_K = \frac{C}{G_K} \tag{2.6}$$

$$\tau_{lk} = \frac{C}{G_{lk}}. \tag{2.7}$$

$0 < n, m, h < 1$ are dimensionless quantities denoting the potassium channel activation, sodium channel activation, and sodium channel inactivation probabilities, respectively. $\alpha_{n,m,h}$, $\beta_{n,m,h}$ are empirically defined rate constants. With V_r the membrane resting potential, and defining $u = V_m - V_r$, then $\alpha_{n,m,h}$ and $\beta_{n,m,h}$ are given by:

$$\alpha_n = \frac{0.01\,(10-u)}{e^{1-0.1\,u} - 1} \tag{2.8}$$

$$\beta_n = 0.125\, e^{-u/80} \tag{2.9}$$

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$$\alpha_m = \frac{0.1\,(25-u)}{e^{2.5-0.1\,u}-1} \tag{2.10}$$

$$\beta_m = 4\,e^{-u/18} \tag{2.11}$$

$$\alpha_h = 0.07\,e^{-u/20} \tag{2.12}$$

$$\beta_h = \frac{1}{e^{3-0.1\,u}+1} \tag{2.13}$$

The sodium and potassium channel conductances of Eqs. 2.5 - 2.6 are given by:

$$G_{Na} = g_{Na}\,m^3\,h \tag{2.14}$$

$$G_K = g_K\,n^4 \tag{2.15}$$

where g_{Na}, g_K denote the maximum sodium and potassium channel conductivities, respectively. G_{lk} is the leakage channel conductance and is not dependent on membrane voltage.

Qualitatively, the Hodgkin-Huxley model correctly predicts the majority of neuronal responses to stimuli, such as action potential generation, refractory period, response to multiple stimuli, etc. With adjustment to its parameters, it can be applied to other species' neurons. However, subsequent analysis of the model by Chua brought up an oversight by the authors. The sodium and potassium channels are governed by two conductances: G_{Na} and G_K. As shown by Chua, these are in fact "memristive one-ports" [45]. Therefore memristors could play a significant part in simplifying the implementation of a Hodgkin-Huxley model.

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Learning algorithms

The synapse has a more important role to play further to mere signal transmission. According to prevalent learning theories, it is also the point where information is stored. This is believed to happen through the synaptic efficacy, or the aptitude of a synapse to retransmit an action potential. It should be noted that the amplitude of the action potential is always the same. What does change is the probability of spike generation. The change in synaptic efficacy is termed plasticity. Plasticity resulting in increased efficacy is termed potentiation, whereas plasticity resulting in decreased efficacy is termed depression. Long-term changes in efficacy are believed to compose the mechanism responsible for learning and memory [46]. Long-Term Potentiation (LTP) and Long-Term Depression (LTD) mechanisms are attributed to various factors, such as changes in postsynaptic receptor density, changes in presynaptic neurotransmitter release machinery, dendritic growth, etc. [47].

Although the induction of LTP and LTD is still a matter of ongoing research, some notions have been verified by experimental data. Psychologist Donald Hebb proposed his theory on learning in his 1949 work The Organization of Behavior [35]. According to this theory, when a (neuron) cell repeatedly takes part in firing another cell, the synaptic efficacy increases. This mechanism is now known as Hebbian learning. A subtle point has been often overlooked when examining Hebbian learning: “take part” implies causality between the two events and not temporal coincidence. In fact, later experiments verified Hebb’s hypothesis. Furthermore, studies on associative memory explored the issue of timing between the firing of two adjacent neurons. Experiments on the hippocampal neuron [48] have shown that timing is critical: when the presynaptic neuron fires first, LTP is induced, whereas when the postsynaptic neuron fires first, LTD is induced. The process is illustrated in Fig. 2.5. This biological process is now known as STDP and has become a field of extensive study in biology and neuromorphic engineering.

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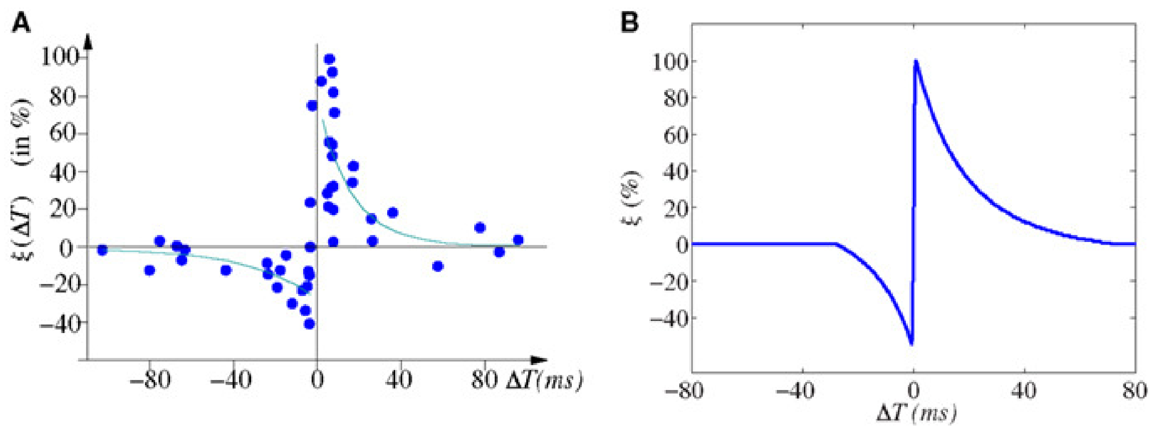

Figure 2.5: Illustration of STDP. Change in plasticity is plotted with respect to time difference of spikes of post-synaptic and pre-synaptic neuron. (A) Experimentally measured results from the hippocampal neuron. (B) Idealized STDP function.

2.2.3 Discussion

Bioinspired architecture can be implemented using existing von Neumann computing platforms or software emulation. However, the benefits of bioinspired design will maximize with the use of corresponding hardware.

Computers based on the von Neumann model of computation rely on information fetching from the memory to the processor. This creates a bottleneck that causes delay in execution, generates heat, and requires high bandwidth. The biological nervous system combines information processing and information storage at the synapse. This addresses the "Memory Wall" issue explored in previous sections.

The operation of bioinspired circuits can be asynchronous and event-driven, such that power is only dissipated during meaningful calculations [50]. Event-driven computation ensures that redundant events are not transmitted, while additionally permitting their transmission with short latencies. This offers another advantage: delocalized processing enables filtering of information, such that redundant information is rejected. An example of delocalized processing happens at the eye's retina, where preprocessing sheds unnecessary spatial and temporal information [51].

Neural circuits are inherently parallel in their design and execution. This allows complex tasks, such as image recognition, to be performed extremely fast due to time

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efficient algorithms. On the contrary, parallelism comes with its own challenges in von Neumann-type machines, exemplified by the "ILP Wall".

Neural circuits exhibit a scalability unmatched by von Neumann-based machines. In addition, they can be designed for high fault-tolerance and reliability under noise [52]. Furthermore, they are ideally suited for unsupervised learning.

A comparison of projected data comparing power efficiency of IBM's Watson and the human brain is discussed in [24]. Notwithstanding the consideration of vastly different capabilities between the two, it is shown that, even if current scaling continues, in 2020 the human brain compared to Watson will still be more efficient by three orders of magnitude.

Fig. 2.6 is indicative of the merits of bioinspired architecture, as well as its room for improvement, through the comparison of power and space efficiency of digital computers, silicon neurons (CMOS-based neuron emulators), and biological neurons. The power efficiency of digital computers is estimated to be 10^{-3} - 10^{-7} J/spike, silicon neurons have a power consumption in the order of 10^{-8} J/spike, whereas the power budget of a neuronal spike is in the order of 10^{-11} J. At the same time, a single computer core has an average size between ~50 and ~90 mm^2, silicon neurons have a footprint of approximately 4,000 μm^2, while the span of biological neurons is estimated to be roughly 10 μm^2 [53].

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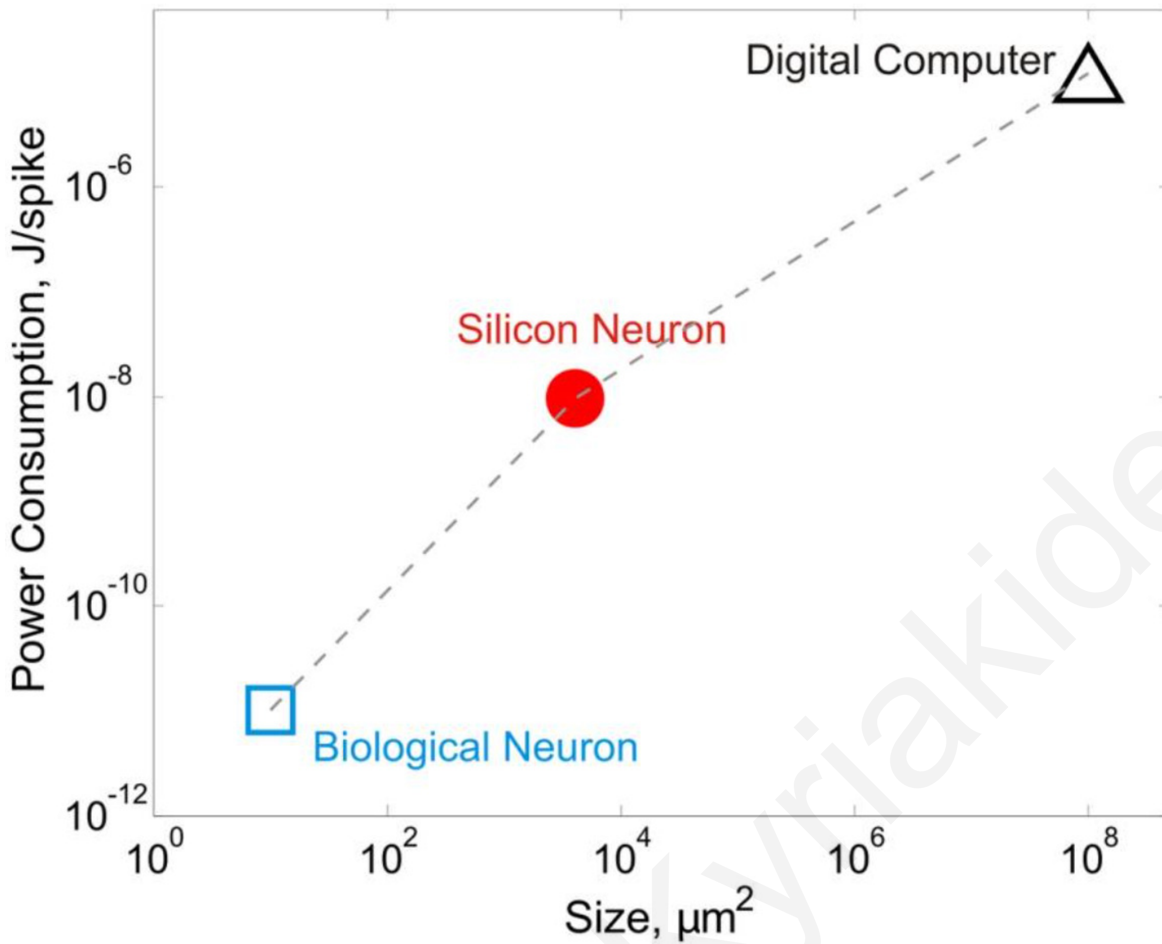

Figure 2.6: Comparison between the power and space efficiencies of digital computers, silicon neurons, and biological neurons.

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2.3 Memristive devices

Following the background behind the first identified memristor, this sections provides an overview of memristor theory. Their functionality is described and their characteristics are explained. Finally, the state-of-the-art in memristive devices is analyzed and the implementations compared in Tab. 2.1.

2.3.1 Historical review

In 1971 Professor Leon Chua of the University of California at Berkeley published his insightful paper on the theoretical prediction of a fourth fundamental circuit device [13]. Based primarily on symmetry arguments, the paper postulated that besides the resistor, inductor and capacitor, a fourth passive circuit element would relate charge with magnetic flux. This relationship has certain implications. This element, which he called a memristor, could vary its resistance according to the history of supplied input. It should also maintain its state in the absence thereof. Chua's postulation went largely unnoticed for 37 years, before, in 2008, HP Labs announced that they had managed to fabricate and prove the function of a memristor using a Pt/TiO_2/Pt sandwich device [18].

The breakthrough by HP Labs classified the memristor as the fourth fundamental passive circuit element. Its function cannot be replicated by any combination of the other three elements. Specifically, as electronics technology stands today, a complex network of at least 15 transistors and other passive elements is required to emulate the function of a memristor [28].

HP Labs also demonstrated that a memristance effect arises naturally in nanoscale systems in which solid-state electronic and ionic transport are coupled under an external bias voltage [18]. Therefore, memristors are not limited to a single implementation. In fact, memristor implementations can be especially diverse with regards to structure and materials used. E.g. sandwich devices such as the original TiO_2 [18] also include NiO-based devices [54]. Voltage-driven memristance effects have been demonstrated in molecular monolayer [19], in polymeric [20] and in amorphous silicon [21] devices. Similar effects have also been demonstrated in poly-crystalline silicon nanowires [55] and graphene-based devices [22]. Single-element electromigration-based devices have also exhibited memristance effects [56], yet at lower frequencies (< 1 Hz).

With the discovery of the memristor, a new domain has opened to the semiconductor industry. Various memristor applications have been proposed, such as non-volatile memory [57], spiking neural networks [58], implementation of the Hodgkin-Huxley model [59], and other novel solutions, such as maze solving [60]. Memristors have also been shown able to emulate the entire synapse, the interface between two neurons [61]. Hence, they can be used to build a low-cost, low-power circuit equivalent of the synapse for use in spiking neural networks and other applications.

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2.3.2 Memristor theory

Leon Chua published his seminal paper on memristors in 1971. The reasoning behind his postulation was simple:

Electricity exhibits four fundamental attributes: current, voltage, charge, and flux. There are three passive devices relating each quantity to the other (Fig. 2.7). The resistor relates current to voltage through resistance. The capacitor relates charge to voltage through capacitance. The inductor relates flux to current through inductance. But there is no device connecting flux to charge. He proceeded to postulate that such a device should exist and should possess certain attributes. The most important of these would be memory, hence the name “memristor”, a portmanteau of “memory” and “resistor”. The associated parameter - Memristance (M) - is measured in units of Ohms.

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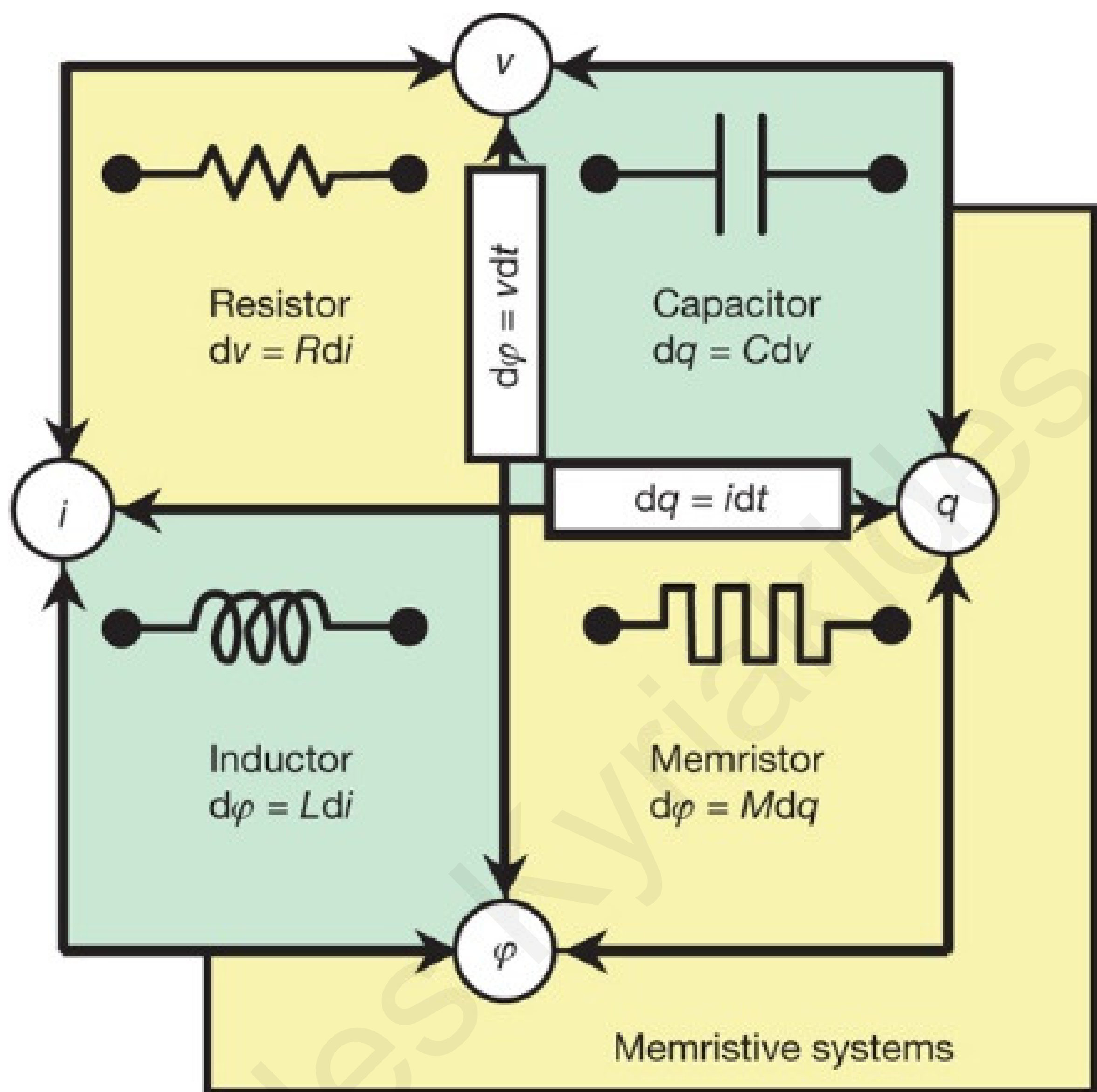

Figure 2.7: The four fundamental circuit elements.

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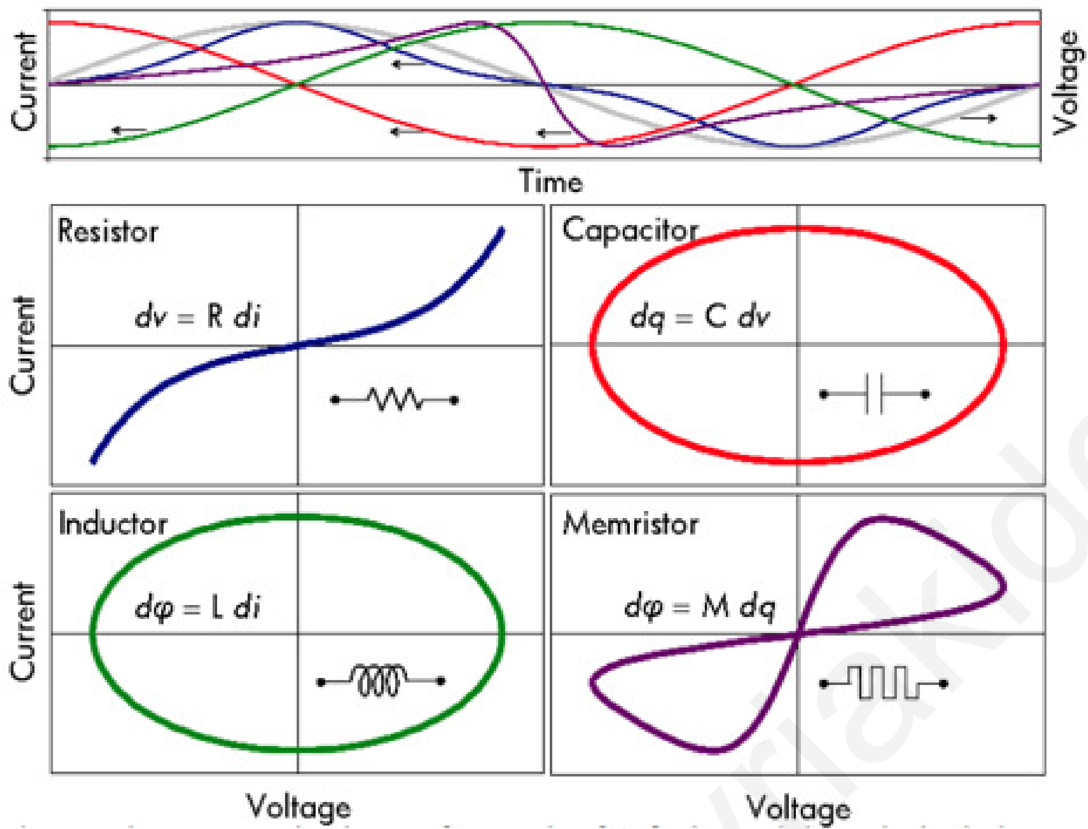

Figure 2.8: Current-voltage characteristics for the resistor, capacitor, inductor and memristor.

The memristor's distinct I-V curve is shown in Fig. 2.8 compared to those of the other three fundamental passive electronic devices. The basic mathematical definition of the current-controlled memristor is:

$$\frac{dw}{dt} = f(w, i) \tag{2.16}$$

$$v(t) = M(w, i)\, i(t) \tag{2.17}$$

where w is an internal state variable, $i(t)$ is the current through the device, $v(t)$ is the voltage across the device, $M(w, i)$ is called the memristance, and t is time. Alternatively, the voltage-controlled memristor is defined by:

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$$\frac{dw}{dt} = f(w, v) \tag{2.18}$$

$$i(t) = G(w, v)\, v(t) \tag{2.19}$$

where $G(w, v)$ is called the memductance.

Due to the novelty of the device, the scientific community still finds itself coming to grips with its very notion. Researchers are divided over the range of devices that can be classified as memristors. Chua asserted that "all 2-terminal non-volatile memory devices based on resistance switching are memristors, regardless of the device material and physical operating mechanisms." [63]. Williams included PCM, magnetoresistive random-access memory (MRAM), and resistive random-access memory (RRAM) as memristor technologies [64].

The differentiation, if any, between memristors and memristive devices is also a matter of ongoing debate. In pertinent literature some publications define memristors as those devices having dw/dt (with w being the state variable) exhibit a linear relationship with current, as opposed to memristive devices, where dw/dt exhibits an exponential relationship with current [65]. In other publications [66], memristors are defined as passive two-port elements with variable resistance and memristive systems as an extension to memristors, where a current-controlled time-invariant memristive device is one that can be represented by Eqs. 2.16 - 2.17. In yet other publications, the terms memristor and memristive systems are used interchangeably to describe memristive devices [62].

Even further, Di Ventra et al. extended the notion of memristive systems to capacitive and inductive elements, namely, memcapacitors and meminductors. These elements typically show pinched hysteretic loops in the two constitutive variables that define them. Just as current-voltage comprise the constitutive variables for the memristor, charge-voltage and current-flux comprise the constitutive variables for the memcapacitor and the meminductor, respectively [67].

In an effort to resolve the disputes on nomenclature and classification, the memristor "fingerprint" was introduced by Chua [63], shedding some light on the mathematical relationships governing memristor functionality. Hence, the fingerprint of a memristor is a zero-pinched hysteresis loop in the I-V plane, as shown in Fig. 2.9. This must hold for all amplitudes and initial conditions of any periodic excitation waveform [68]. Additionally, it

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must hold for low frequencies. It can be shown that the hysteresis loop degenerates towards a single-valued function with higher driving frequencies [63], as seen in Fig. 2.9. This implies that, as the input frequency increases, the area of the hysteresis loops decreases and tends to a single-valued curve.

Hysteretic behavior is encountered in a variety of devices and forms. E.g. some devices exhibit non-crossing zero-pinched hysteresis loops. Non-crossing refers to the two loops having the same rotation and meeting, not crossing, at the origin. Other devices have a three-terminal configuration. Moreover, memcapacitive and meminductive devices also exhibit hysteretic behavior. Therefore, this thesis follows the classification whereby: a memristor is a device adhering to the strict aforementioned definition by Chua, whereas a memristive device is one that belongs to the broader class of devices exhibiting hysteretic behavior. Therefore, such devices, including three-terminal, non-crossing, etc., which, however, exhibit hysteretic behavior, are included in the memristive devices category. The former, category of memristor devices is a subset of the latter category of memristive devices.

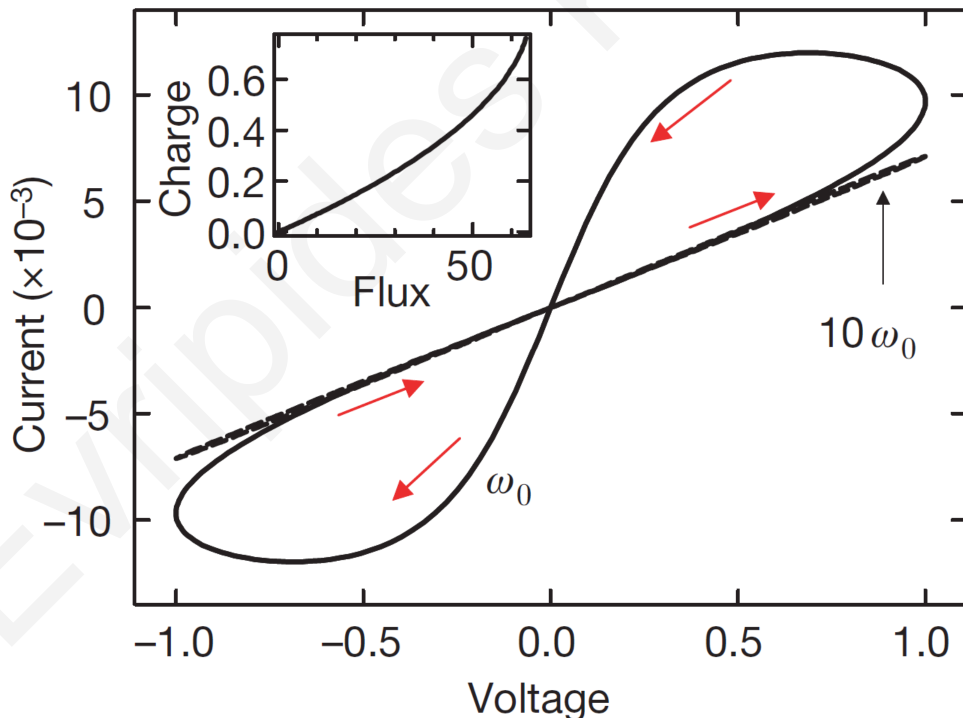

Figure 2.9: Characteristic behavior of memristor.

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Mathematically, the memristor is defined as a two-terminal electronic device characterized by a constitutive relation between the charge (q) and flux (φ) through the device [63]. q and φ are defined as the integral of current and voltage of the device, respectively:

$$q(t) = \int i(t)\, dt \tag{2.20}$$

$$\varphi(t) = \int v(t)\, dt \tag{2.21}$$

The device is differentiated between charge-controlled if the constitutive relation is defined as

$$\varphi = \hat{\varphi}(q) \tag{2.22}$$

or flux-controlled if the constitutive relation is defined as

$$q = \hat{q}(\varphi) \tag{2.23}$$

where $\hat{\varphi}(q)$ and $\hat{q}(\varphi)$ are continuous and piecewise-differentiable functions with bounded slopes.

Differentiating Eq. 2.21 and with respect to time, we obtain

$$v = \frac{d\varphi}{dt} = \frac{d\hat{\varphi}(q)}{dq}\frac{dq}{dt} = R(q)\, i \tag{2.24}$$

where

$$R(q) = \frac{d\hat{\varphi}(q)}{dq} \tag{2.25}$$

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is the memristance at q, and has the unit of Ohms (Ω).

Similarly, differentiating Eq. 2.20 with respect to time, we obtain

$$i = \frac{dq}{dt} = \frac{d\hat{q}(\varphi)}{d\varphi}\frac{d\varphi}{dt} = G(\varphi)\, v \tag{2.26}$$

where

$$G(\varphi) = \frac{d\hat{q}(\varphi)}{d\varphi} \tag{2.27}$$

is the memductance at φ, and has the unit of Siemens (S).

The implications of these equations are that the instantaneous memristance at any time t_0 is dependent on the history of $i(t)$ from $t = -\infty$ to $t = t_0$. Similarly, the instantaneous memductance at any time t_0 is dependent on the history of $v(t)$ from $t = -\infty$ to $t = t_0$.

Another implication is the zero-pinched hysteresis loop. The illustration of this is best elucidated through an example, as follows:

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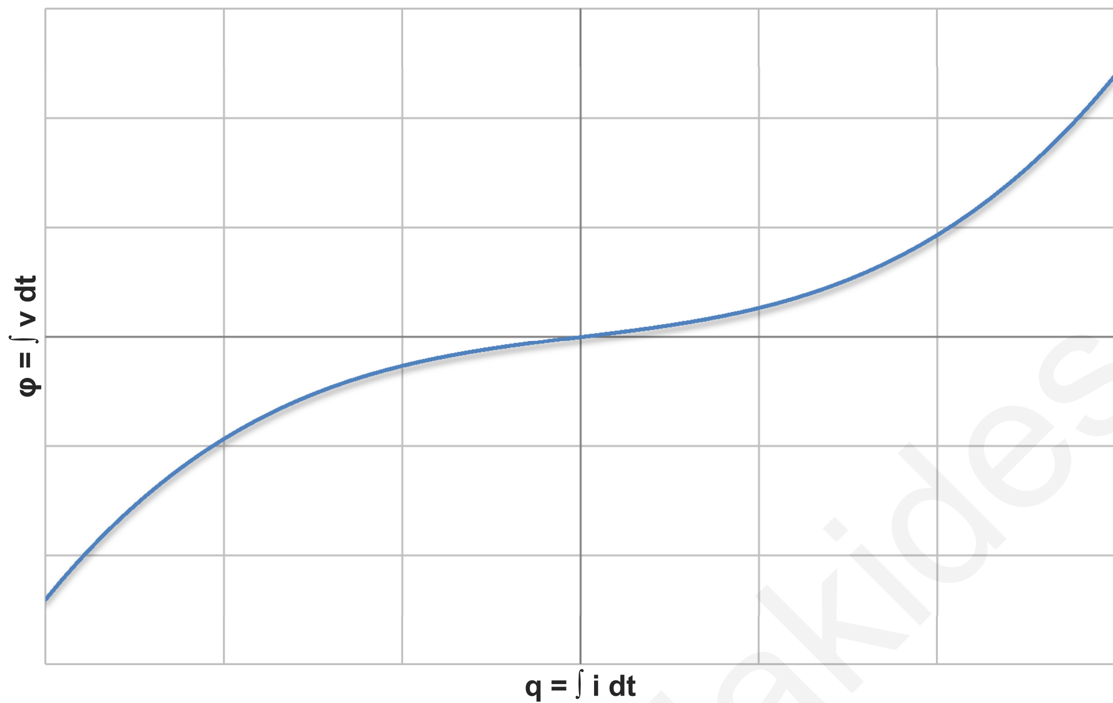

Figure 2.10: Graphical representation of $\varphi(q) = q + {}^{q^3}/_3$.

As per the aforementioned definition, memristor functionality is governed by a constitutive relation between charge and flux. The constitutive relation must be confined in the first and third quadrants. It should not be linear, since that would constitute a resistor - a degenerate case. A third-degree polynomial is one of the simplest possible expressions, yet at the same time a good approximation to physically plausible devices [63]. Hence, assuming the constitutive relation of an ideal memristor to be (Fig. 2.10):

$$\varphi(q) = q + \frac{q^3}{3} \tag{2.28}$$

and with $R(q)$ defined by Eq. 2.25 as

$$R(q) = \frac{d\varphi(q)}{dq} \tag{2.29}$$

then:

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$$R(q) = 1 + q^2 \tag{2.30}$$

Introducing a sinusoidal excitation to the system to reveal the bow-tie hysteresis curve:

$$i(t) = A\, sin(\omega t)\ A \tag{2.31}$$

then, the charge through the device is calculated through Eq. 2.20 as:

$$q(t) = \int_0^t i(t)\, d(t) = \int_0^t A\, sin(\omega t)\, d(t) = \frac{A}{\omega}\, [1 - cos(\omega t)] \tag{2.32}$$

Substituting this into Eq. 2.28, it follows that the flux through the device is

$$\varphi(t) = \frac{A}{\omega}\, [1 - cos(\omega t)] \left\{1 + \frac{1}{3}\, (\frac{A}{\omega})^2\, [1 - cos(\omega t)]^2\right\}. \tag{2.33}$$

According to Eq. 2.21, the voltage is obtained by differentiating the flux with respect to time:

$$v(t) = \frac{d\, \varphi(t)}{dt} = A\left\{1 + (\frac{A}{\omega})^2\, [1 - cos(\omega t)]^2\right\}\, sin(\omega t)\, V \tag{2.34}$$

Plotting $v(t)$ of Eq. 2.34 with respect to $i(t)$ of Eq. 2.31 we get the zero-pinched hysteresis loop (Fig. 2.11). The hysteresis occurs because the maxima and minima of the sinusoidal input current $i(t)$ do not occur at the same time as the corresponding memristor voltage $v(t)$. The zero pinching at the origin occurs because both $i(t)$ and $v(t)$ become zero at the same time.

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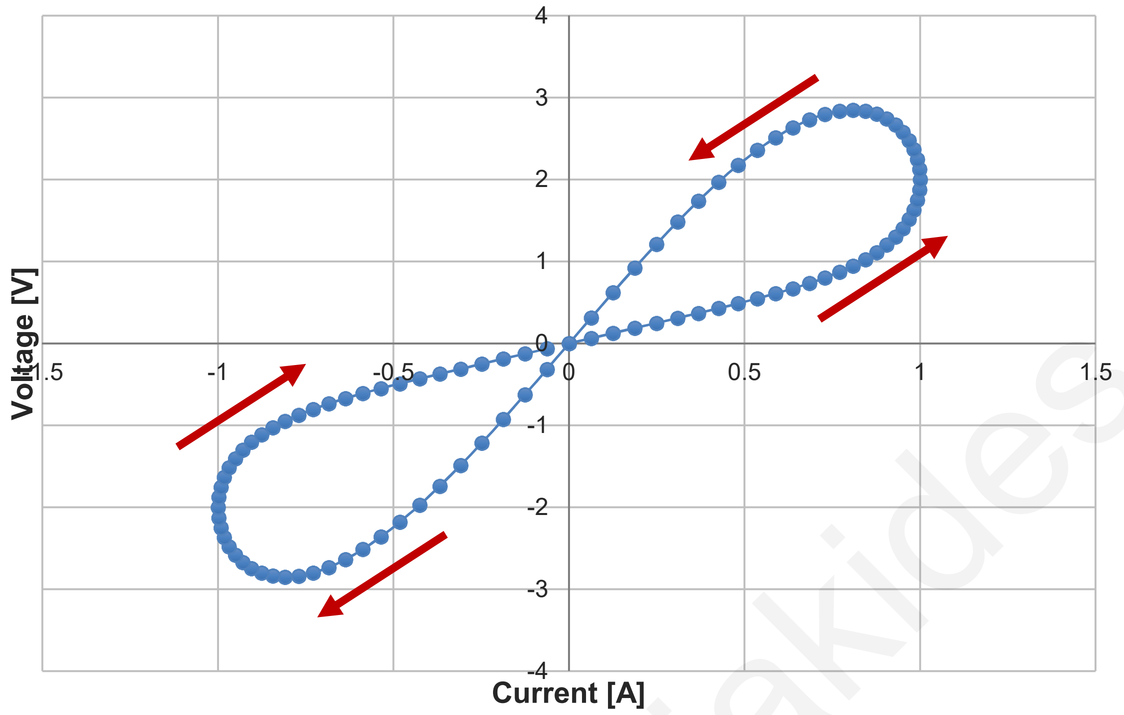

Figure 2.11: Pinched hysteresis loop of $(v(t), i(t))$ with $A = 1$ and $\omega = 2\pi$.

In a degenerate case, the bow-tie loop collapses to a single-valued function with increased driving frequency. This is illustrated by taking the limits of the derived functions as the angular frequency ω goes to infinity, to see that:

$$\lim_{\omega \to \infty} q(t) = 0 \tag{2.35}$$

and

$$\lim_{\omega \to \infty} \varphi(t) = 0. \tag{2.36}$$

Therefore, from Eq. 2.30 and Eq. 2.35:

$$\lim_{\omega \to \infty} R(q(t)) = R(0) = 1 + 0^2 = 1 \tag{2.37}$$

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and through Eq. 2.34:

$$\lim_{\omega \to \infty} v(t) = A\,(1+0)\,sin(\omega t) = A\,sin(\omega t)\;V, \tag{2.38}$$

i.e. the I-V hysteretic curve degenerates to a single-valued function. This is shown by plotting $v(t)$ of Eq. 2.38 with respect to $i(t)$ of Eq. 2.31 (Fig. 2.12).

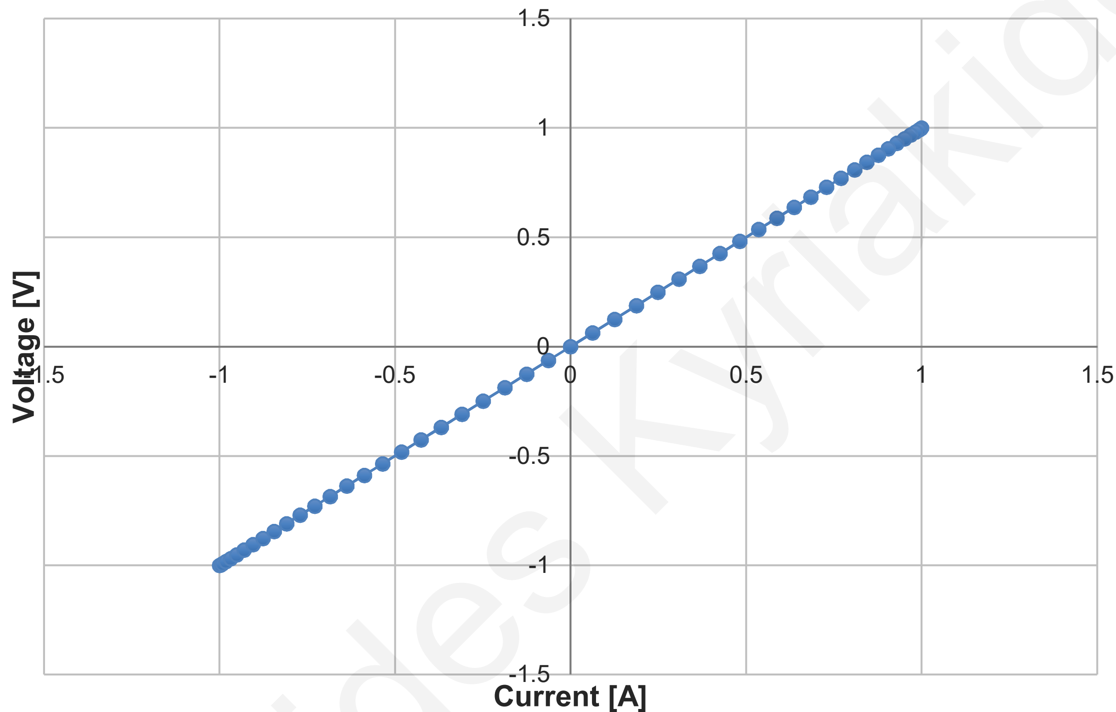

Figure 2.12: Degenerate case of hysteresis loop of $(v(t), i(t))$ with $A = 1$ and $\omega = 2\pi$.

To complete the treatment of the theoretical device, the ideal memristor definition defined by Eqs. 2.16 - 2.17 can be generalized to include additional state variables. Under such assumptions, Eq. 2.17 is re-written as the state-dependent Ohm's law:

$$v(t) = R(w, i)\; i(t) \tag{2.39}$$

and the state equation of Eq. 2.16 as:

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$$\frac{dw}{dt} = f(w, i) \quad (2.40)$$

where $R(\mathrm{w}, 0) \neq \infty$ and $w = (w_1, w_2, \dots, w_n)$ is a vector with n internal state variables $(w_1, w_2, \dots, w_n)$.

The equations above lead, through evaluation, to the qualitative description of memristors. A memristor is a two-terminal passive device, meaning it lacks any internal power sources. The device has a variable resistance which is associated with one or more internal variables. These variables represent the physical processes taking place in the device which are responsible for the change in resistance. The variable resistance manifests itself into a hysteresis loop in the I-V domain. This Lissajous figure exhibits certain traits. As shown above, it is zero-pinched, i.e. it passes through the origin of an I-V graph. With increasing driving frequency, the loop "shrinks," meaning the area within the loops in the first and third quadrants diminishes. Eventually, with high enough frequency, the double-valued function becomes a single-valued one. This is considered a degenerate case, where the memristor becomes a (possibly non-linear) resistor. There are a variety of physical processes responsible for a memristor's variable resistance. A review of these is presented in the next section.

2.3.3 State of the art in memristive structures

In 2008, while working on future non-volatile memory devices, researchers at HP Labs came across some unexpected behavior by one of their devices. While working in analyzing the behavior of a TiO_2-based device, they encountered a peculiar phenomenon; the structure's layers were different from those originally deposited. They inferred that the structure had changed during operation. This led them to deduce that ionic drift had taken place between the layers. Looking into the literature to find traces of this phenomenon it also became clear that this was a device belonging to the class of memristors, never before identified. The TiO_2-based device was in fact the first verified memristor.

The discovery by HP Labs caused a flurry of activity in the area. Various groups from diverse fields began publishing their findings with different devices that could be classified as memristors. Some of these have been novel devices while others were devices that had

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been fabricated and characterized ignoring their association with memristive behavior. Following, is a review of memristive devices that have been presented in the bibliography, either as memristors per se, or as devices that exhibit memristive behavior. The list is divided into groups depending on the devices' main trait, i.e. structure or operation mechanism.

Metal-insulator-metal devices feature a "sandwich" structure consisting of thin films. The top and bottom layers are metallic electrodes, whereas the intervening layer is, in the device virgin state, an insulator. Electromigration devices are based on the movement of ions under the influence of an electric field resulting in geometrical variations. Organic devices are based on organic thin films in their active region to vary their conductivity. Silicon-based structures are defined as those whose active region is consists of silicon in one of its forms, be it amorphous, doped, or otherwise. Insulator-metal transition devices rely on an initially insulating layer that is taken through a transition to display metallic traits. Finally, cation-migration-based devices rely on the diffusion of metal ions into a dielectric medium to vary conductivity.

2.3.3.1 Metal-insulator-metal

Pt/TiO_2/Pt

As reported earlier, the first memristor device developed at HP Labs has a Pt/TiO_2/Pt structure [69]. It consists of two metal layers and an intervening oxide bilayer. The platinum and titanium metal layers were deposited by electron-beam (e-beam) evaporation at room temperature. The TiO_2 films were fabricated either by sputter deposition or atomic layer deposition (ALD) methods. The TiO_2 layer used for the junctions was 50 nm thick and was deposited by sputtering from a TiO_2 target with 3 mTorr Ar and 250 °C substrate temperature. The TiO_2 (15 nm)/TiO_{2-x} (15 nm) bilayer films used for the junctions were synthesized by ALD at 200 °C with an additional in situ annealing in an N_2 environment at 300 °C. The annealing process was carried out following the first 15 nm deposition to create oxygen vacancies in the lower half of the TiO_2 film, or was carried out following the full 30 nm deposition to create oxygen vacancies in the upper half of the TiO_2 film.

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Titanium (IV) isopropoxide precursor was used with water as the oxidizing agent for the ALD TiO_2 films. The Ti (1.5 nm adhesion layer) + Pt (8 nm) electrode used for the 50 nm × 50 nm nanojunctions was patterned by ultraviolet-nanoimprint lithography. The Ti (5 nm adhesion layer) + Pt (15 nm) electrode used for the microjunctions (5 µm × 50 µm) was fabricated using a metal shadow mask. A single irreversible forming step was necessary for the as-prepared (virgin) devices before they exhibited repeatable switching cycles; for the nanodevices this forming occurred at approximately +8 V and 10 mA. The cross-point structure and the memristor fingerprint curve can be seen in Fig. 2.13.

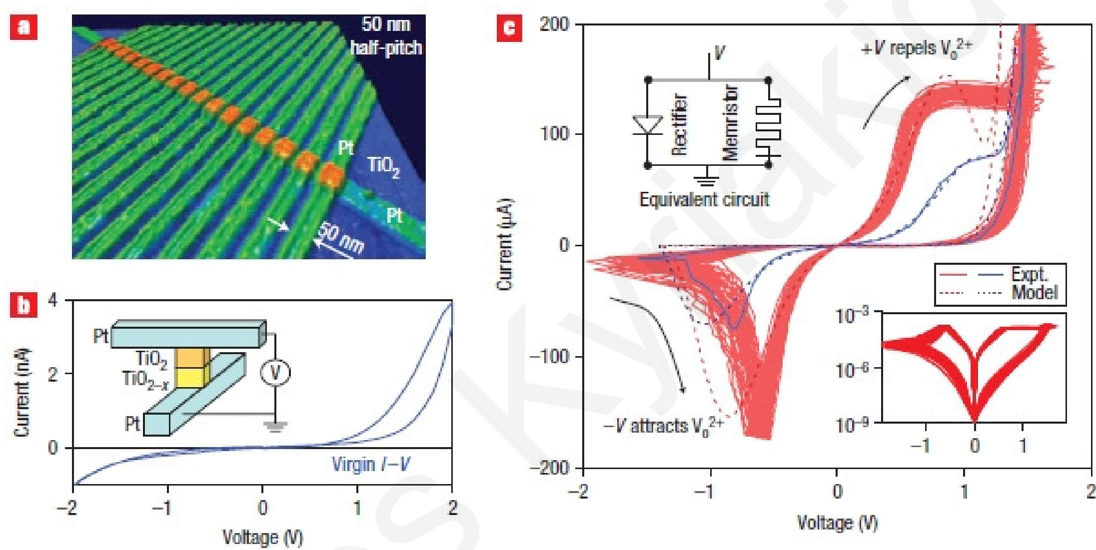

Figure 2.13: The TiO_2 memristor, showing (a) the cross-point structure, (b) the initial I-V curve of the device, and (c) experimental vs. modeled I-V curves.

The Pt/TiO_2/Pt is widely considered to be the benchmark for memristor devices, due to the fact that it was the first device to be defined as a memristor, as well as, its extensive characterization by HP and other groups.

A bulk process, namely migration of oxygen vacancies, was initially believed to be the mechanism responsible for the memristance effect. However, later published results point to a more filamentary-type effect, again involving oxygen vacancies. In order for the virgin devices to exhibit repeatable switching, an electro-forming step is required. This is a common procedure in memristor devices which will be investigated in depth in subsequent chapters.

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Similar results to the ones reported by HP were obtained by Prodromakis et al. [70] using a TiO_2/TiO_{2+x} bilayer. This structure differs from the one presented by HP Labs in replacing the oxygen-deficient TiO_{2-x} layer with an oxygen-abundant TiO_{2+x}. This work demonstrates that the electrical characteristics of the two devices are similar and that the device dimensions can be significantly larger whilst still giving memristance effects.

Al/a-TiO_2/Al

Although based on TiO_2, like the HP Labs devices, the Al/a-TiO_2/Al device [71] has aluminum contacts. As a result, it is mechanically flexible. Rather than using expensive methods and equipment for the deposition of the active TiO_2 layer of the device, a room-temperature deposition was performed through a spin-on sol gel process that required no annealing. This procedure consists of spinning a titanium isopropoxide solution on the flexible plastic substrate at approximately 33 Hz for 60 s, and then leaving the precursor in air for at least 1 h to hydrolyze and form a 60 nm-thick amorphous TiO_2 film. To electrically contact the active area, a simple two-terminal crossbar is formed by depositing the bottom contact (80 nm Al) on the substrate (approximately 2.5 cm × 2.5 cm square of HP color laserjet transparency C2934A) prior to spinning the precursor, and depositing the top contact (80 nm Al) after the precursor has hydrolyzed. The devices were fabricated by depositing the top and bottom metal contacts via thermal evaporation through a shadow mask; however, there is the potential to deposit contacts from solution to enable roll-to-roll or inkjet processing.

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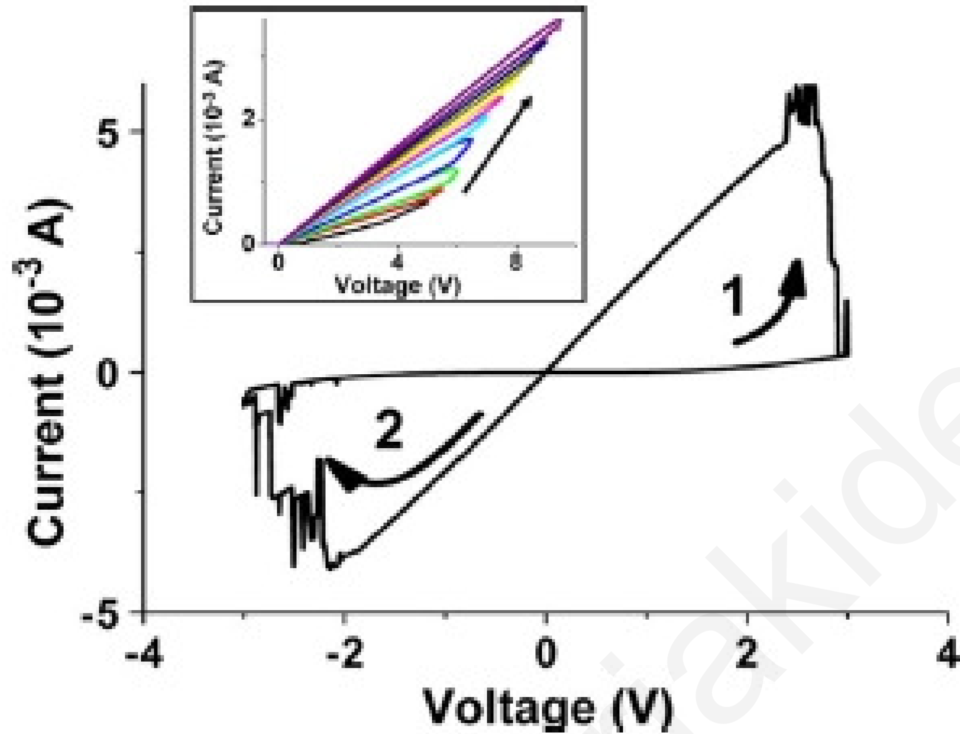

Figure 2.14: Current versus voltage for one switching cycle of the Al/a-TiO_2/Al device. The inset shows sweeps of the same bias polarity applied consecutively demonstrating a decrease in device resistance with each sweep.

The final Al/TiO_2/Al stack has an area of approximately 2 mm × 2 mm and clearly exhibits hysteresis and memory, as seen in Fig. 2.14. The most important aspect of this device, however, is its flexibility. Combining flexibility with low-cost manufacturing could prove a significant advantage in the future commercial appeal of memristive devices.

Ti/Gd_2O_3/Pt

The reported Ti/Gd_2O_3/Pt device [72] employs a bilayer technique for the bottom electrode. A bilayer metal Pt/Ti was deposited on SiO_2 layer as a bottom electrode by e-beam evaporation. Thin metal titanium was used to enhance the adhesion of platinum electrode on SiO_2 layer. A 250 Å-thick Gd_2O_3 (gadolinium oxide) thin film was then deposited on Pt/Ti/SiO_2/Si substrates at room temperature by pulsed laser deposition (PLD) with oxygen pressure of 0.01 Pa using a metal gadolinium target. The advantage of PLD is the stoichiometric transfer of complex target materials in a single-step process.

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Finally, the bilayer electrode Pt/Ti was deposited on Gd_2O_3 as the top electrode. A shadow mask with a diameter of 200 μm was used to define a contact pad for measurement, thus completing the fabrication process.

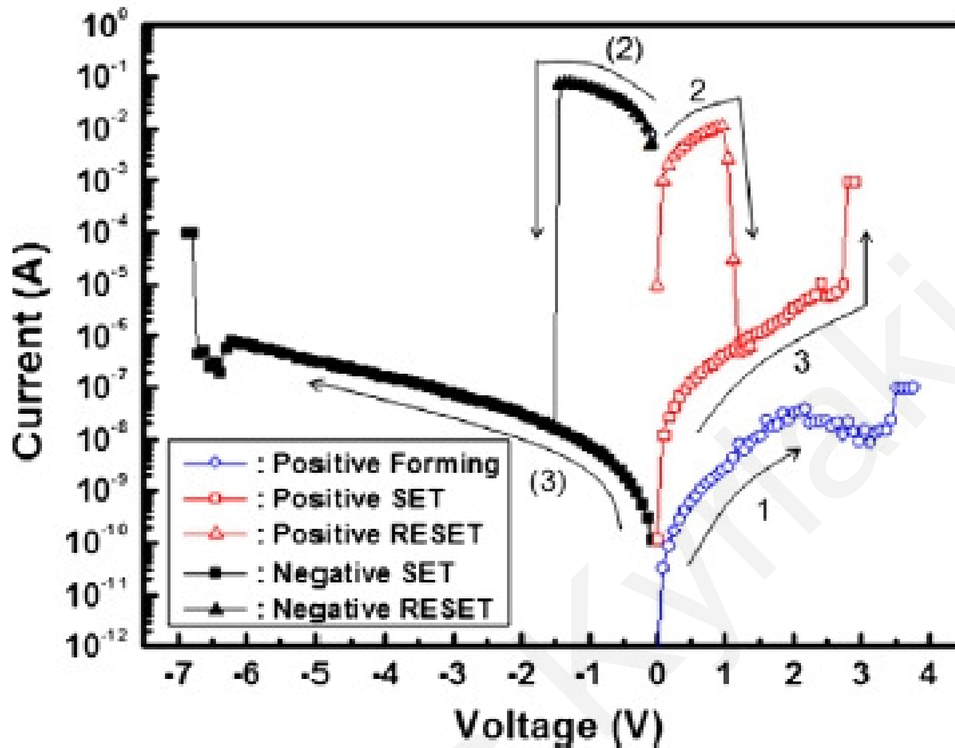

Figure 2.15: Typical unipolar I–V characteristics Ti/Gd_2O_3/Pt structures. Blue line represents the forming process. Red and black lines represent I–V characteristics under the positive and negative bias operation, respectively.

The Gd_2O_3-based device differentiates from previous implementations in its unipolar switching behavior, as seen in Fig. 2.15. The switching behavior is attributed to the formation and rupture of a filamentary path consisting of oxygen vacancies. The anode, which can be either the titanium or the platinum electrode, depending on voltage polarity, controls the migration of oxygen ions (O^{2-}) during switching, thereby explaining the discrepancy between the positive and negative "SET" values. This device has been shown to perform stable switching for 100 cycles.

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Pt/NiO/Pt

Devices based on NiO, despite apparent similarities with the original TiO_2-based devices, function in an entirely different manner. After electroforming, they give unipolar switching behavior, as seen in Fig. 2.16.

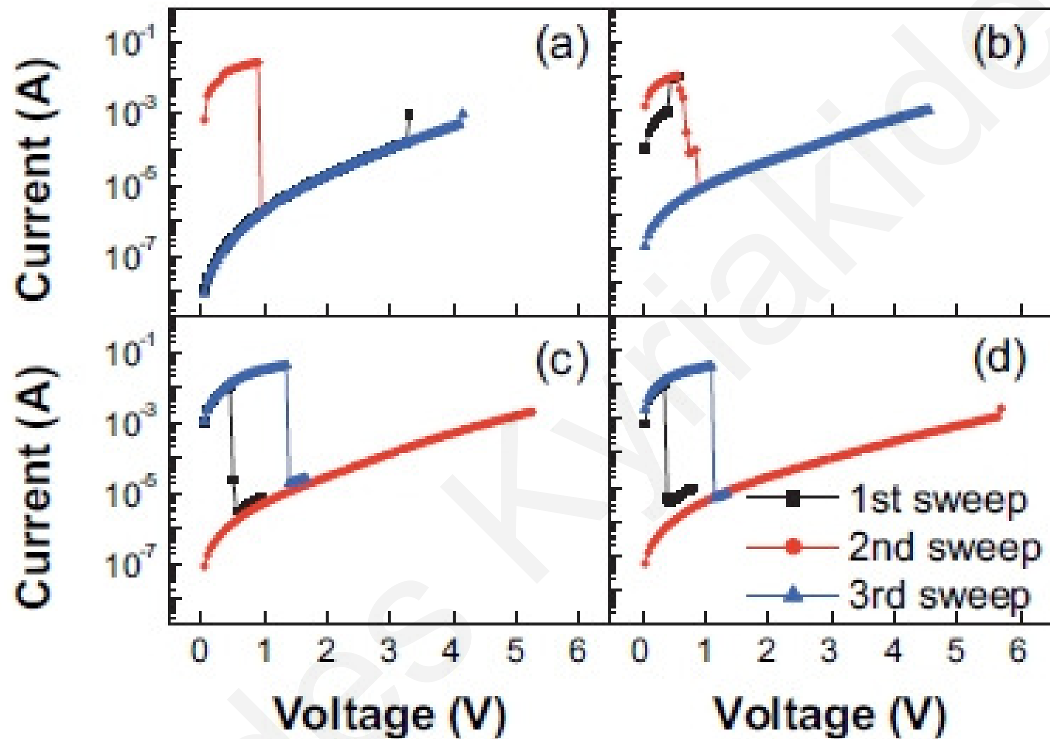

Figure 2.16: Conductive AFM measurements show three I-V curves of NiO devices (a) without forming, and with forming (b) once, (c) twice, and (d) four times.

Pt/NiO/Pt [54] devices are fabricated by DC reactive sputtering of a 50 nm-thick NiO polycrystalline thin film on $Pt/Ti/SiO_2/Si$ substrate. The base pressure in the chamber is maintained under 1×10^{-6} Torr using a turbo pump. During deposition, the substrate temperature and working pressure are kept at 500 °C and 5 mTorr, respectively. Subsequently, $30 \times 30\ \mu m^2$ patterns are fabricated by a conventional e-beam lithography technique. To measure electrical properties, 100 nm-thick platinum top electrodes are deposited by a DC magnetron sputtering method on the aforementioned patterns.

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The switching mechanism is attributed to filamentary paths located in the NiO layer. An electroforming step is utilized to transition the device from High Resistance State (HRS) to Low Resistance State (LRS), similar to most other resistance-switching devices. However, in this case, the electroforming step requires a voltage of around 15 V, which can be problematic. ICs currently use lower voltage sources, e.g. 3.3 V, meaning that if these devices are to be used with other CMOS components they would require a separate high voltage source and possibly a different fabrication process.

Ag/a-Ag_2S/Pt

Plain silver is used as the active layer in Ag/a-Ag_2S/Pt devices [68] to exploit the properties of Ag_2S, a mixed ionic/electronic conductor. Ag_2S films are grown on clean Si (100) substrates with a native oxide layer. First, a layer of platinum (100 nm thickness and 10×10 mm^2 surface area) is sputtered onto the substrate, followed by a layer of silver (240 nm thickness and 5×5 mm^2 surface area) which is sputtered using a shadow mask. After sputtering follows the synthesis of Ag_2S by sulfurization of the silver film. Sulfur powder (reagent grade powder purified by sublimation) is loaded into a quartz tube (18 mm internal diameter) and the sample is held at 10 cm vertical distance facing the sulfur powder. Once the sulfur and the sample are loaded, the tube is evacuated to a pressure of 1×10^{-6} mbar. The temperature in the tube is then increased to 523 K using a vertical furnace with a programmable temperature control. The tube is kept under static vacuum to create a sulfur atmosphere, while the temperature remains constant at 523 K for 1 h. After 1 h, the tube is evacuated but kept at 523 K to anneal the samples for one more hour. Finally, the sample is slowly cooled down to room temperature at the rate of 1 $K\cdot min^{-1}$.

The resulting bipolar behavior, involving movement of the Ag^+ ions, is shown in Fig. 2.16. This is attributed to a shift of the major conduction mechanism, from a Schottky diode at low bias voltages, to silver filaments at higher bias voltages. Further investigation into these devices should determine their switching speed and cycling endurance.

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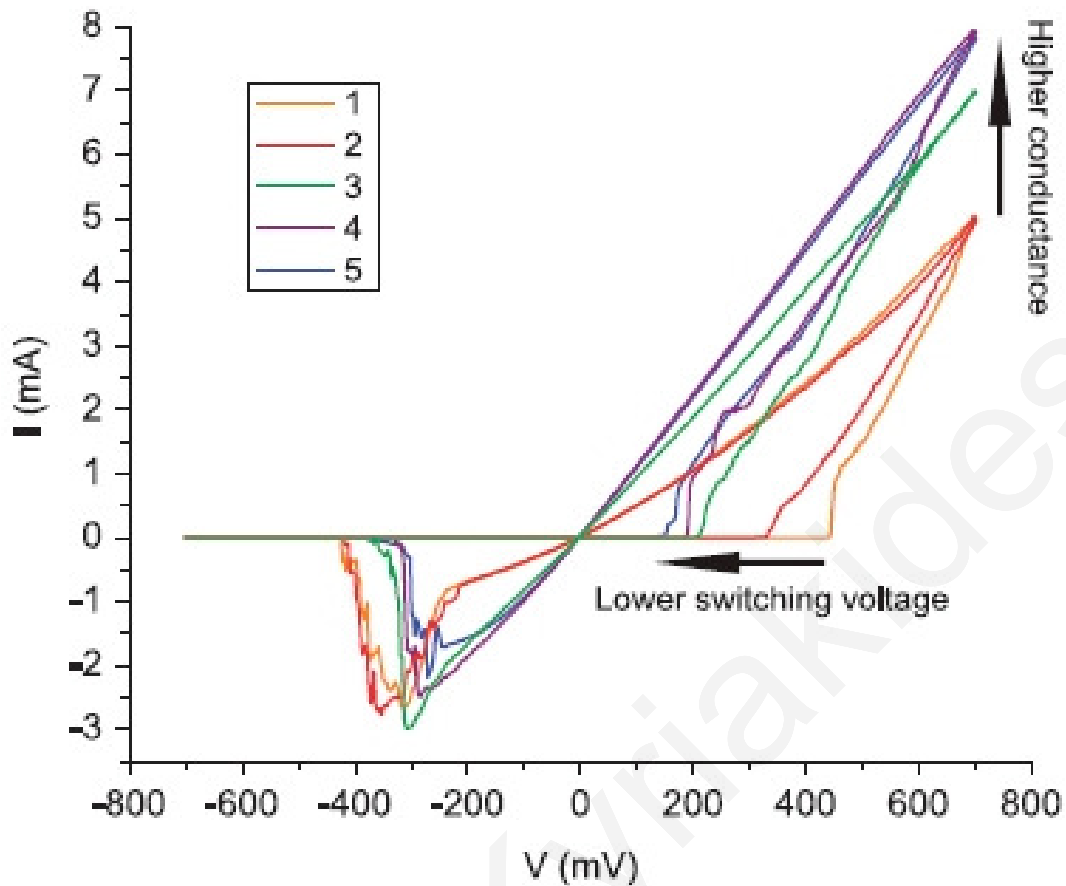

Figure 2.17: Multiple voltage sweeps reveal change in device switching voltage and conductance.

Au/Li_xCoO_2/Si

Au/Li_xCoO_2/Si structures [74] are included in the MIM category because the bottom electrode layer is highly doped (p++) silicon. The Li_xCoO_2 films were deposited on a (p++) doped silicon wafer by RF magnetron reactive sputtering. The procedure was performed using an Alcatel SCM 600 with a stoichiometric (x = 1) Li_xCioO_2 target at 500 W RF power. The films were grown in a 3/1 Ar/O_2 (2.2 Pa) atmosphere and a bias of –50 V was applied to the substrate. The films (100 nm, as determined by a profilometer) were subsequently heated to 600 ° C for 1 h in air in order to obtain the crystallized R-3m high-temperature Li_xCoO_2 phase. The corresponding stoichiometry was determined by atomic absorption spectroscopy and X-ray diffraction (XRD) experiments to be x = 0.9.

The top metal layer was obtained by the deposition of upper gold electrodes on the Li_xCoO_2 thin films by conventional Joule evaporation; rectangular pads of around 100 ×

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400 μm² were used to characterize the switching properties. I–V measurements were performed under vacuum (5×10^{-6} Torr) using a Keithley K487 instrument as both voltage source and current ammeter.

A typical I-V graph of the device is shown in Fig. 2.18. The switching behavior observed is attributed to a bulk process in the Li_xCoO_2 layer rather than a filamentary one, as attested by the lack of need of an initial electroforming step. Open questions remain with regards to the involvement of the two metal-oxide interfaces in the switching behavior.

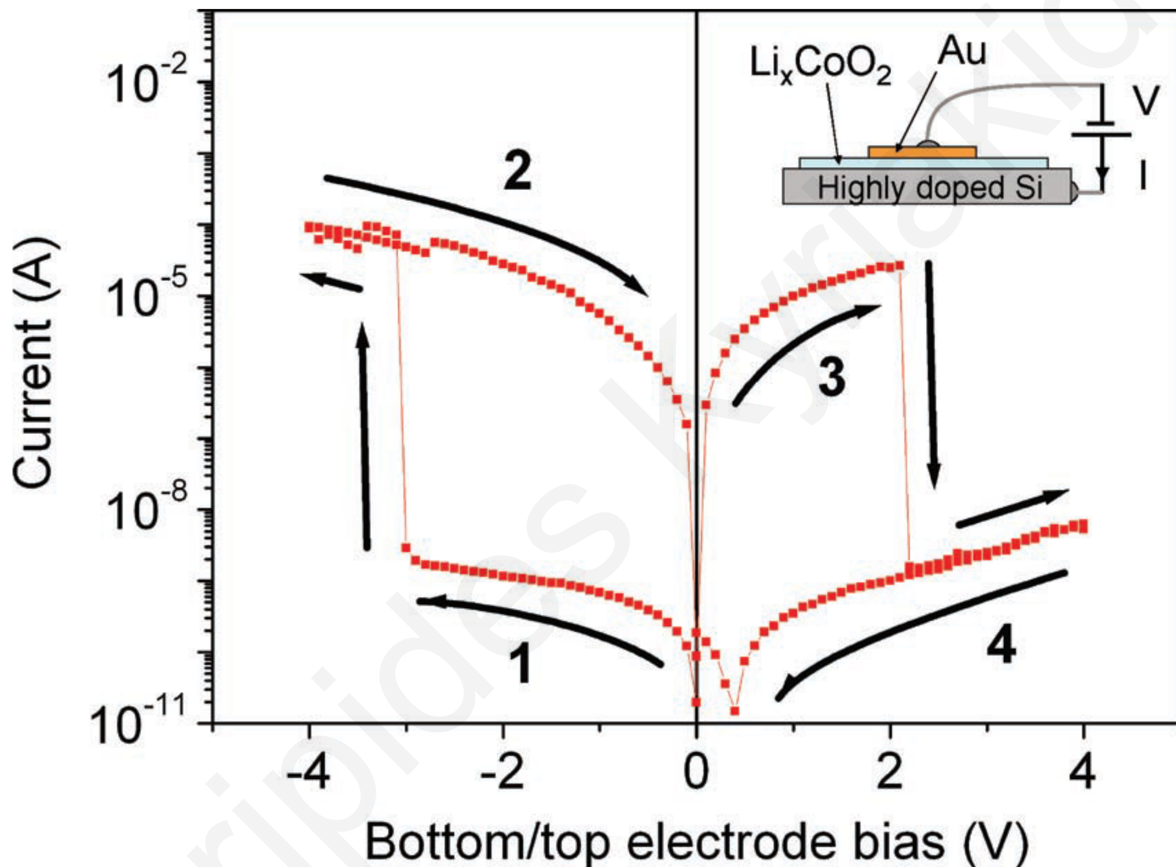

Figure 2.18: I–V characteristics of the Li_xCoO_2 device (structure shown in the upper left insert). The sweeping rate of the potential, between -4 V and +4 V, is 100 mV·s^{-1}. The rapid state transition occurs from the HRS to the LRS at about -3 V and from the LRS to the HRS at around +2.5 V.

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2.3.3.2 Single-element

Gold nanowires

S. L. Johnson et al. from the Department of Physics and Astronomy at the University of Kentucky utilized reversible electromigration to create single-metal memristors [56]. The devices consist of gold nanowires measuring 20 nm thick, ~100 nm wide ~300 nm long. The metallic wires were constructed without titanium or chromium adhesion layers making them truly single-component. Connection to the wires was made using two large gold leads.

The devices were fabricated using a Raith e_Line electron beam lithography (EBL) system. A bi-layer resist consisting of methyl-methacrylate/methacrylic-acid (MMA/MAA) copolymer and poly(methyl-methacrylate) (PMMA) was spun onto 300 nanometer-thick oxidized silicon substrates. The samples were then taken through EBL exposure, and subsequently developed in a mixture of 3:1 isopropanol:methyl-isobutyl-ketone (IPA:MIBK) for 60 s. They were then immediately placed in an electron-beam evaporation chamber for metal deposition. 20 nm of gold was evaporated and metal lift-off was performed in a bath of *N*-methyl-2-pyrrolidinone (NMP) held at 70 °C for approximately 1 h.

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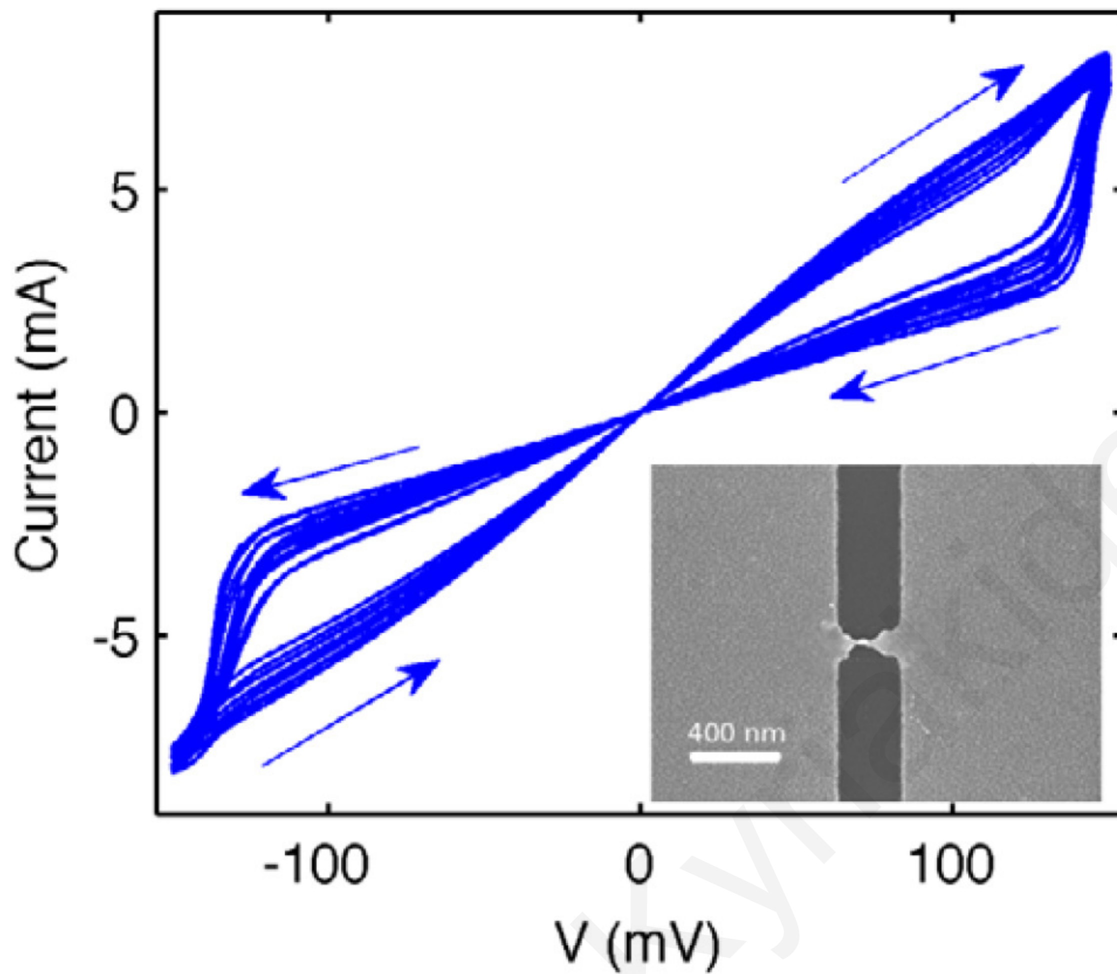

Figure 2.19: I–V curves of gold nanowires generated over 14 cycles. Inset: Corresponding nanowire.

The devices were characterized using voltage-clamp experiments to show zero-pinched bow-tie curves, as shown in Fig. 2.19. The memristance effect, attributed to the geometrical changes to the wire, is reproducible and the resistance is non-volatile in the absence of stimulation. However, the timescale for switching from a high to a low state is roughly 10 s. The timescale, though, can be shortened with the scaling of the device.

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2.3.3.3 Organic

Graphene

Graphene-based devices have also been proposed as memristive elements [70]. The design consists of two arrays of parallel wires arranged perpendicularly to each other with a graphene oxide (G-O) layer sandwiched in between. Each cross-point is a memristor.

To fabricate these devices, after depositing 50-micrometer-wide aluminum wires on a 6.5-square-centimeter piece of plastic, a solution is spun containing suspended G-O flakes onto the surface. This forms a thin film of overlapping G-O flakes over which the researchers deposit the top aluminum wire array. This results in 25 memristors, each 50 μm wide.

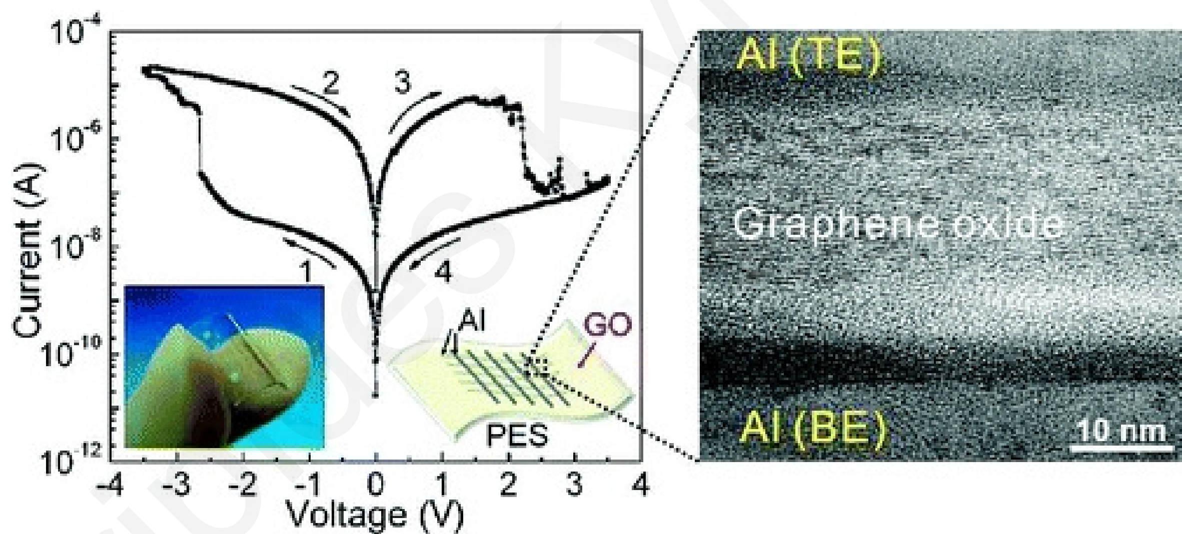

Figure 2.20: Left: Typical I-V curve of a Al/G-O/Al/PES device plotted on a semilogarithmic scale with the arrows indicating the voltage sweep direction. Right: TEM image of the device.

The device is initially OFF due to an insulating oxygen-abundant top layer in the graphene oxide (Fig. 2.20). The transition to the ON state occurs by the formation of local filaments in this layer due to oxygen ion diffusion induced by an external negative bias. The graphene-based devices exhibit a very high cycling lifetime and, although they cannot

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match other memristors' size, they are mechanically flexible and cheap to manufacture [75].

PEO/PANI

The working principle of the element seen in Fig. 2.21 is based on the dramatic variation of the electronic conductivity in a thin (50 nm) conducting polymer (polyaniline, PANI) multilayer in oxidized and reduced states. Such variation is induced and regulated by ionic flux into (and out of) the PANI multilayer at the junction with a film of a solid electrolyte (Li-doped polyethylene oxide, PEO) [20].

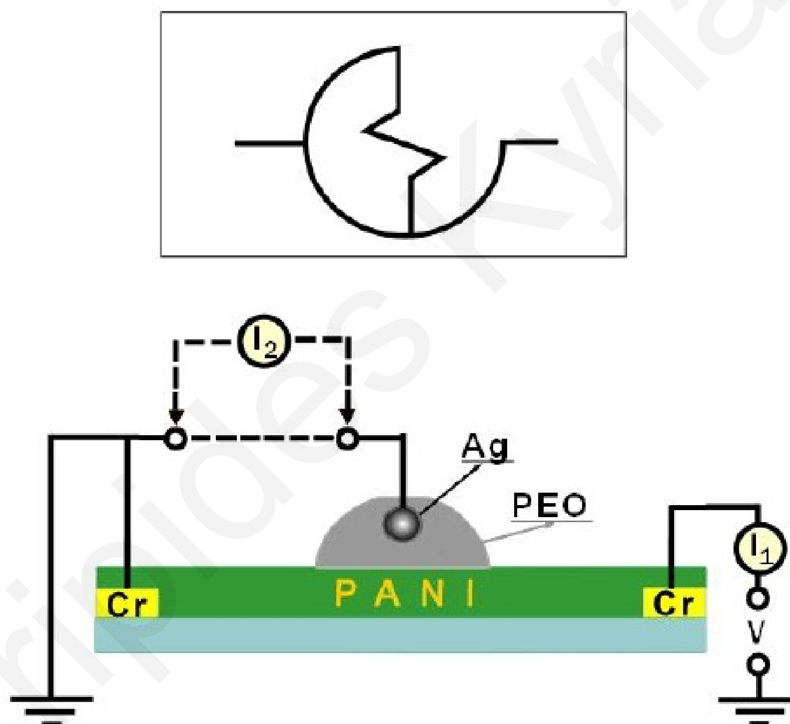

Figure 2.21: PEO/PANI electrochemical element structure (below) and its symbol (above).

The devices are made using an established routine: as a preliminary step, two chrome electrodes are evaporated at the sides of a 13 mm × 8 mm rectangular glass substrate. The glass is then cleaned with water and chloroform, and placed in a custom built sample holder, used for the deposition of the PANI layer.

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Langmuir films of PANI are spread in a KSV 5000 LB trough and deposited using a modified Langmuir–Schaefer (horizontal lift) technique. Water purified with a Milli-Rho-Milli-Q system is used as a subphase (resistivity 18.2 MΩ·cm). A single spreading allows the deposition of 24 to 28 monolayers of PANI over the glass substrate with the electrodes, using separation of the trough surface into independent sections by a special grid with size and shape of windows corresponding to that of glass substrate. Quality and homogeneity of the deposition were controlled with an optical microscope. The film is considered as a homogeneous one when visible impurities or defects are not observed. The whole deposition process is then repeated; the devices contain from 48 to 56 PANI layers, which provide both rather high conductivity and fast response to electrochemical changes.

The PANI film is successively doped by the treatment in 1.0 M HCl for about 1 min; to reduce the resistance between the electrodes from >200 MΩ to a value of about 1.2 - 1.8 MΩ. After 40 min the doping is repeated, in order to achieve a stable doped state. A PEO strip, about 1 - 2 mm wide, is cast across the PANI strip, approximately in the center between the two electrodes. A thin silver wire is placed over the PEO strip and then is again covered with doped PEO; a small indium patch was attached at one end of the wire to provide a stable electrical contact. The resulting hysteresis in the gate current with respect to the drain voltage is illustrated in Fig. 2.22.

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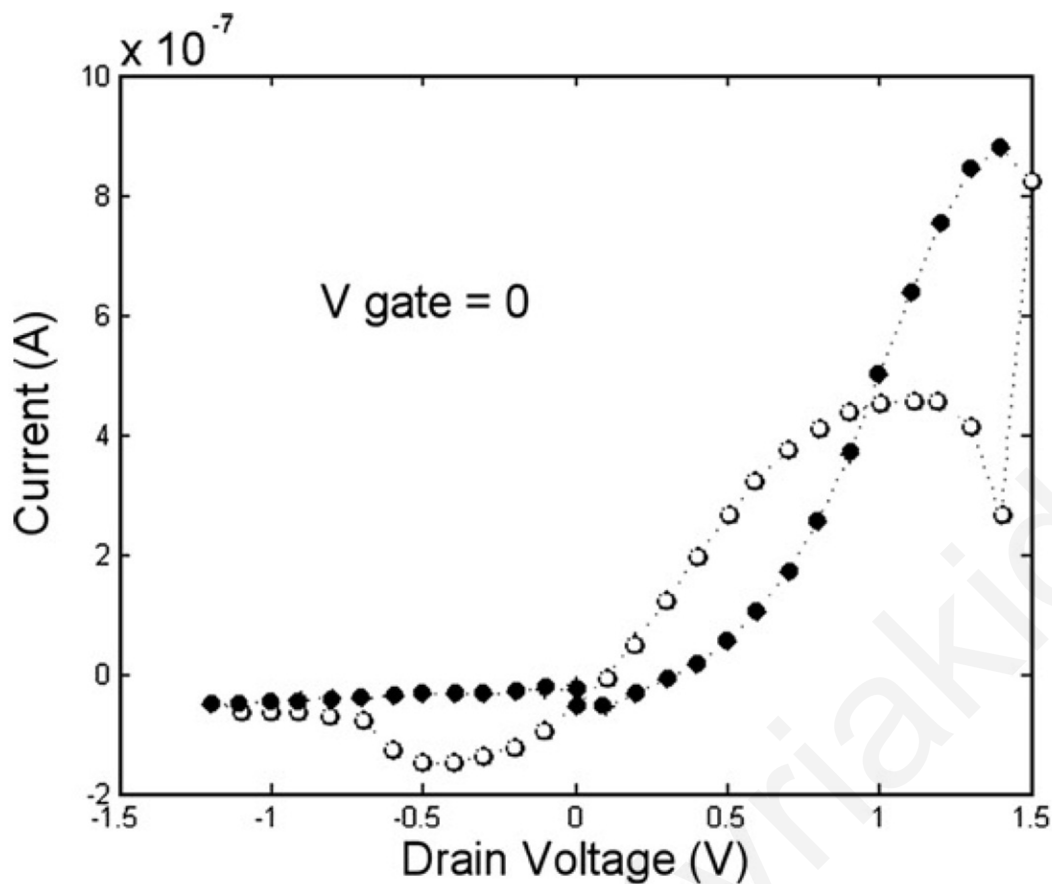

Figure 2.22: Hysteresis curve in gate current with respect to the drain voltage of PEO/PANI device.

As opposed to the devices reviewed so far, this is a three-terminal device. The working principle is based on the interaction between the adjacent PEO and PANI layers. When positive potential is applied to the middle (gate) electrode, Li^{+} ions in the PEO layer start flowing into the PANI layer. This oxidizes the PANI layer, transforming a zone between source and drain from insulating to conducting. A negative potential reverses the process, reducing the PANI layer and making the conducting zone insulating again. However, as with the gold nanowire electromigration-based device presented previously, the operation timescales appear to be very high. Substantial changes in conductivity appear in timescales of minutes, thus frequency of operation would be prohibitively low.

Ti/organic/Pt

The Ti/organic/Pt structure was first proposed by the HP Labs team, along with other collaborators, before identifying the TiO_2-based device as a memristor [19]. It consists of

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an organic monolayer between two metal electrodes. Two terminal metal/molecular-monolayer/metal planar junction devices were fabricated by sequential deposition of the bottom electrode, Langmuir-Blodgett (LB) monolayer, and top electrode on a flat insulating substrate to form 1 × 1 and 3 × 6 crossbar junction arrays. The substrates were polished <100> silicon wafers capped with 200 nm of thermal SiO_2. Bottom electrodes of 100 nm-thick platinum were formed by optical lithographic techniques. Scanning electron micrographs of the platinum electrode cross-section revealed sidewalls with a minor slope from vertical and a local tapered interface to the silicon oxide. Oxygen plasma cleaning of the platinum immediately prior to LB deposition generated a thin ~0.4 nm platinum oxide surface. The platinum surface roughness measured by atomic force microscopy was 0.4 nm RMS over a 1 μm^2 area. The static contact angle of water was 38 ° for the 200 nm thick thermal SiO_2 and 90 ° for the platinum electrode.

Three different LB monolayers were investigated: eicosanoic acid $C_{19}H_{39}COOH$ (Aldrich) deposited as the cadmium eicosanoate salt, an amphiphilic [2]rotaxane "R", which consists of a mechanically interlocked dumbbell component and ring component, and the dumbbell-only component of R, labeled "DB", which is identical to R except lacking the interlocked tetracationic cyclophane ring. Eicosanoic acid was chosen as a control molecule for all investigations because it forms well characterized, highly ordered LB films and is intrinsically an insulator.

During LB film deposition, the aqueous subphase was maintained at pH ~8.5 by the addition of tris(hydroxymethyl)aminomethane (TRIS) to typical concentrations of 10^{-4} M, at 21 °C. For the cadmium eicosanoate films, cadmium chloride was added to a concentration of 1 mM. Ellipsometric analysis of the cadmium eicosanoate, [2]rotaxane R, and dumbbell DB monolayers yielded average film thicknesses of 2.8, 3.5, and 3.3 nm, respectively.

The top electrode of 5 nm Ti + 200 nm Al was evaporated using e-beam evaporation through a shadow mask onto the LB film within 1 h after monolayer deposition. Previous investigation had shown that Ti deposited onto an organic monolayer reacts aggressively with the top organic functional groups to form titanium carbon complexes; this interfacial layer prevents subsequent titanium penetration through the monolayer. Crossbar devices were constructed with lateral wire widths of 1 - 10 μm Pt and 5 - 20 μm Ti/Al, yielding active junction areas of 5 - 200 μm^2 and thus 107 - 109 molecules electrically in parallel at each junction. DC bias sweeps of the fabricated device (Fig. 2.23) clearly show the ability of resistance tuning.

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These devices warrant further investigation, since the results were not proven robust across devices. This is the result of partial understanding of the mechanisms at play, with the authors suggesting differences between top and bottom electrodes, e.g. work function, or interface interaction between the monolayer and one of the electrodes, as possible explanations, among others.

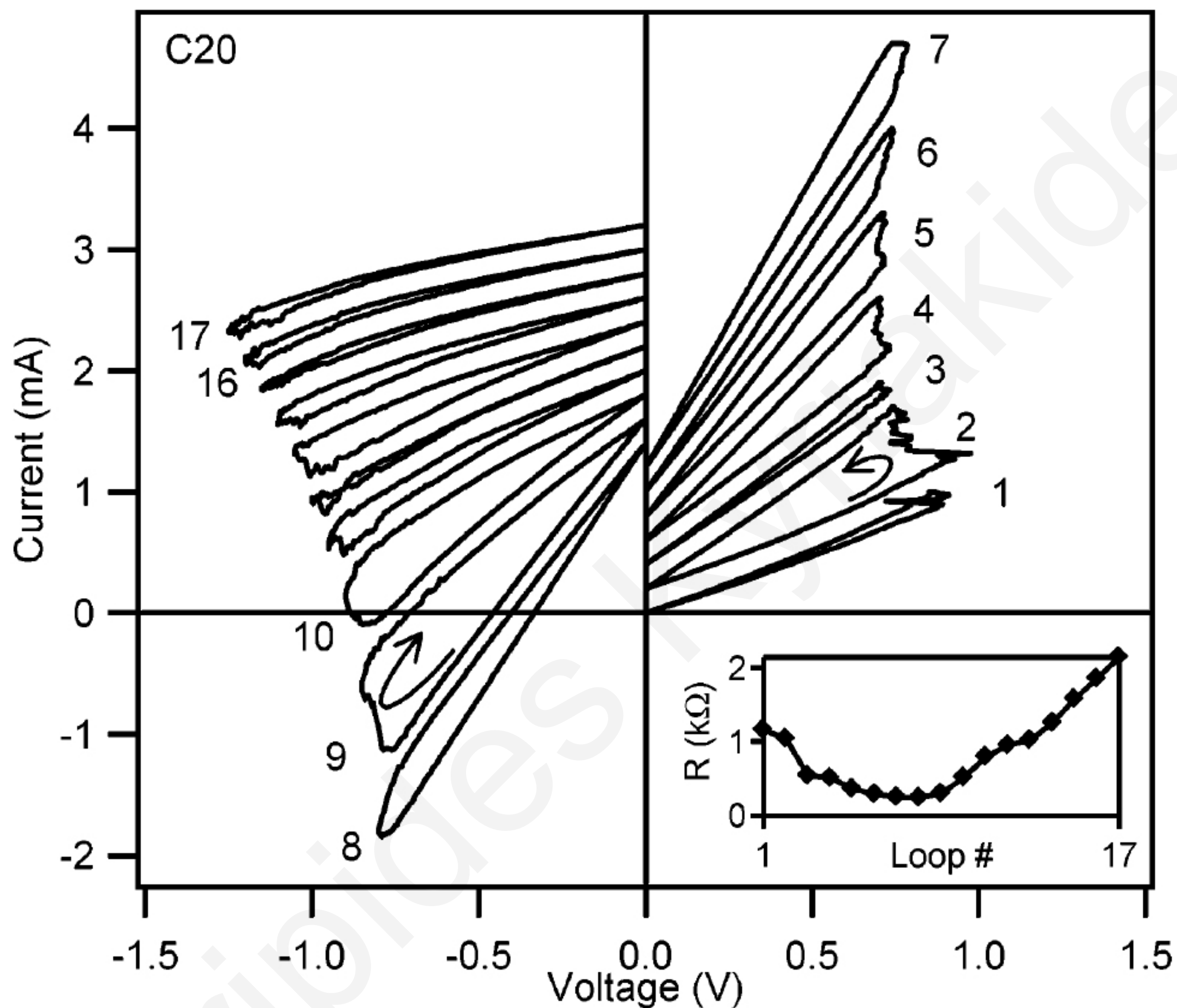

Figure 2.23: Continuous resistance tuning from 1.1 kΩ to 250 Ω and back to 2.1 kΩ. Successive curves achieved by applying positive DC current-bias sweeps, numbered 1 - 7, followed by negative DC voltage-bias sweeps, numbered 8 - 17. Successive curves are offset by +0.2 mA.

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2.3.3.4 Silicon-based

Poly-crystalline Silicon (Poly-Si) nanowires

Memristive effects have been shown in poly-Si nanowires [55]. In these structures the hysteresis is explained by charge trapping and detrapping at the SiO_2/poly-Si interface.

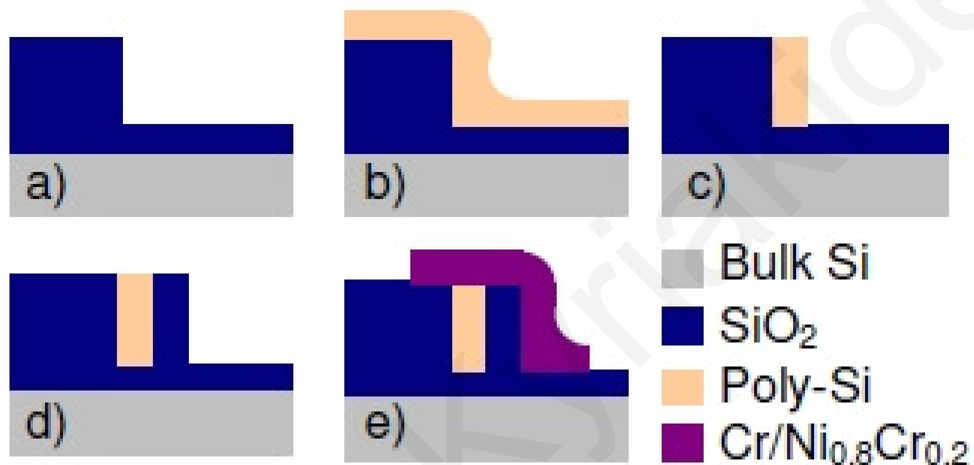

Figure 2.24: Fabrication steps of poly-Si nanowire Field-Effect Transistor (FET): (a) sacrificial layer etch, (b) poly-Si deposition, (c) RIE etch, (d) LTO spacer definition, and (e) metallization.

This process uses the spacer technique in order to define subphotolithographic dimensions by using standard photolithography and CMOS steps. The process flow, shown in Fig. 2.24, starts by defining a SiO_2 sacrificial layer on a silicon substrate (p-doped, 0.1 - 0.5 Ω·cm). Then, a thin conformal layer of poly-Si with a thickness ranging from 40 to 90 nm is deposited. Poly-Si is obtained by Low Pressure Chemical-Vapor-Deposition (LPCVD) of SiH_4 at 600 °C. This layer is then etched with Reactive Ion Etching (RIE), in order to remove the horizontal layer while keeping the sidewall as a spacer. The poly-Si spacer is densified at 700 °C for 45 min. A second Low Temperature Oxide (LTO) spacer is then defined next to the poly-Si in a similar way in order to isolate the first poly-Si spacer.

The LTO was deposited from the reaction of SiH_4 with O_2 at 425 °C. This LTO spacer is densified for 45 min in N_2 flow at 700 °C. The spacers are reminiscent of nanowires

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with thicknesses ranging between 20 and 60 nm. The contact regions of the undoped poly-Si nanowire were defined by the electron-beam evaporation of 10 nm chromium and 50 nm nichrome ($Ni_{0.8}Cr_{0.2}$) and lift-off. Chromium enhances the adhesion and thermal stability of nickel to oxidation during the subsequent 2-step annealing process (5 min at 200 °C, followed by 5 min at 400 °C). The substrate was used as a back-gate with a thick dry oxide as insulator (400 nm).

The resulting characterization yielded evident hysteresis in the I-V curve, as captured in Fig. 2.25. This is a three-terminal device and the hysteresis is evident when plotting I_{ds} vs. V_{gs}. Numerical simulations verify that the effect is a result of charge trapping and detrapping at the SiO_2/poly-Si interface. The difference rate at which charge trapping and detrapping occurs (detrapping is slower) explains the discrepancy between ascending/descending curves, as well as, left/right lobes. For better CMOS integration, these devices would have to be improved with respect to the voltage range necessary for them to exhibit hysteretic behavior.

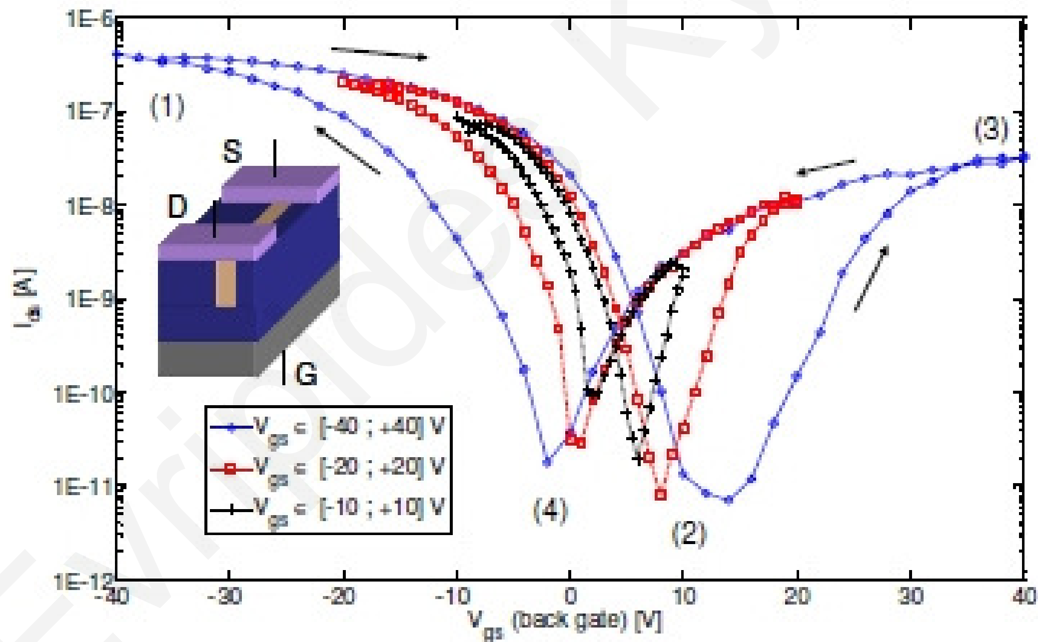

Figure 2.25: Variation of hysteresis of I_{ds}-V_{gs} at V_{ds} = 3.1 V.

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Gate-All-Around Silicon Nanowire FETs

Another implementation involves the use of a gate surrounding silicon nanowires [76]. Bulk-Si wafers with low boron concentration (NA ~ 10^{15} atoms·cm^{-3}) are used as a substrate for the fabricated devices. Vertical stacks of silicon nanowires are defined on the substrate by optical lithography without any constraint on the resolution limit (1 μm). The photoresist is then used as a mask for a Deep Reactive Ion Etching (DRIE). The optimized DRIE technique, which alternates plasma etching with passivation steps, defines scalloped trenches attached to silicon pillars with high reproducibility. The enhanced scalloping effect produces vertical modulation of the trench width. A sacrificial oxidation is then carried out with the double purpose of eliminating the silicon where the trench is thin, and also to reduce the surface roughness induced by the etching. A combination of chemical mechanical polishing (CMP) and buffered HF dip leaves vertically stacked nanowires suspended on a thick layer of insulating oxide. The gate oxide is grown in a horizontal furnace with a dry atmosphere. The gate poly-silicon is conformally deposited and doped with phosphorous by means of a diffusion process and then patterned with a combination of isotropic and anisotropic plasma etching steps. The fabrication of SBFETs requires the use of metallic source and drain contacts, meaning source-to-body and drain-to-body Schottky junctions. Cr/Ni bilayers (10 nm/50 nm) are patterned on top of the silicon pillars, partially covering the silicon nanowires at the anchor points. This leads to the silicidation of the nanowires channel from the Cr/Ni bilayer toward the gated region of the nanowire. The major fabrication steps are illustrated in Fig. 2.26, whereas the resulting hysteresis in the I-V curve is shown in Fig. 2.27.

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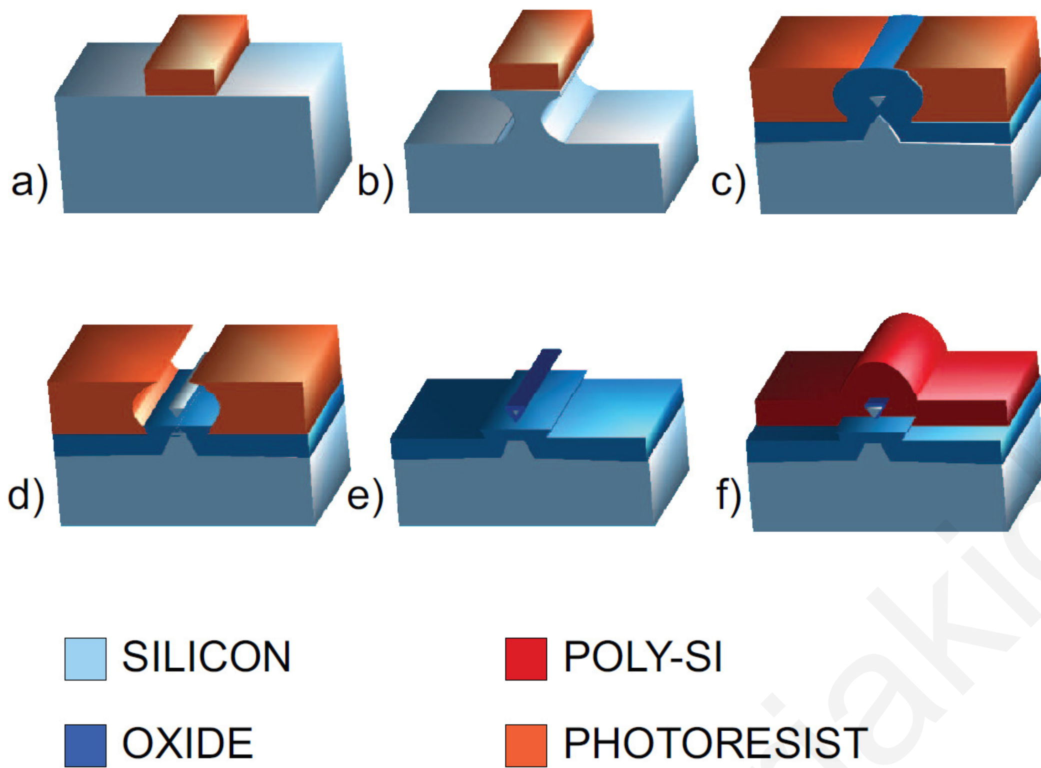

Figure 2.26: Fabrication steps of gate-all-around silicon nanowire FET: (a) A photoresist line determines the nanowire position. (b) DRIE etching forms a scalloped trench. (c) After wet oxidation, the silicon trench reduces to a suspended nanowire. The caves are filled with photoresist and planarized with CMP. (d) Buffered HF oxide etch releases the silicon nanowires. (e) Gate oxidation. (f) Poly-silicon is deposited and patterned to form the gate.

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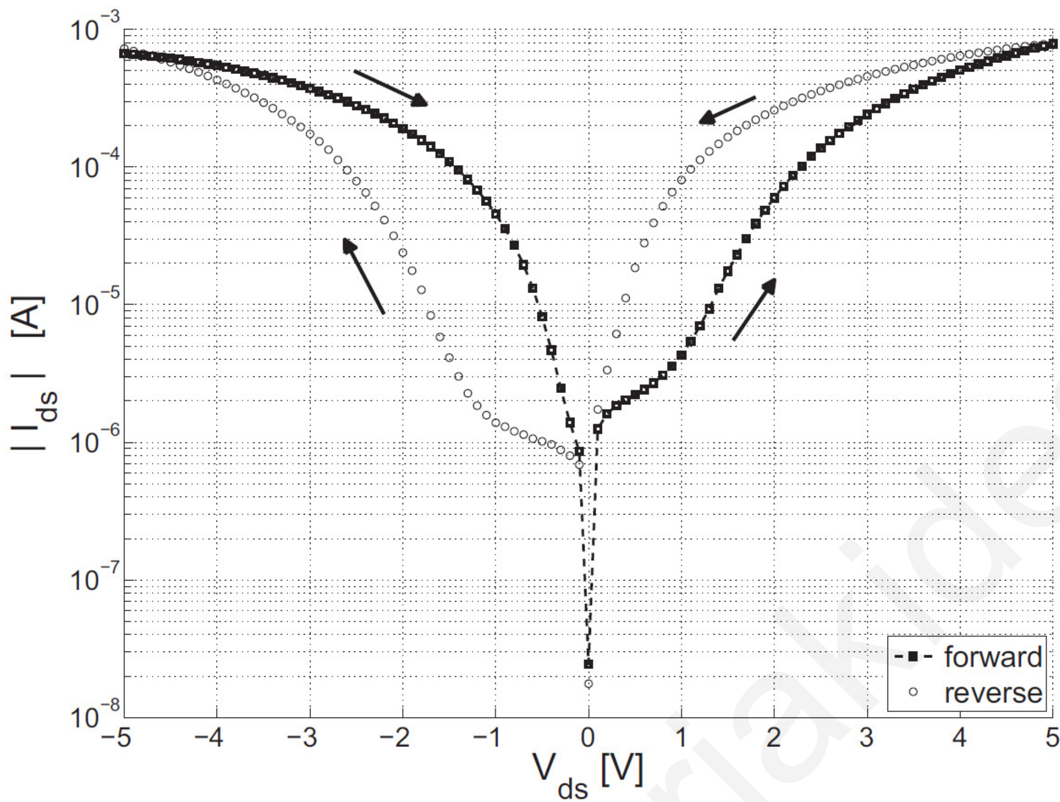

Figure 2.27: I_{ds}-V_{ds} characteristic showing the trapping/detrapping of charges at the metal/semiconductor junction. The device channel consists of 10 silicon nanowires in parallel.

It should be noted that these devices do not exhibit hysteresis in the I_{ds} vs. V_{gs} diagram. As shown in Fig. 2.27, the hysteresis occurs when plotting I_{ds} vs. V_{ds}. A large current is evident in this case - in the range of mA. This is attributed to the large parallel parasitic structure in the bulk. The hysteresis is traced to the presence of interface states in the metal/semiconductor interfaces of the device. Further electrical characterization of these devices should fully describe their behavior and test them with regards to frequency and repeatability.

Ag/a-Si/p-Si

The fabrication of Ag/a-Si/p-Si devices [21], such as those seen in Fig. 2.28, starts with the deposition of B-doped p-type Silicon (p-Si) and amorphous Silicon (a-Si) films on a Si/SiO_2 substrate. E-beam lithography and RIE are then carried out to form the bottom p-Si nanowire electrodes. The a-Si layer is etched along with the p-Si film during this process.

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To make Ohmic contacts to the p-Si nanowire electrodes, the a-Si layer at the end of each nanowire is etched, followed by platinum metal deposition. The device then goes through Spin-On Glass (SOG) coating, thermal curing and planarization processes. Ellipsometry is used to monitor the thickness of the SOG during the partial etch such that the thickness is controlled to ±10 Å. The silver top nanowire electrodes are patterned by e-beam lithography and lift-off. The contact pad patterns are fabricated by a photolithography process and configured to fit a custom made probe card. A final SOG coating and e-beam cure process are performed to passivate the silver nanowire electrodes.

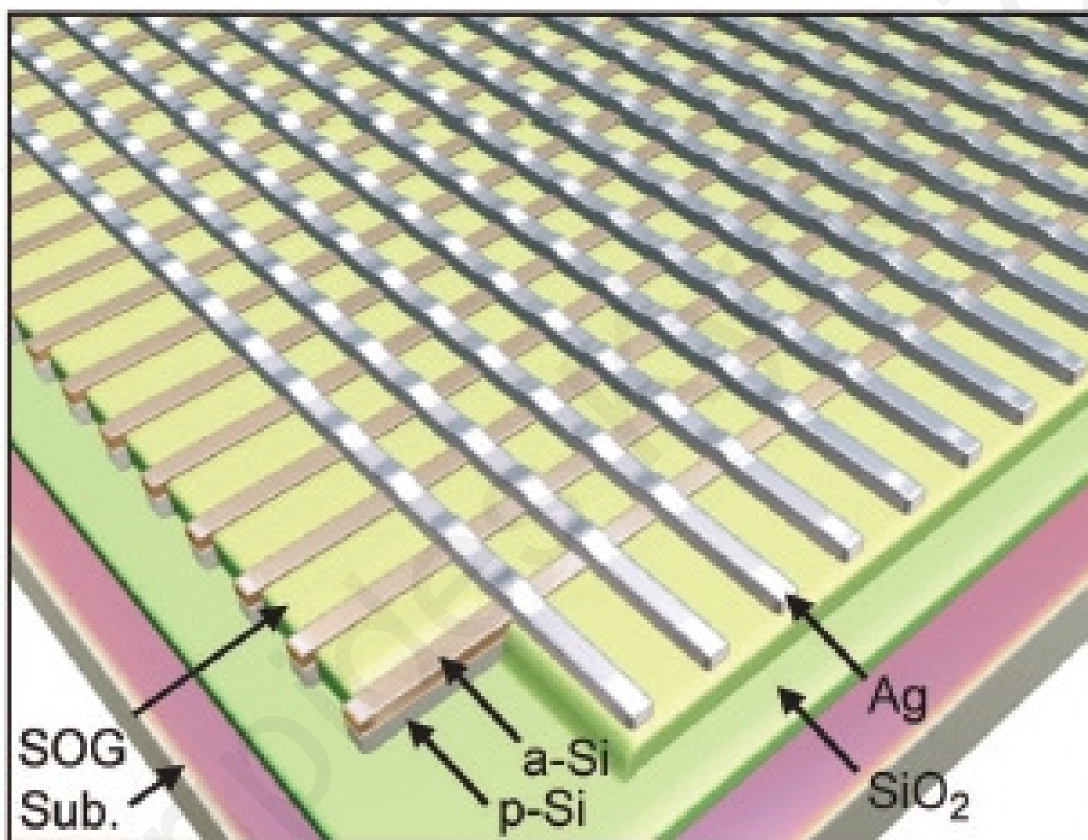

Figure 2.28: Crossbar array formed with Ag and p-Si nanowire electrodes and a-Si as the active layer.

The switching characteristics of the devices can be seen in Figs. 2.29 - 2.30. Fig. 2.29 depicts a typical Ag/a-Si/p-Si device. In Fig. 2.30 the forming cycle and a subsequent cycle are shown for a similar device, where the p-Si of the top electrode is replaced with nickel.

The characterization results point to evidence of filament formation in the a-Si layer consisting of silver atoms. The resistance during switching is thus defined by the resistance between the last silver atom in the filament and the bottom electrode. The Ag/a-Si/p-Si devices have been tested primarily as bipolar memory devices and in that respect show very good write speed, endurance, and retention.

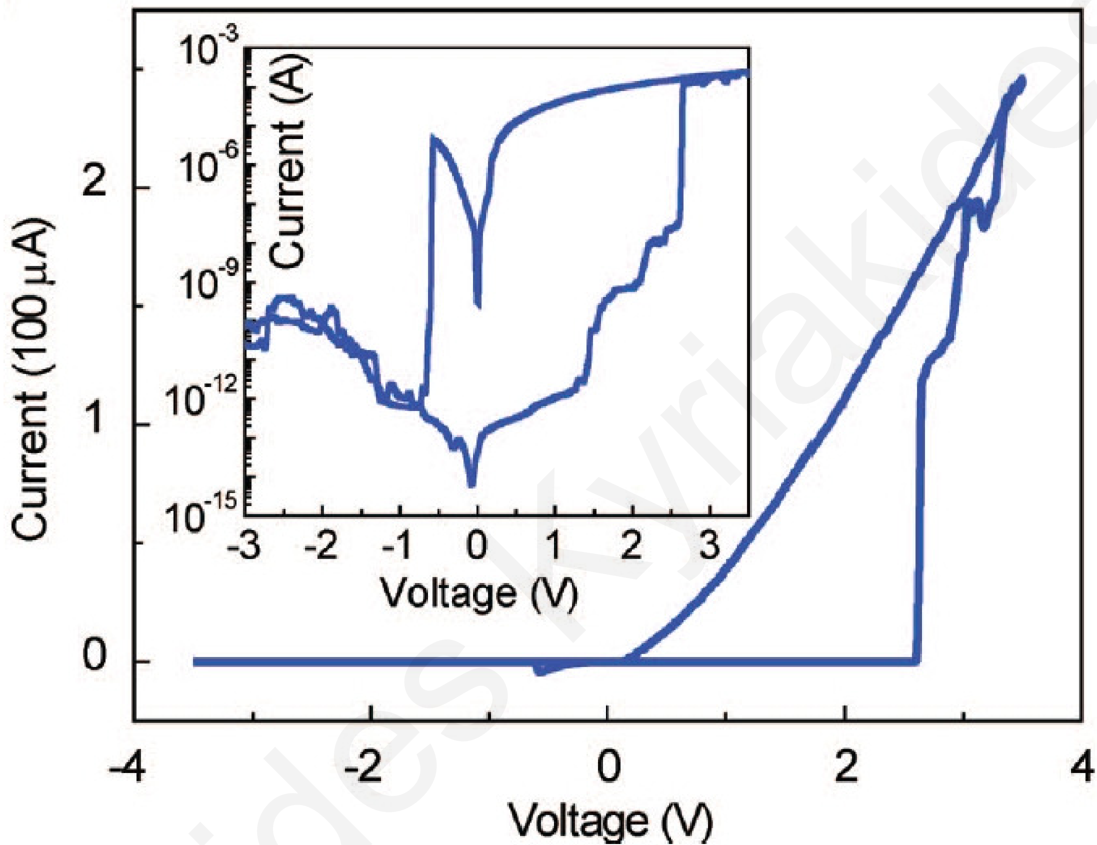

Figure 2.29: DC resistance switching characteristics for a typical Ag/a-Si/p-Si device with a 30 nm thick a-Si layer. Inset: The same I-V curve is plotted in semilogarithmic scale.

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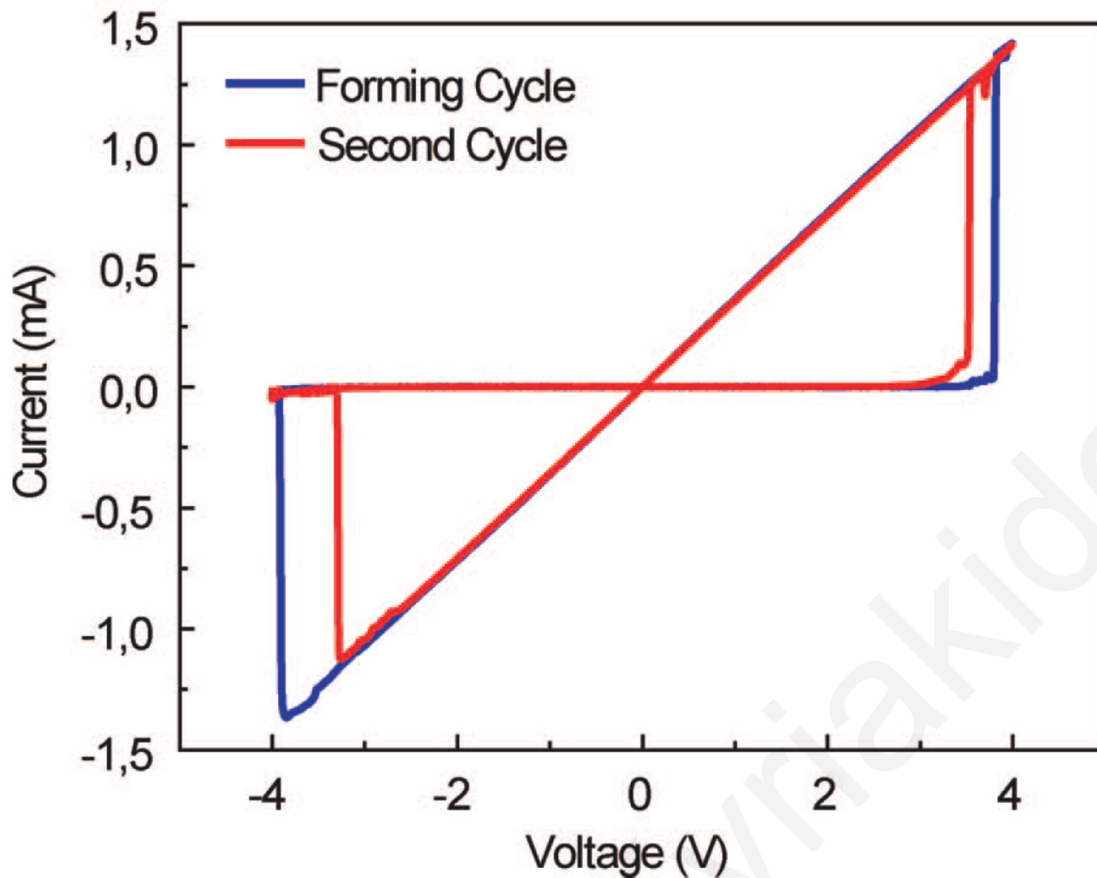

Figure 2.30: Resistance switching characteristics of a typical Ag/a-Si/Ni device.

2.3.3.5 Insulator-metal transition

$Pr_{1-x}Ca_xMnO_3$ (PCMO)

To investigate the resistive switching characteristics of the Au/PCMO/Pt sandwich structures [77], PCMO films were grown on Pt/Ti/SiO_2/Si (100) substrates by using PLD employing a KrF excimer laser with a wavelength of 248 nm. The target was synthesized by using a conventional solid-state reaction and its composition was $Pr_{0.7}Ca_{0.3}MnO_3$. The PCMO films were deposited at the substrate temperature ranging from 500 °C to 700 °C under oxygen pressure of 300 mTorr with constant laser energy density of 2 J·cm^{-2} and constant laser repetition rate of 5 Hz. The distance between target and substrate was fixed to 5 cm. Gold top electrodes with a diameter of ~200 μm were deposited on the PCMO

films by thermal evaporation under a base pressure of < 5×10^{-6} Torr with a dot-patterned metal shadow mask.

The oxygen-annealing effect on the resistive switching phenomenon of the PCMO film was investigated. For this, the PCMO films were deposited at a substrate temperature of 700 °C under oxygen pressure of 200 mTorr. After deposition, the films were in situ annealed at 500 °C for 1 h under oxygen pressure of ~200 Torr.

In this configuration, it is deduced that the resistance switching effect takes place at the Au/PCMO and PCMO/Pt interfaces. More specifically, it must involve manganese ions in the mixed valence state of Mn^{4+}/Mn^{3+}, pointing to a metal/PCMO interface effect. Results from the I-V characterization of these devices are shown in Fig. 2.31, however the switching mechanism remains unclear. Different explanations have been offered and various results have been reported [78]. Particularly, the role of the top electrode should be clarified, with some groups reporting near rectifying characteristics [79], most likely dominated by the Schottky diode. It should also be noted that an apparent feature of PCMO devices is the scaling of their resistance with device area [80].

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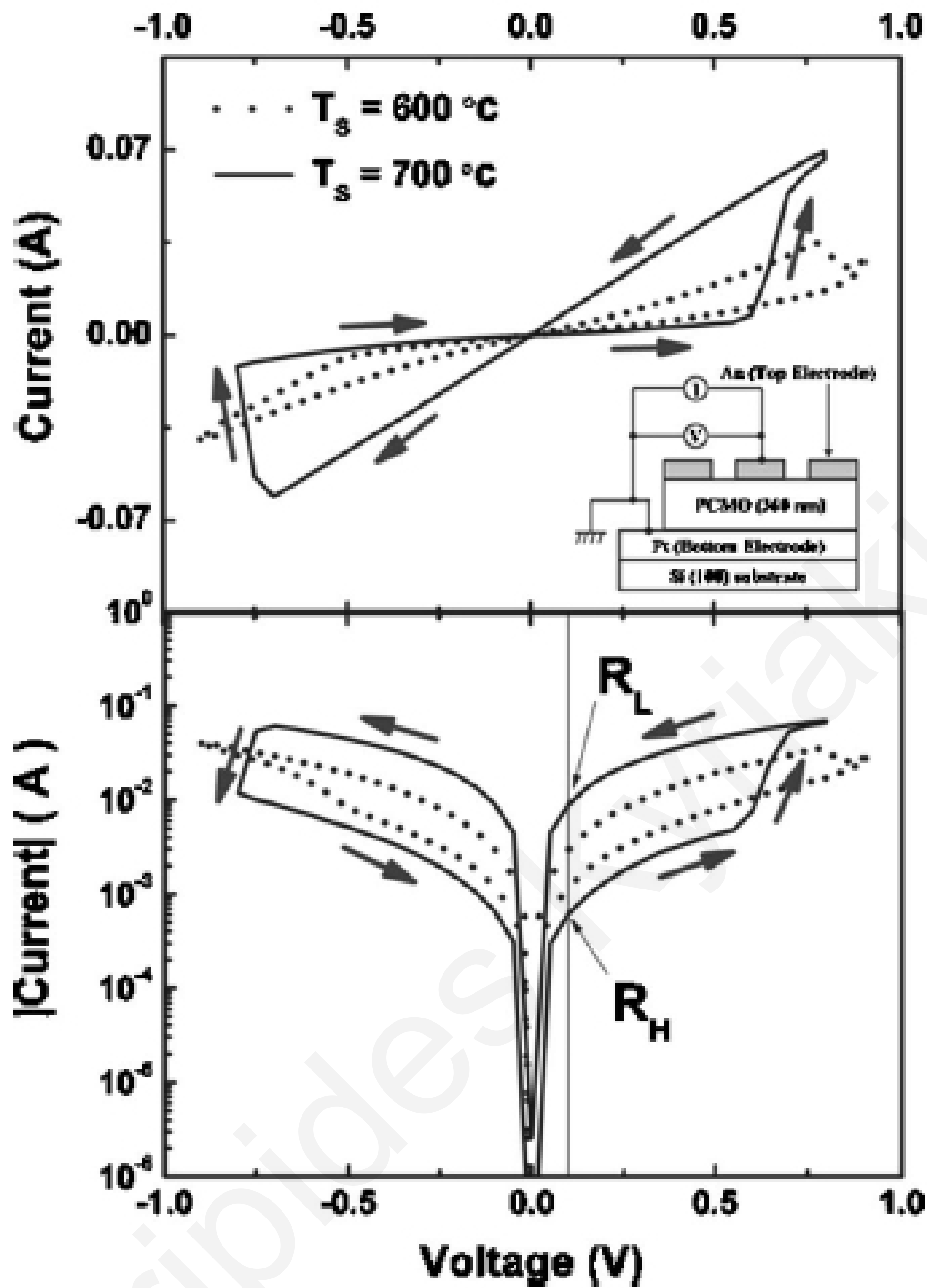

Figure 2.31: I-V characterization of Au/PCMO/Pt structures for two different substrate deposition temperatures. Top panel is drawn in linear scale and bottom panel in semilogarithmic scale. Inset panel shows schematic view of I-V measurement system.

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2.3.3.6 Transition metal oxide

$SrTiO_3$

$SrTiO_3$-based devices are amongst the most prominent transition metal oxide systems [81]. The thin film fabrication of these devices starts with conducting 0.5 wt% Nb-doped $SrTiO_3$ substrates. Epitaxial Fe-doped $SrTiO_3$ thin films are then grown on the substrates by PLD. The $SrTiO_3$ thin films have Fe-contents of 2% site-fraction and a thickness of 20 nm. The deposition parameters for the films were set to a laser fluence of 0.7 $J \cdot cm^{-2}$, a substrate temperature of 800 °C, an oxygen partial pressure of 0.1 mbar and a repetition rate of 5 Hz. Finally, a 25 nm-thick gold layer is sputter deposited and structured into 10 μm × 10 μm electrode pads by optical lithography.

Voltage sweeps reveal an initial forming step and subsequent hysteresis curves, as shown in Fig. 2.32. However the repeatability of these results appears insufficient. Moreover, the physical mechanism responsible, be it movement of ionic defects or strontium ions, remains unclear.

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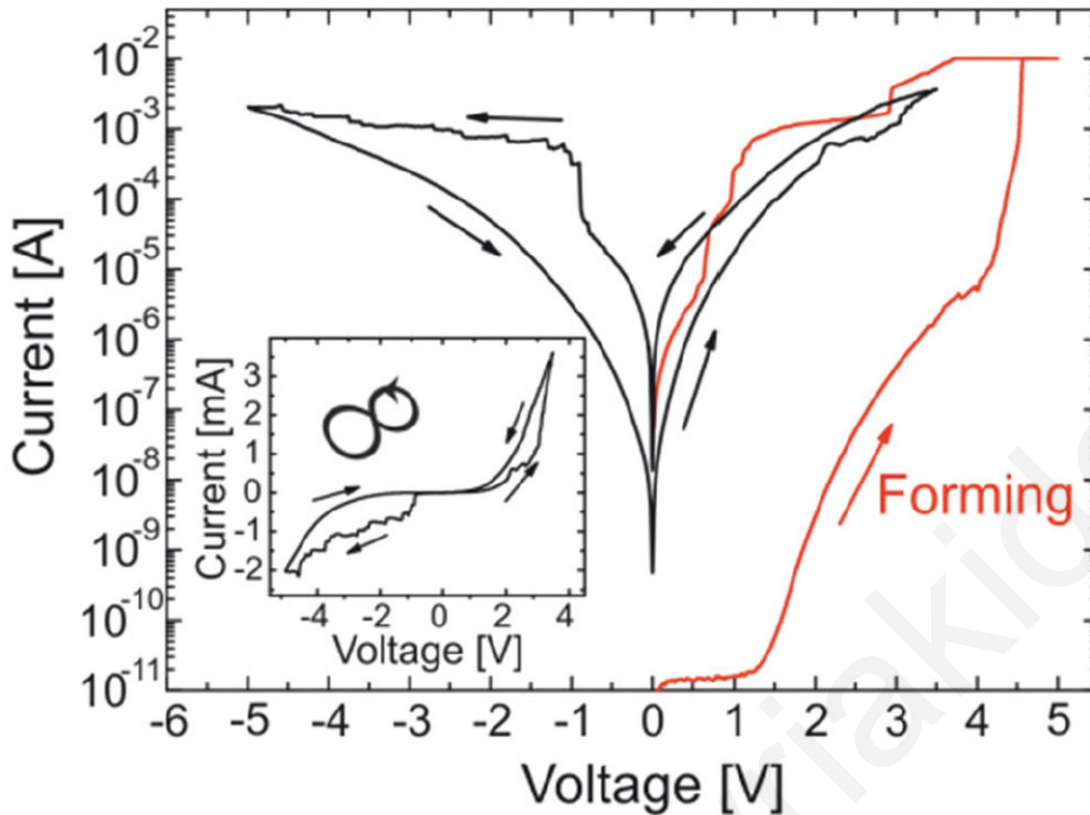

Figure 2.32: Semilogarithmic hysteresis loop of $SrTiO_3$ thin film device with initial forming indicated in red. Inset: Bow-tie loop apparent in linear scale.

2.3.3.7 Valence change memory

TiN/HfOx/TiN

In valence change memory cells, the operation involves a metal oxide insulator and mobile ionic defects (oxygen vacancies or cation interstitials) acting as donors [82]. Accumulation of these defects changes the local conduction by electron doping (valence change) in the metal sublattice. Oxygen deficiency can be induced by using oxygen-scavenging metal cap layers (e.g. Ti, Ta or Hf). It can also be generated by an initial electroforming step, creating an oxygen-deficient filament. Valence change memory cells switch in a filamentary mode under bipolar operation. SET and RESET are controlled by a combination of drift of the ionic defects and redox reactions at the electrode interfaces. The fabrication of TiN/Hf/HfO_2/TiN cells can be directly integrated in a CMOS process [83].

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The SET/RESET operation of a $TiN/HfO_x/TiN$ cell is shown in Fig. 2.33. For the SET process, an external current compliance has to be used to limit the filament growth, thus controlling the set resistance. HfO_x-based valence change memory suffer from inherent filament instability issues that can limit repeatability.

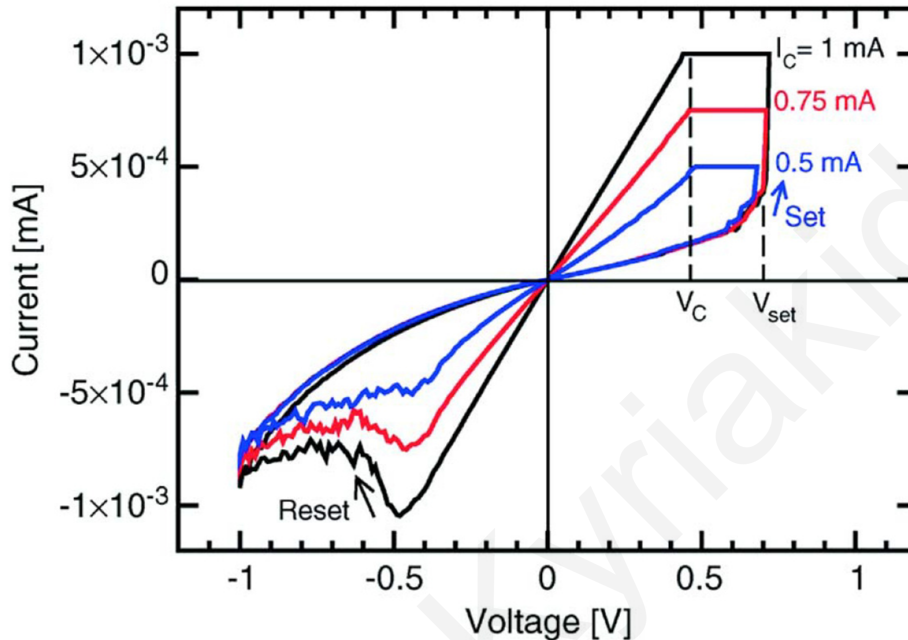

Figure 2.33: Filamentary bipolar switching of a $TiN/HfO_x/TiN$ structure. SET and RESET operations are reported for different compliance current values, denoted by I_C.

2.3.3.8 Cation-migration-based

Au/Cu_2S/Cu

Au/Cu_2S/Cu devices [85] feature a top layer of Au/Pt/Ti acting as an electrode, which electrically contacts with the Cu_2S/Cu film through a hole in the insulating layer. The fabrication sequence begins with a 120 nm-thick copper film on SiO_2/Si, which is sulfidized using anodic polarization. The copper film is immersed into a 0.025 M Na_2S solution. A positive voltage is biased to the film while grounding the immersed gold electrode. As the voltage is biased, sulfide ions are absorbed on the surface of the film, and then the surface is sulfidized electrochemically. The ionic current between two electrodes

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can be monitored during the polarization. Molar ratio between copper and sulfur in the sufidized film is estimated to be 2:1 using Rutherford backscattering. At room temperature, copper sulfide can form five stable phases: covellite CuS, anilite $Cu_{1.75}S$, digenite $Cu_{1.8}S$, djurleite $Cu_{1.95}S$, and chalcocite Cu_2S. It is deduce that the phase of the fabricated film is a chalcocite Cu_2S, which is a copper-ionic conductor and also a p-type semiconductor. After sulfidization, an insulating layer with a hole is made from a chloromethylated calixarene film, which is an electron beam (EB) negative resist, using EB lithography. The diameter of the hole ranges from 0.03 to 0.3 μm. The hole defines the contact area of the Cu_2S film with the top electrode. Finally, the top electrode of the Au/Pt/Ti is formed.

This device shows average switching repeatability with an average of 3×10^3 cycles before failure. Evidence points to filamentary conduction due to copper ion migration in the Cu_2S film, with switching characteristics shown in Fig. 2.34. The switching time to the ON state is 100 μs and depends on the pulse amplitude. However, the dwell time to the OFF state is very long. After applying constant positive voltage while the device is in the OFF state, the state switching occurs at best after 2.5 s. Changing the dimensions of the structure and voltage levels could help mitigate the issue.

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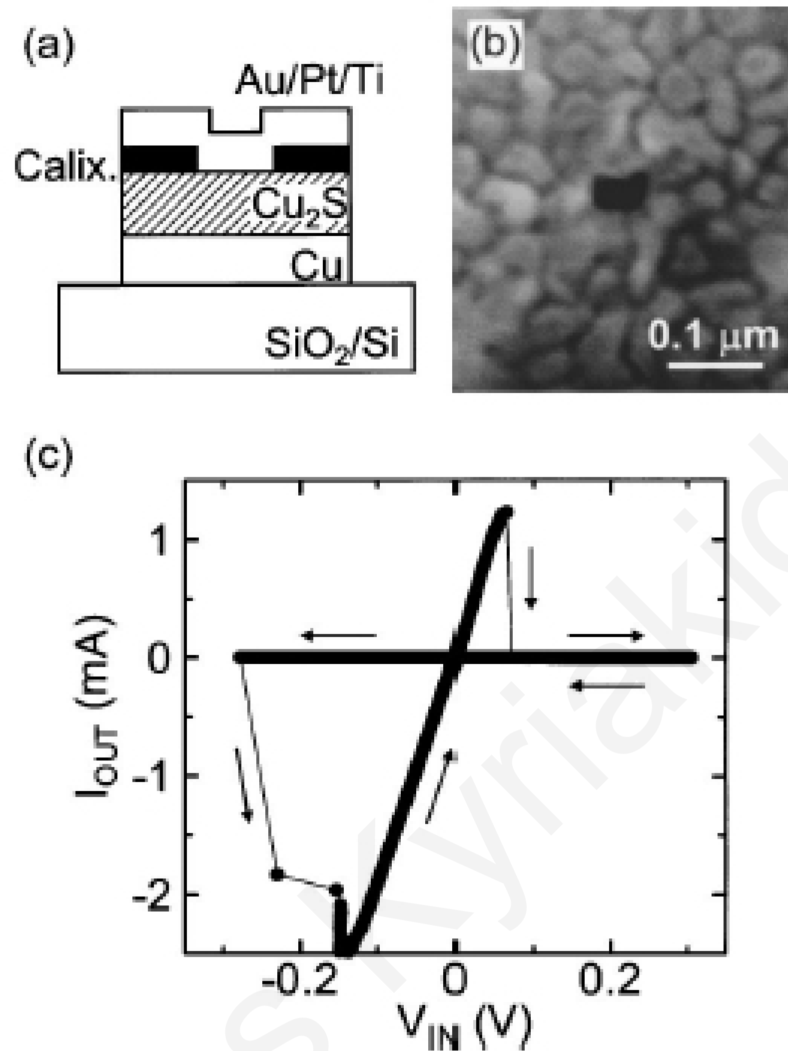

Figure 2.34: (a) Schematic view of nanometer-scale Cu_2S-based switch. (b) Plane view of top electrode with contact hole. (c) Current-voltage characteristics of the device with a 0.03 mm hole.

Cu/Ta₂O₅/Pt

The $Cu/Ta_2O_5/Pt$ structure has been proposed as a nanometer-scale switch. The function of the switch is revealed through its current-voltage characteristics, shown in Fig. 2.35. $Cu/Ta_2O_5/Pt$ devices can be fabricated on both quartz and silicon substrates. The structure is similar to the $Au/Cu_2S/Cu$ device, where an interlayer dielectric defines a contact window to one of the electrodes.

The fabrication process starts with the deposition of 10 nm-thick titanium and 50-nm thick platinum layers. This titanium layer serves as the adhesion layer and the platinum

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layer as the bottom electrode. The layers were deposited under an argon pressure of 7 mTorr. Subsequently, a 15 nm-thick Ta_2O_5 layer is deposited. The deposition is carried out using a polycrystalline Ta_2O_5 target with a 50% argon and 50% oxygen gas mixture. Finally, a 50 nm-thick layer of either Cu is deposited as the top electrode. All the layers are deposited at room temperature by RF sputtering using metal masks. The junction area of the cross-point structure measures 20 μm × 20 μm, whereas the contact window has a diameter ranging from 0.2 to 10 μm.

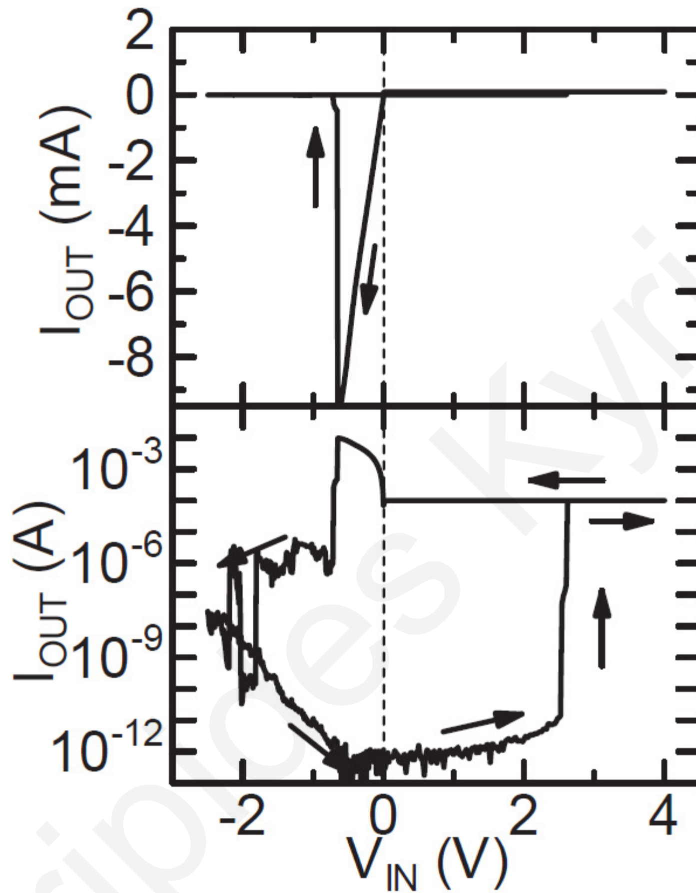

Figure 2.35: Current-voltage characteristics of $Cu/Ta_2O_5/Pt$ nanometer-scale switch in linear (top) and semilogarithmic (bottom) scales.

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2.3.4 Discussion

Memristive devices have been shown theoretically to possess unique attributes, which could enable the realization of novel applications and improvement of existing ones. They

can be used for implementation of the Hodgkin-Huxley equations and appear suitable for emulation of synaptic dynamics. The challenge that remains is the implementation of such applications. The recent discovery of memristor devices has come to bridge the gap between theory and application. The applications mentioned thus far are significant, yet others may be waiting to be discovered. However, the first step in that direction is the understanding of fabricated devices and association to theory.

The list of memristive devices presented in the previous section is representative of devices that have been shown to exhibit memristive behavior and is continuously growing as new devices are added to the bibliography. It is divided into groups according to their predominant characteristic. That can be the structure and active materials, wherever those are shown to be the critical features for their behavior, or, otherwise, the physical mechanism shown to be responsible for memristive behavior. The devices are summarized in Tab. 2.1.

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Device	Type	Mechanism	Advantages	Disadvantages
Pt/TiO_2/Pt	Metal-insulator-metal	Drifting oxygen vacancies	Small footprint	Electroforming required
Al/a-TiO_2/Al	Metal-insulator-metal	Drifting oxygen vacancies	Low manufacturing cost	Large footprint
Ti/Gd_2O_3/Pt	Metal-insulator-metal	Drifting oxygen vacancies, unipolar switching		Repeatability of results
Pt/NiO/Pt	Metal-insulator-metal	Drifting oxygen vacancies, unipolar switching		High voltage electroforming
Ag/a-Ag_2S/Pt	Metal-insulator-metal	Ag^+ filament formation		Repeatability of results
Au/Li_xCoO_2/Si	Metal-insulator-metal	Bulk switching process	No electroforming required	Unknown operation parameters
Au nanowires	Single-element	Reversible electromigration switching	Reproducible effect	Low operation frequency
Graphene	Organic	G-O filaments	Low manufacturing cost	Large footprint, CMOS compatibility
PEO/PANI	Organic	Li^+ migration, three-terminal configuration	Innovative nature	Low operation frequency
Ti/organic/Pt	Organic	Electrode-electrode or electrode-organic layer interaction	Promising results	Repeatability of results
Poly-Si nanowires	Silicon-based	Interface charge trapping/detrapping	CMOS integration	High voltage operation
Gate-All-Around Silicon Nanowire FETs	Silicon-based	Interface charge trapping/detrapping	CMOS integration	Unknown frequency/operation parameters
Ag/a-Si/p-Si	Silicon-based	Ag^+ filament formation		High speed, endurance, and retention
PCMO	Insulator-metal transition	Interface effect	Promising results	electrode effect clarification, scaling of resistance with area
$SrTiO_3$	Transition metal oxide	Movement of ionic defects or Sr ions		Repeatability of results, unknown processes
TiN/HfO_x/TiN	Valence change memory	Filament through defect accumulation	Small footprint	Filament instability
Au/Cu_2S/Cu	Cation-migration-based	Cation filament formation	Fast switching	Long reset dwell time
Cu/Ta_2O_5/Pt	Cation-migration-based	Cation filament formation	Fast switching, scalability	Average cycling endurance

Table 2.1: Comparison table of memristive devices.

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The majority of devices belong to the metal-insulator-metal category. These include the original Pt/TiO_2/Pt device, as well as the Al/TiO_2/Al, Ti/Gd_2O_3/Pt, and Pt/NiO/Pt devices, among others. Despite sharing the "sandwich" structure, these devices rely on different mechanisms to exhibit memristive behavior. The Pt/TiO_2/Pt stack (with either oxygen-deficient or oxygen-abundant layers) owes its functionality to conductive filaments consisting of drifting oxygen vacancies in the TiO_2 layer. The Al/TiO_2/Al functions in the same way, but adds the benefit of flexibility and low-cost manufacturing. The Ti/Gd_2O_3/Pt and Pt/NiO/Pt stacks are based on the same principle of oxygen vacancies, yet display unipolar switching. The Ag/a-Ag_2S/Pt stack, on the other hand, relies on Ag^+ filament formation to vary its resistance. Finally, Au/Li_xCoO_2/Si stacks rely on a bulk process in the Li_xCoO_2 layer for resistance variation. In general, devices based on the metal/insulator/metal stack exhibit a cycling endurance in the range of hundreds of cycles. This is an aspect that needs further improvement before further deployment.

Gold nanowire devices rely on reversible electromigration to vary conductivity. The major challenge faced by these devices is frequency. Even in nanometer dimensions they exhibit switching frequencies below 0.1 Hz. Though scaling the devices will increase switching frequencies, their critical dimensions are already close to fabrication limits.

Graphene-based memristors could prove very interesting in the future, however they would require a major shift from current CMOS-based fabrication processes. Given their high cycling endurance, integrating them into novel fabrication processes would take advantage of their simple manufacturing process.

The PEO/PANI device is a three-terminal organic device. It is based on the migration of Li^+ ions between the two aforementioned films. Its main disadvantage, though, is a very low frequency of operation, in the order of minutes.

A different type of "sandwich" device consists of an LB monolayer between two metallic electrodes (Ti/organic/Pt). The device clearly exhibits memristive switching and resistance tuning, but since the mechanisms involved are not conclusively determined and the results are not robust across devices, they should be studied in depth before further development.

The poly-Si nanowire device presented above, is another three-terminal device exhibiting memristive behavior. Unlike the PEO/PANI device, though, the mechanism

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involved here is charge trapping and detrapping at the interface between SiO_2 and poly-Si. The major drawback of these devices is the large voltage required for operation. In the case of gate-all-around silicon nanowire FETs, the hysteresis is observed in the I_{ds} vs. V_{ds} domain. This configuration results in large currents and warrants verification of the memristance mechanism and operational aspects.

A silicon-based "sandwich" configuration has also been presented. The crossbar array structure involves the Ag/a-Si/p-Si stack. This device relies on a silver filament formation in the a-Si layer for resistive switching. It exhibits very good operation frequency and cycling endurance.

A deviating type of device has been disclosed using PCMO. This device differentiates itself because it owes its behavior to the mixture of valence states (Mn^{4+}/Mn^{3+}) in the active film. Additionally, the mixed valence states have to be present at both metal interfaces. The results reported so far hold promise, however, due to the unknown combination of mechanisms at play in this device, some key aspects need to be clarified with further investigation. Therefore, this device should be studied further to fully elucidate the mechanisms involved. Furthermore, a major drawback of this type of device is the scaling of resistance with area.

Barring the long dwell time (i.e. the time required to restore the device from LRS to HRS), the Cu/Cu_2S device appears to be one of the most promising of the devices presented so far. It has repeatability in the range of kilocycles, a relatively short switch-on time (100 μs), a well understood physical mechanism, and is compatible with CMOS fabrication processes. Further investigation of this device should focus on scaling the device in an effort to reduce the dwell.

The $Cu/Ta_2O_5/Pt$ device is CMOS compatible, with the structure's elements already integrated into standard CMOS fabrication processes. The switching time is in the order of 10^{-5} - 10^{-4} s is relatively short. The switching mechanism allows for scaling, with patterning possible down to nanometer dimensions. The reliability is above average compared to other devices reviewed, with cycling endurance > 10^4. Therefore, the $Cu/Ta_2O_5/Pt$ device appears very promising as a potential memristor implementation.

A common denominator in the list presented thus far is the cycling endurance of memristive devices coupled with a concrete understanding of the electrochemical processes governing their behavior. A thorough understanding of the principles dictating

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their functionality is a necessary step before the widespread use and possible commercialization of memristive devices.

2.4 Conclusion

This chapter has introduced the basic concepts of this thesis: bioinspired design and memristive devices.

Bioinspired design is traced back to the first attempts at understanding biological neurons and proposing artificial equivalents. The recent resurgence in the field is documented by the prospects made available through recent breakthroughs. A brief look at the functionality of the biological neuron leads to the importance of synapses and the accurate description of membrane excitation through the Hodgkin-Huxley model. Biologically plausible learning algorithms are presented to complete the framework of neuromorphic engineering.

Subsequently, memristors and their properties are introduced. The major events in their evolution, namely their postulation in 1971 and their realization in 2008, are recounted. The distinctive characteristic of these devices is the zero-pinched bow-tie hysteresis loop in the I-V domain. The reason behind that is derived mathematically. Additionally, it is shown how this loop's area should diminish with increasing driving frequency.

Finally, a bibliographical review of memristive device implementations has been presented. The devices show the variety of structures and mechanisms that can lead to memristive phenomena. Device structures include organic, silicon-based, and metal-insulator-metal, among others. Memristance mechanisms mainly derive from ion migration. This can manifest itself into metallic filament formation, oxygen vacancy drift, electromigration, or insulator-metal transition.

The fabrication processes for these devices have been explained and their distinct memristive behavior has been indicated. Wherever possible, their behavior was explained through the underlying physical mechanism. A comparison between memristive devices leads to a critical review revealing their shortcomings. Further research is deemed necessary at the device level in order to bring memristive devices to the level of deployment.

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The next chapter focuses on the process and methodology of fabrication of the first of two memristive devices.

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Chapter 3

NiTi Device

3.1 Introduction

This chapter covers the fabrication, characterization, and modeling of NiTi devices. NiTi is the first of the two memristive devices that have been fabricated in the context of this thesis. However, the literature on NiTi devices is limited with regards to their electrical behavior. Additionally, this is the first time their hysteresis in the I-V domain has been explored. Therefore, the device's behavior had to be analyzed both qualitatively and quantitatively for subsequent circuit inclusion.

The following sections illustrate the process of rendering NiTi memristive devices ready for circuit integration. Various possible implementations were looked into before deciding on the final structures to be fabricated. Initially, the choice of the NiTi structure is explained, followed by a description of its fabrication methods. This is followed by a description of the characterization necessary for its unique properties, the methodology, and the respective results. The results are described mathematically to produce a behavioral model for the device. The model is coded in HDL, permitting its use in circuit design.

3.2 Choice of NiTi structure

Various degrees of volatility in neurons and their synapses are found in biological systems, relating to short/long-term plasticity. For example, after a stimulation to the nerve axon, the various states of that axon, as described by the Hodgkin-Huxley equations, will return

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to the initial state after a few tens of milliseconds, thus determining the need for artificial neural components with moderate volatility. On the other hand, artificial neural components with very little volatility are also required for storing information that doesn't change often, such as spatial maps. An example of these, in biology, are the NMDA receptors in the hippocampus, which are responsible for long term potentiation of synapses that store spatial information [88] over long periods of time.

Thus, it is necessary to find new components, to be added to the VLSI toolbox of computer engineers, which enable compact memory elements, with various degrees of volatility. The distribution of these memory components within the computational fabric is an important feature required for energy-efficiency [89]. Furthermore these components should be CMOS compatible and must not increase manufacturing costs significantly. Memristive devices seem to be promising candidates.

Much emphasis has been put on non-volatile memristors, given that their recent re-discovery was as a result of research aimed at developing cross bar digital memories [21], however as mentioned above there is also a need for different degrees of "leaky" memories [90] in bioinspired computational systems, in order to prevent overtraining of the neural networks. Hence, a memristive structure is presented, which is CMOS compatible and is cheap to fabricate and whose versatility is such that the degree of volatility can be controlled. The memristive structure consists of NiTi Shape Memory Alloy (SMA). The unorthodox nature of NiTi offers the potential for multi-time-scale volatility. The alloy's properties were first discovered at the Naval Ordnance Laboratory in 1959, hence the name nitinol (Nickel Titanium-Naval Ordnance Laboratory) [91].

The NiTi memristive device consists of a nearly equiatomic composition of nickel and titanium. This composition results in a physical mechanism that causes it to alternate between two lattice phases with temperature. Combined with its high resistivity, the device can undergo Joule heating, thereby changing its properties with the induced current. The effect is a drop in resistance with increased or continuous current. Thus far it has been used primarily for actuation and stents. This marks the first time a smart alloy's electrical properties are explored in relation to memristive devices. The NiTi alloy is CMOS-process compatible and can be easily added to a regular fabrication process. Micron-scale NiTi alloy wires were acquired for the purpose of this thesis and characterized with regards to their resistive behavior. The measured results were subsequently used to derive analytical models of the device.

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The prevailing mechanisms assumed to be responsible for the memristance effect in the cases of NiTi and Cu/Ta_2O_5 implementations involve change in crystal structure and ion movement in the lattice, respectively. After fabrication, behavioral models of the devices were designed to be verified through extensive characterization, a process which is described in the following chapters.

In the ensuing sections, following the description of the two implementations, the fabrication processes are detailed.

3.3 Fabrication of NiTi devices

The family of smart alloys include, amongst others, copper-zinc-aluminum-nickel and copper-aluminum-nickel. Chosen for investigation as part of this thesis was the simpler nickel-titanium alloy, NiTi, of nearly equiatomic composition. The physical mechanism responsible for changes in shape and resistivity is the transition between two lattice phases: austenite and martensite. The mechanism is known as twinning. This type of deformation consists of the rearrangement of atomic planes without causing slip or permanent deformation [92]. The thermal activation energy between the two lattice phases is quite low. At higher temperatures it takes the simple cubic crystal structure, referred to as austenite, whilst at lower temperatures it transforms into a more complicated body-centered tetragonal (monoclinic) structure, referred to as martensite (Fig. 3.1). The alloy's basic material properties are shown in Tab. 3.1.

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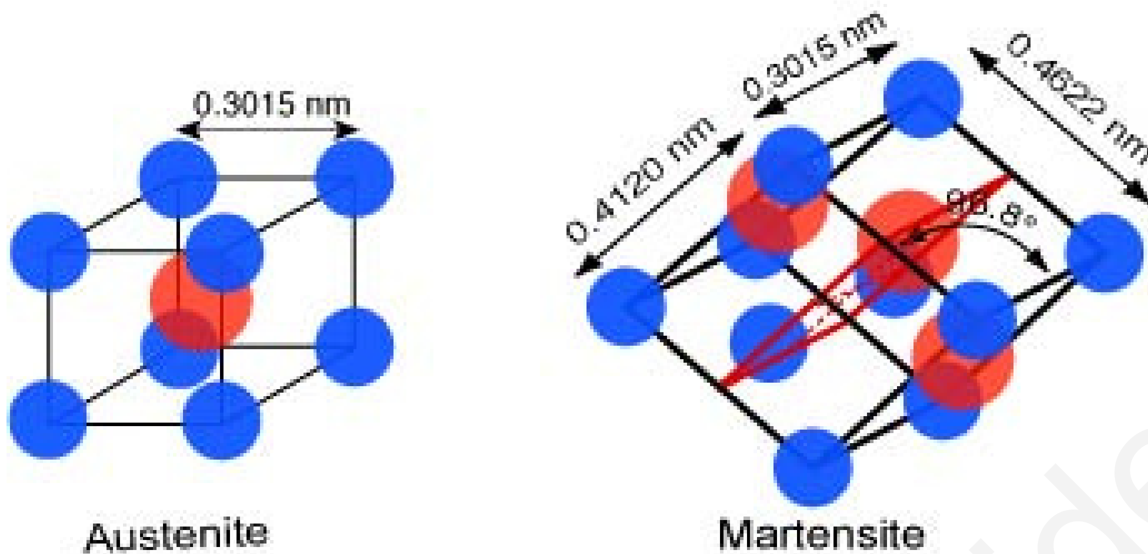

Figure 3.1: The two lattice structures of the NiTi alloy; austenite and martensite.

Property	Value	Units
Density	6,450	kg··m^{-3}
Specific heat capacity	322.3	J·kg^{-1}·K^{-1}
Melting point	1573	K
Latent heat of transformation	24.2	kJ·kg^{-1}
Thermal conductivity	20	W·m^{-1}·K^{-1}
Thermal expansion coefficient		
Martensite	6.60×10^{-6}	K^{-1}
Austenite	11.0×10^{-6}	K^{-1}
Poisson ratio	0.33	

Table 3.1: NiTi physical properties. The different thermal expansion coefficients for each lattice phase become relevant when analyzing hysteretic behavior of the alloy.

In the context of the mechanical properties of this smart alloy, the interest focuses on the contraction of the metal (Fig. 3.2). In that case, it usually suffices to find a single temperature "threshold" where it can be assumed that the transition from austenite and martensite is complete and vice versa. Note that it is possible to adjust this "threshold" by varying the composition of the alloy. In fact, even small changes in composition can significantly impact the material properties, resulting in a different "threshold". The single "threshold" approach does not however provide adequate information for the case where

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one is to use this device as a memristive device. It is later shown that the transition is spread over a few tens of degrees.

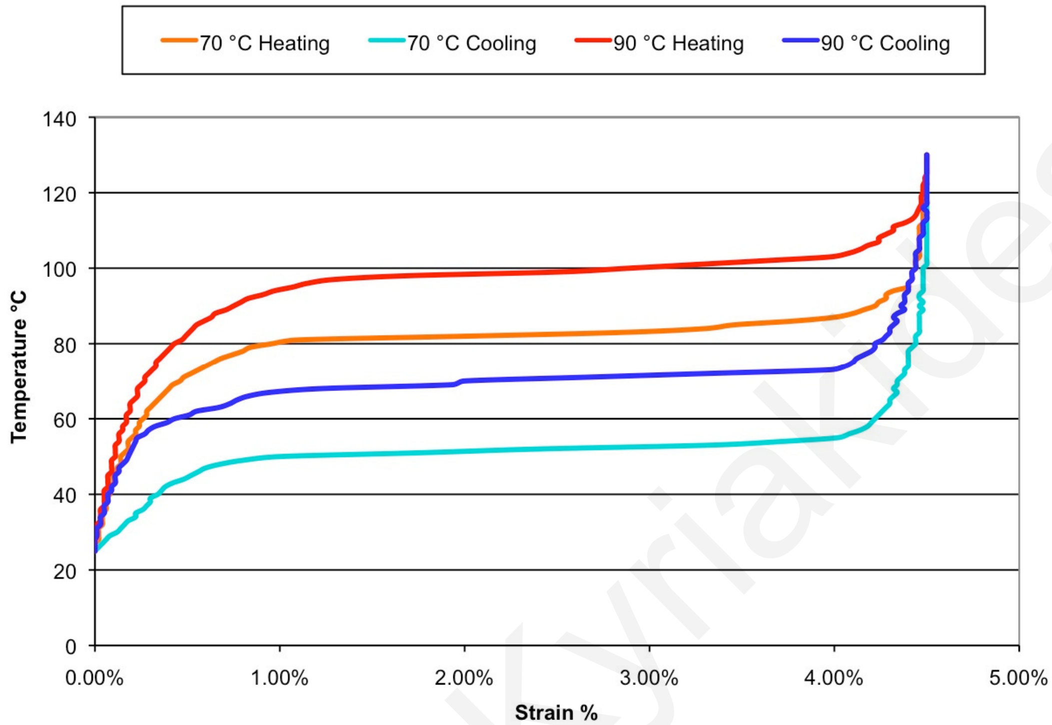

Figure 3.2: Typical temperature vs. strain characteristics for NiTi. The two sets of heating-cooling curves represent different alloy compositions.

Electrically, NiTi is classified as a conductor, where its high electrical resistance, enables it to undergo significant Joule heating that can cause the transition between the two lattice phases. Coupled together, these phenomena constitute a unique mechanism for memristive behavior; current can be driven through the device to raise its temperature, change lattice phase and reduce its electrical resistance. The current driven through the device is defined by the applied voltage over its resistance. The current driven through the device will in turn modify its resistance. The variable resistance will modulate the current through the device. This feedback loop cannot be treated instantaneously rather over a specific time interval, where the voltage and current are integrated over time. Given that the time integral of voltage is defined as the flux (Eq. 2.16) and the time integral of current is the charge (Eq. 2.15) through the device, it follows that the flux φ is coupled with the charge q. Above-threshold flux activity leads to an increase in charge flow. Equivalently, one can observe a drop in resistance with an increase in voltage that causes self-heating.

With these memristive properties it is expected that NiTi devices can be used to implement the Hodgkin-Huxley dynamics where a voltage can be used to "open" the path for more charge carriers (i.e., lower resistance) as happens with the Na^+ and K^+ ion channels. Moreover, NiTi memristive devices can be used for short-term learning synapses in Hebbian neural circuits, whereby often used paths have greater charge carrying capacity.

3.3.1 Enclosure fabrication

In order to characterize the proposed memristive devices, at first it is necessary to know how the resistivity varies as a function of temperature as the crystal structure transitions between the two states. Subsequently, the relationship between the applied voltage and the resulting current, which will provide the self-heating energy, can be determined. This energy, in conjunction with heat losses, will determine the NiTi temperature at a particular moment in time, which along with prior temperatures will define the memristive state at a particular point in time.

Alloy samples measuring 25 µm in diameter were obtained from Dynalloy, Inc., Irvine, California. The composition of these alloys is between 55% -56% nickel and 44% - 45% titanium. Attempting limit the heat losses that would enhance the memory effect of the device, ways to encapsulate the NiTi alloy were considered. These were enclosed in borosilicate glass (Pyrex) and subsequently heat treated to 840 °C so that the borosilicate glass would completely enclose the NiTi alloy. A schematic of the resulting device and the manufacturing result are shown in Fig. 3.3 and Fig. 3.4, respectively.

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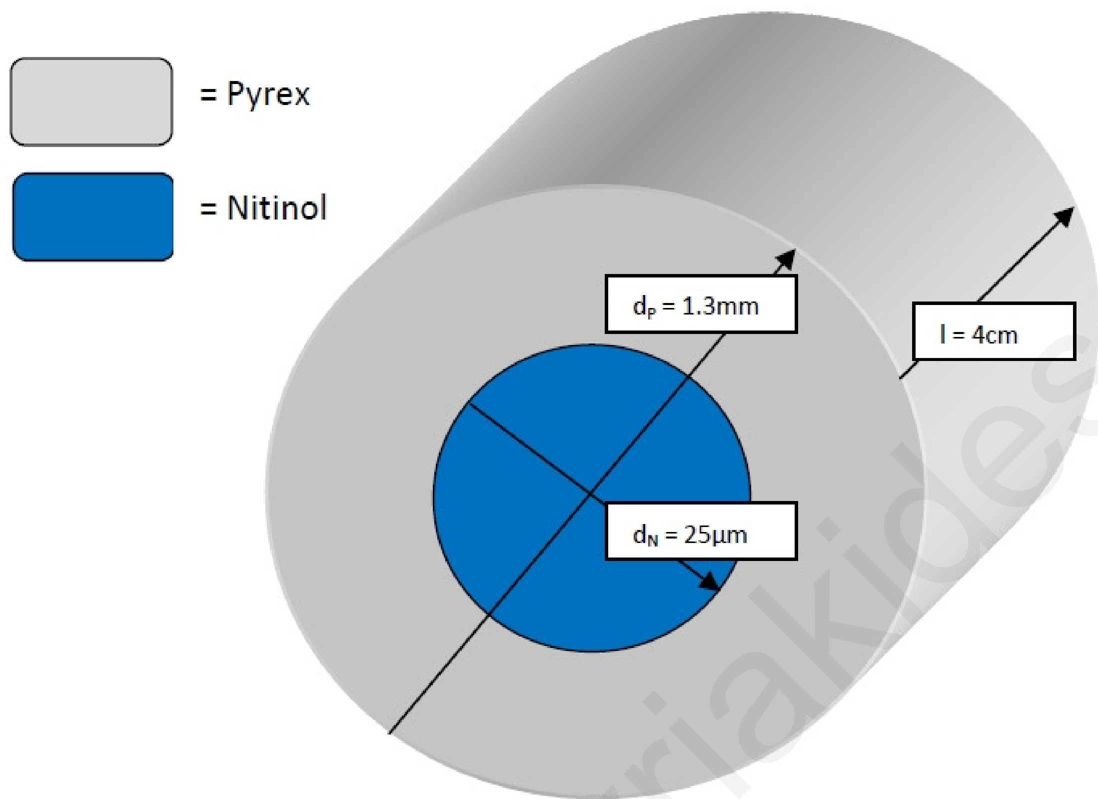

Figure 3.3: Schematic of NiTi enclosure.

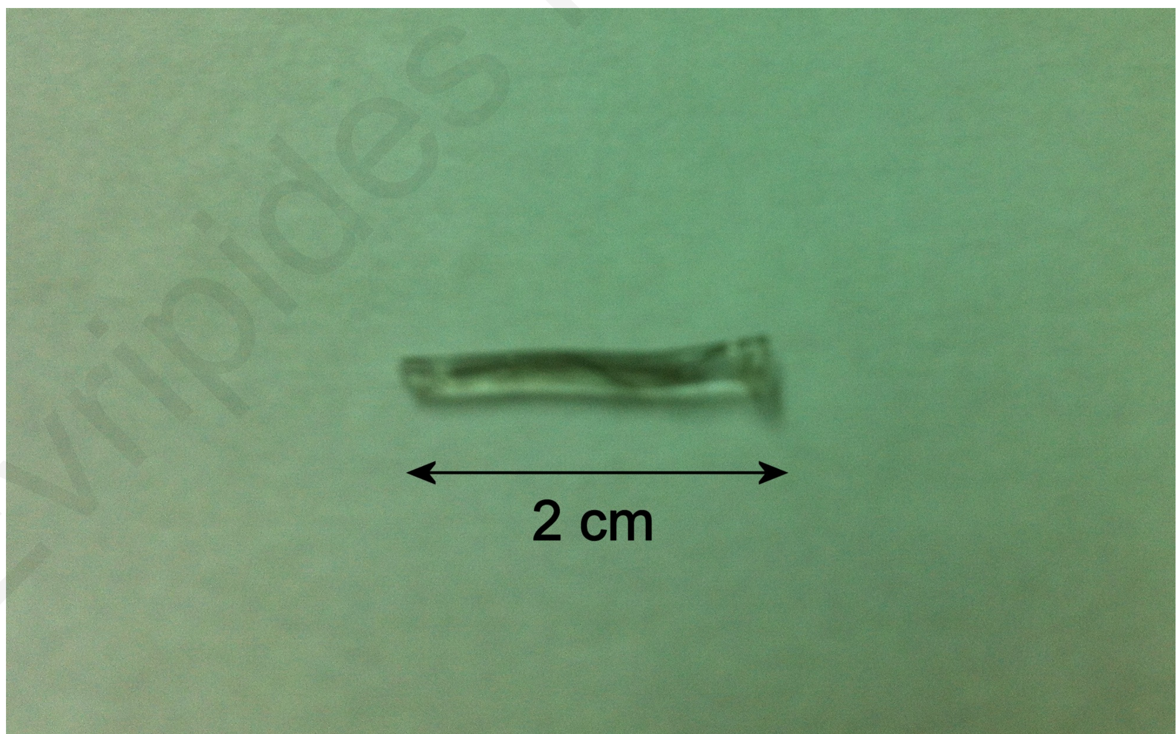

Figure 3.4: Image of a NiTi enclosure of a 2 cm alloy segment. Borosilicate glass is used to encapsulate NiTi alloy in an effort to limit ambient heat loss.

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3.3.2 Discussion

When stimulated with a voltage pulse, the NiTi memristive device's resistance will drop as the device self-heats. Once the stimulus is withdrawn, the "time-varying resistance" will start to increase as the device cools back to the ambient temperature. This characteristic can be used to obtain short-term potentiation in memristive synapses, since if a second voltage spike arrives before the NiTi has returned to its original state, more charge will flow through the potentiated memristive device. In practice, in order to achieve different volatility time constants, chip designers can vary the geometry of the memristive devices.

The fabrication of NiTi devices, as described above, produced unexpected results. Uncharacteristically high resistances were measured during testing. The most probable explanation is the oxidization of nickel during the heating process. This produces a layer of insulating NiO thereby not permitting effective contact between the test equipment and the device. A remedy for this procedure is the heat treatment in inert N_2 atmosphere. However this procedure was not feasible under available equipment. An alternative is the use of bare wires which will serve the purpose of proof-of-concept.

NiTi thin films can be integrated into ICs through deposition on wafers in a CMOS-compatible graphoepitaxial co-sputtering process [94] or by basic co-sputtering of two targets onto an unheated wafer. The latter method gives rise to amorphous NiTi, which can be annealed at the upper limit of CMOS-compatible post processing, i.e. 400 °C [95], to give a crystal structure to the single metal layer that will form the basis of the memristive devices on chip. Millisecond flash annealing will work for the newer CMOS technologies, which are more sensitive.

The devices need to be thin enough so as to be easily restrained on the chip by limiting their mechanical strength. The time constants associated with the heating and cooling of the memristive devices are directly related to their shape and cross-sectional area [96]. These films can be wet etched with a mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and DI water [97], while access to the underlying CMOS circuits can be provided through vias. In recent technologies it is common to have six or more metal layers. By using one or more of these to add the NiTi memristive structures, it is possible to open up a whole new range of design possibilities.

The behavior of NiTi was defined using various electrical characterization techniques, as described later. The modeling of the device was completed using Verilog-A in Cadence

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Virtuoso environment based on the characterization results. The results of the modeling are presented in the form of coding and simulation results in the following chapter.

3.4 Characterization and modeling of NiTi devices

The variation in NiTi resistance stems from two factors; thermal expansion and change in crystal structure. Both of these factors depend on the device's temperature. In order to characterize the proposed NiTi devices, it is first necessary to know how the resistivity varies as a function of temperature as the crystal structure transitions between the two lattice phases. Subsequently, the relationship between the applied voltage and the resulting current, which will provide the self-heating energy, can be determined. This energy, in conjunction with heat losses, will determine the NiTi temperature at a particular moment in time. A given temperature, along with prior temperatures, will define the memristive state at a particular point in time.

Therefore, in order to obtain a preliminary description of the memristive behavior of NiTi as a function of temperature, NiTi samples were obtained. Measurements on these samples must be used in conjunction with heat loss simulations and ab initio calculations to produce the model of the devices.

3.4.1 Methods

The NiTi devices were modeled in the aspect of their thermal characteristics. To that end, NiTi samples were acquired from Dynalloy, Inc. The samples were bare, crimped NiTi wires measuring 25 μm in diameter. Their transformation temperature was designed by the manufacturer to be 343.15 K (70 °C).

Whilst the heat is induced through Joule heating, the cooling of the devices is a result of convection through the ambient medium. Therefore, whereas the Joule heating phase can be calculated in a straight-forward manner, the cooling phase has to be modeled.

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The measurements for the heating phase were made using a temperature chamber and a Digital Multimeter (DMM), whereas the heat loss process was simulated using a multi-physics platform. A Keithley 2100 DMM was used in conjunction with an ESPEC SU-261 temperature chamber to measure the resistivity of NiTi devices. The four-wire resistivity measurement setup and the equipment used is shown in Fig. 3.5. The computational model presented in this work was developed using the multi-physics CFD-ACE+ platform (ESI, Paris, France) [98] and it describes the behavior of the devices during the heat loss phase [99].

As shown below, the results of the NiTi ab-initio calculations and heat loss computational model yielded the Verilog-A code and Cadence model for the simulated memristive device.

Figure 3.5: Four-wire resistivity measurements: The Keithley 2100 DMM, used to measure the NiTi device resistance during heating, connected to the ESPEC SU-261 temperature chamber, used for controlled heating of the NiTi devices.

3.4.2 Thermal simulations

In the same way that a gated ion channel memristor returns to its original state with the removal of the voltage stimuli, NiTi device's "time-varying resistance" will increase after the self-heating voltage pulse is withdrawn. In order to utilize these memristive devices in bioinspired circuits, it is necessary to know how long it will take for the device to return back to its original state. This amounts to finding out the time required by the structure to cool down to the martensite state.

For NiTi wires exposed to room-temperature static air, the transition time between the austenite and martensite phases ranges between 150 ms to 17 s, depending on the thickness of the wire [96]. The transition time can be reduced by designing the phase change to occur at higher temperatures, so that the larger temperature difference ΔT allows for greater heat flow, or by using smaller diameter wires, which have a much larger surface area to volume ratio. Furthermore, if the NiTi memristive devices is encapsulated in SiO_2 on a chip, then the relaxation time is expected to drop down to tens of milliseconds or less, which is in the timescales required by gated channels of neuronal dynamics. As a first step towards creating models for the time-dependent behavior of NiTi memristive devices, finite volume analysis simulations were conducted in order to be able to extract compact equations suitable for use in the Cadence simulation environment [100].

The computational model used in CFD-ACE+ platform to quantify the cooling behavior of the NiTi wire - by mapping heat loss - consists of two distinct zones, namely, the NiTi wire domain and the air zone which surrounds it. The NiTi wire measures 4×10^{-2} m in length by 2.5×10^{-5} m in diameter, while the air domain around it has a thickness of 1.4875×10^{-3} m. Model particulars are presented in Tab. 3.2. The presence of the outer air domain, as depicted in Fig. 3.6, helped improve the accuracy of the NiTi cooling results as this domain represented a sound abstraction of reality where convective currents facilitate heat transfer.

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Parameter	Unit	Value	Reference
Mass-density, ρ_m			
NiTi	$kg \cdot m^{-3}$	6,450	[101]
Air	$kg \cdot m^{-3}$	1.2041	[102]
Specific heat capacity, C_p			
NiTi	$J \cdot kg^{-1} \cdot K^{-1}$	322.3	[101]
Air	$J \cdot kg^{-1} \cdot K^{-1}$	1,012	[102]
Thermal conductivity, κ			
NiTi	$W \cdot m^{-1} \cdot K^{-1}$	20	[101]
Air	$W \cdot m^{-1} \cdot K^{-1}$	2.5×10^{-2}	[102]
Dynamic Viscosity, μ			
Air	$kg \cdot m^{-1} \cdot s^{-1}$	1.78×10^{-5}	[102]

Table 3.2: NiTi-Air computational model particulars.

The axisymmetric computational domain of the NiTi-Air model was discretized using structured conforming meshes, mainly owing to the relatively simple geometry of the NiTi-Air system and the higher accuracy permitted by a structured, versus an unstructured, grid. Heat flux in the computational domain was modeled through the transient (time-dependent) solution of the energy equation. Crank-Nicolson's second order time accurate scheme was used with a blending factor of 0.6 and a time-step of 5×10^{-4} s.

The convection in the air domain was modeled through the numerical solution of the flow equations, namely, the continuity equation and the Navier-Stokes equations. Boundary conditions at all sides of the model were kept adiabatic except in the inlet (left) entrance and outlet (right) exit of the air domain. Air velocity in the air zone was kept constant to 0.3 $m \cdot s^{-1}$ throughout the simulation.

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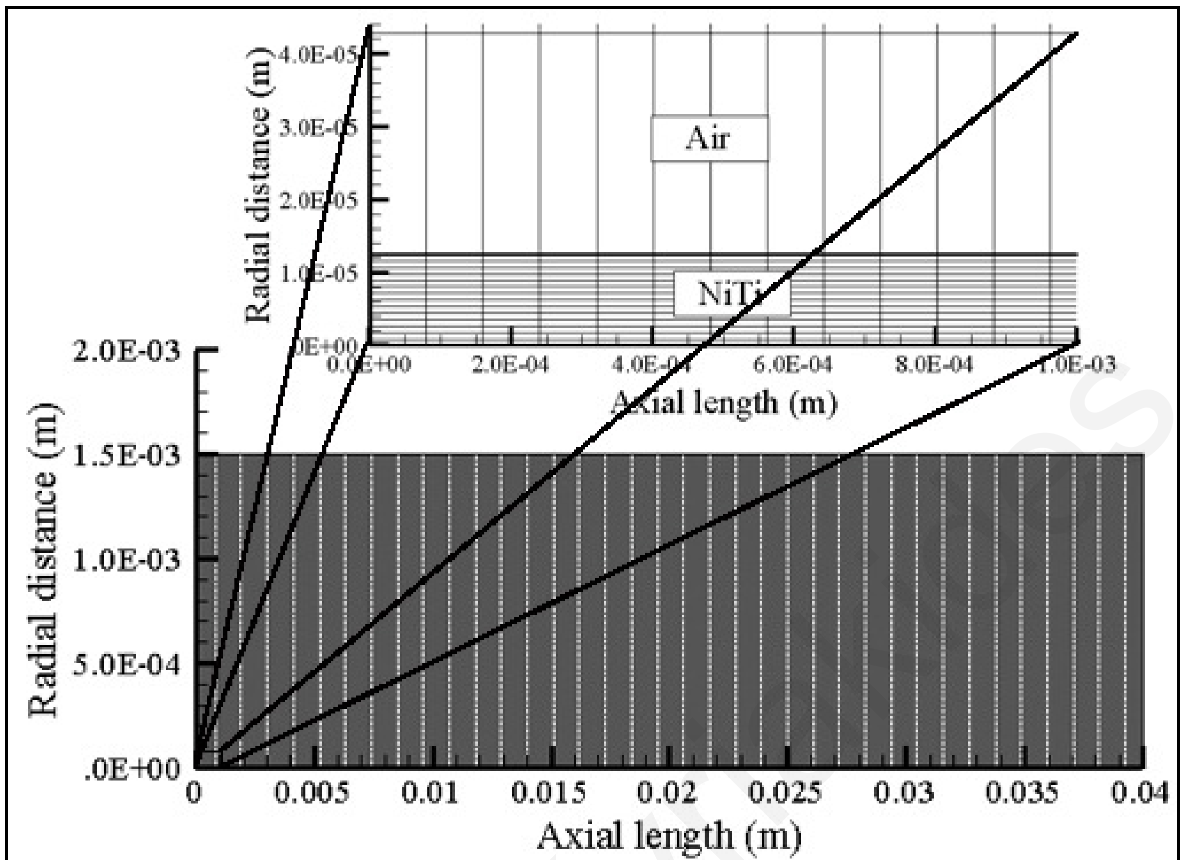

Figure 3.6: The NiTi-Air computational mesh used to calculate heat loss. The lower grid shows the NiTi-Air (axisymmetric) model which consists of 28,443 cells. The top-grid detail highlights the NiTi finer model domain surrounded by the coarser air grid.

Heat transfer in the NiTi wire and the air domain was traced through the numerical solution of the total enthalpy equation [99]. Fig. 3.7 shows the evolution of the temperature drop in the NiTi, at a radial distance of 6.25 μm from the wire's center which experiences an exponential thermal energy decay. The wire's initial condition temperature was set to a uniform value of 348 K while the air temperature was set to 298 K. Inlet air temperature was kept to 298 K for the entire simulation. In aggregate, the simulation reached a steady state temperature of 298 K in considerably less than a second.

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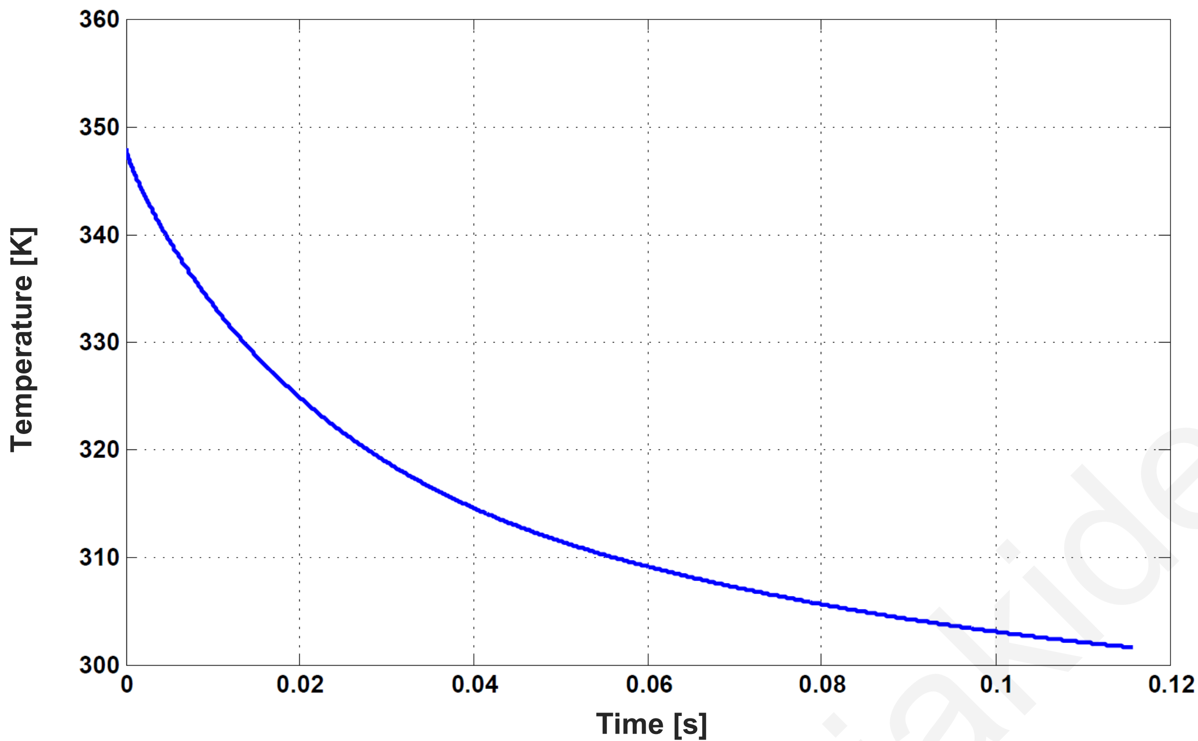

Figure 3.7: Model results of NiTi cooling extracted from the CFD-ACE+ platform. The NiTi temperature is traced during convection cooling from 348 K to steady state.

In order to evaluate the heat loss model, the results can be compared with measured. As shown in Fig. 3.8, which is presented in the next section, the transition from austenite back to martensite phase starts at approximately 350 K and is predominantly completed by 300 K. As seen in Fig. 3.7, this is corresponds to a cooling time of 140 ms, which is very close to the measured restoration time of 180ms [96].

3.4.3 Resistance measurements

The NiTi samples were heated and cooled using a temperature chamber while a DMM was measuring resistance. This procedure was necessary in order to define the samples' change in resistance with respect to temperature. The maximum temperature was varied in order to investigate its effects. As shown in Fig. 3.8, interesting results arose, with their resistance lagging in the cooling phase compared to the heating phase. Also evident is the increase in the area of the lagging curve with increasing peak temperature.

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The samples were forced-air heated to a range of steady-state temperatures in order to investigate the temperature dependence of their resistance. Using an Espec SU-261 temperature chamber, the device temperature was varied while a Keithley 2100 DMM was used to measure the sample resistance. The measurements were conducted using the four-wire resistivity method in order to eliminate the unwanted lead and contact voltage drop. Polytetrafluoroethylene (PTFE - Teflon) plates ensured that the samples were kept electrically insulated. The temperature range was initially set to include the transformation temperature, ranging from room temperature (298.15K, 25 °C) to 353.15 K (80 °C), however in subsequent measurements the range was increased from a lower limit of 273.15 K (0 °C) to an upper limit of 363.15K (90 °C) in order to reach deep into each of the alloy's two crystal states.

Resistance measurements show the resistance-temperature behavior of NiTi. Fig. 3.8 shows the experimental results normalized for a 4×10^{-2} m wire segment for maximum temperature (T_{max}) of 353.15 K (80 °C) and 363.15 K (90 °C). The two curves in the graph represent the change in resistance as the chamber is heated (Ascending) up to 353.15 K (80 °C) or 363.15 K (90 °C), respectively, and subsequently cooled (Descending) down to 273.15 K (0 °C).

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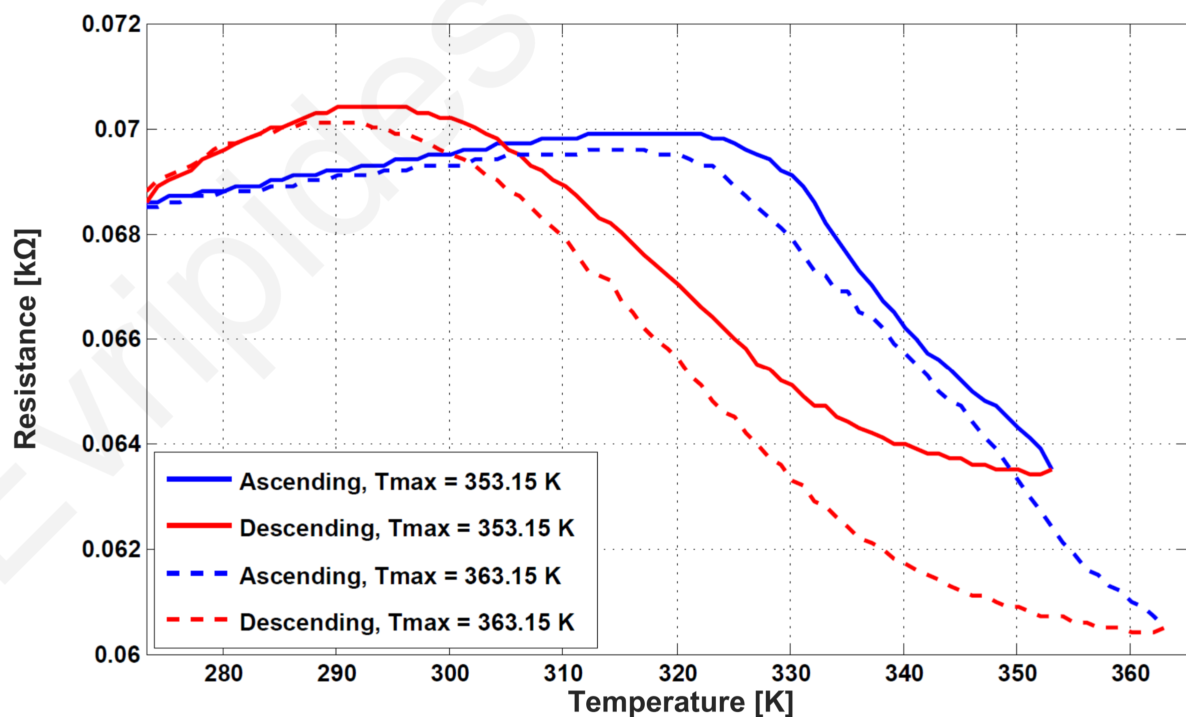

Figure 3.8: NiTi resistance heating curves for T_{max} of 353.15 K (80 °C) and 363.15 K (90 °C).

During heating, a segment of slight increase in resistance is followed by a sharp drop in resistance as the crystal structure assumes the austenite form. During cooling, the resistance increases with a characteristic lag as a “thermal deactivation energy barrier” needs to be overcome for the alloy to return to the initial martensite state. Although the ascending curve follows a unique pattern (irrelevant of T_{max}), the descending curve depends heavily on T_{max} reached by the wire. T_{max} defines the shape of the descending curve, the cross-point and the maximum resistance below it. An interesting observation is the overlap noted in the descending curve above the ascending curve for temperatures below the cross-point.

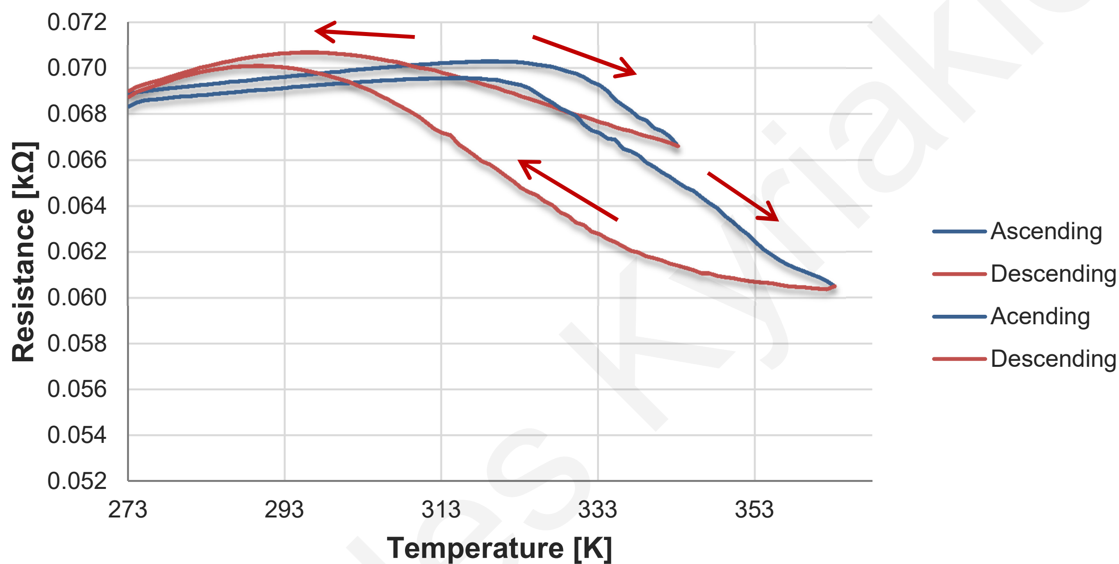

Figure 3.9: NiTi resistance measurements depicting two ascending-descending cycles with different peak temperatures.

Mathematical representation of the results obtained through controlled heating and cooling of the devices required the use of data analysis. The measurements were thus introduced into Origin®, a scientific graphing and data analysis platform. Curve-fitting was performed through nonlinear regression using the Levenberg-Marquardt algorithm in the Origin® platform. A small (< 1.5%) linear offset between measurements was present even in identical samples. It is attributed to the material-lead interface and was not included in the curve-fitting calculations. Sample measurements are shown in Fig. 3.9, whereas the fitted curves are shown in Fig. 3.10. Comparing the matching between measured results and fitting curves, they are shown to be in good agreement.

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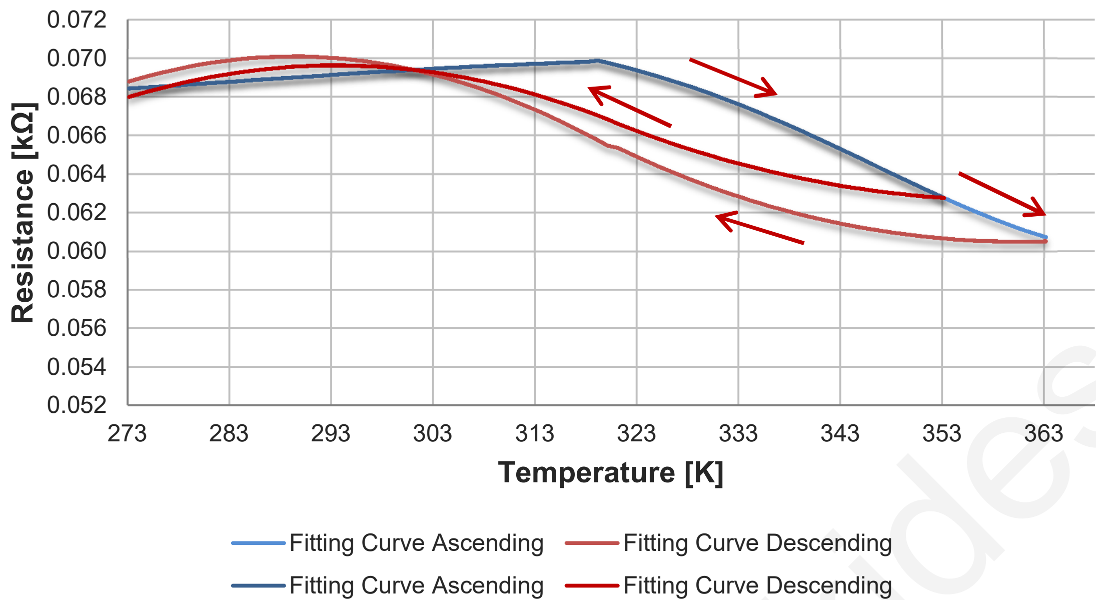

Figure 3.10: NiTi resistance curve-fitting depicting the respective fitting curves of two ascending-descending cycles with different peak temperatures.

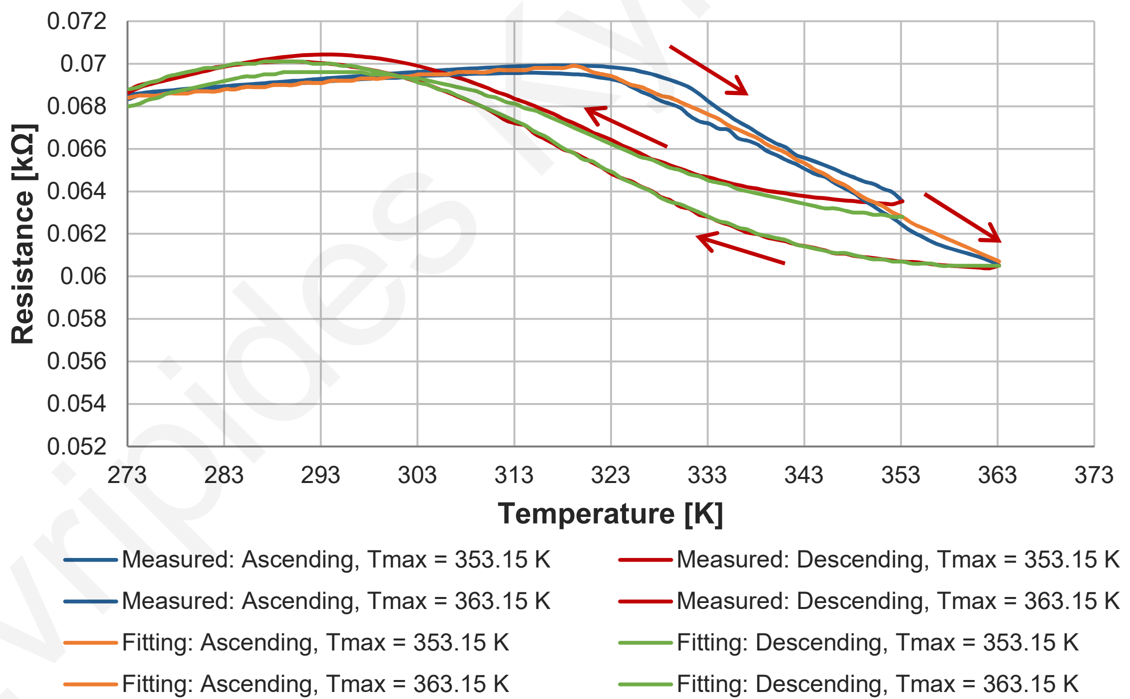

Figure 3.11: NiTi resistance measurements with respective fitting curves of two ascending-descending cycles with different peak temperatures.

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3.4.4 Behavioral modeling

The measurements presented in the previous sections provide the relationships of resistance with respect to temperature (curve-fitting results), on one side, and temperature with respect to time (simulation results), on the other. The relationships deduced were mathematically described. A model of the device thus becomes feasible by joining the two aspects of device functionality into a single entity.

Revisiting the curve-fitting results, the deduced relationships yield heating curves that can be considered extensions of a single function up to T_{max}. The same does not apply to cooling curves. Cooling curves display a multiplicity depending on T_{max}. This increases the complexity and computational overhead to an impractical level. As such, curve-fitting parameters prove difficult to incorporate into a behavioral model. Conversely, ab initio calculations are less computationally intensive and present no convergence issues in a simulator. The following analysis shows that ab initio calculations for the Joule heating effect yield verifiable results.

The model computes all the parameters that affect the resistance of the NiTi sample. The heat created is calculated through a first principles approach, whereas the heat loss is calculated using the cooling simulation data. The required algorithm for such a model is illustrated in a flowchart (Fig. 3.11) and unfolded in detail below.

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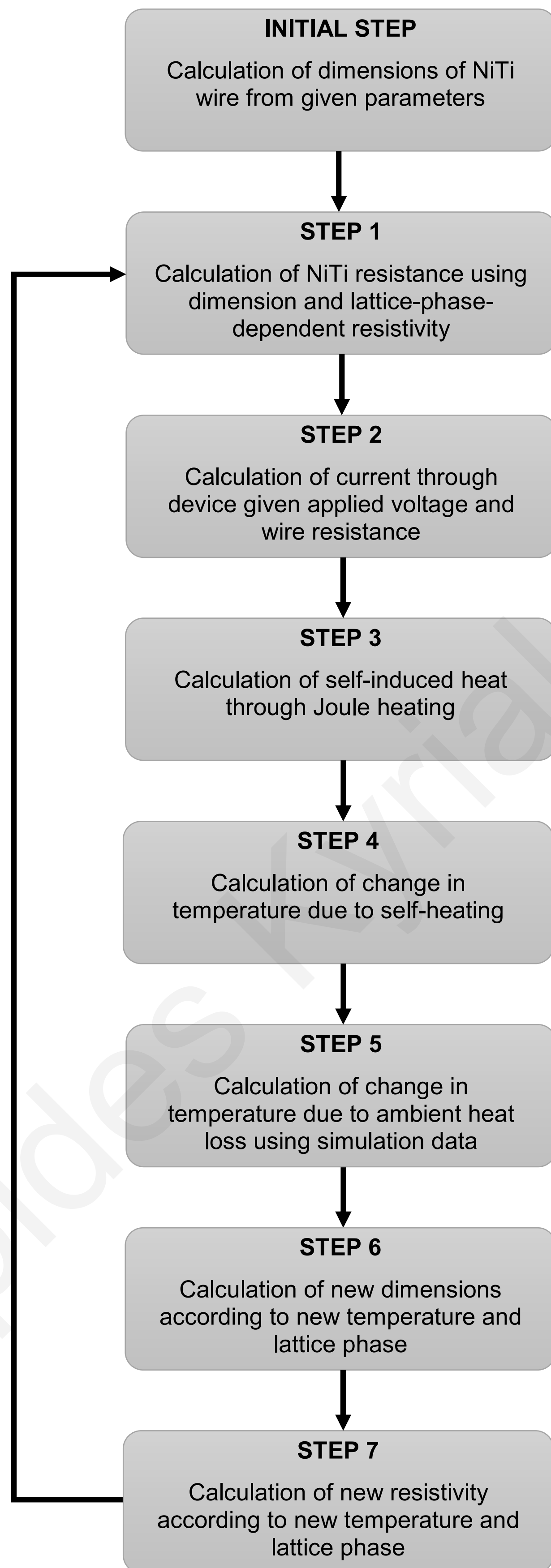

Figure 3.12: Flowchart of algorithm for NiTi simulation.

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NiTi model algorithm

Initial step || Calculation of dimensions

During the first iteration only, the dimensions of NiTi wire (length, diameter) are imported from the parameter list provided. The dimensions of the sample are stored (length, diameter), while other parameters are calculated (cross-sectional area, mass). According to the initial conditions, the sample is at room temperature, therefore the alloy is at martensite lattice phase.

$$A_i = \pi \, {r_i}^2 \quad (3.1)$$

where,

A_i = initial cross-sectional area

r_i = initial radius

$$m = L_i \, A_i \, \rho_V \quad (3.2)$$

where:

m = mass

L_i = initial length

ρ_V = volumetric density

Step 1 || Calculation of resistance

The sample resistance is calculated through $R = \rho \, L/A$, where R is resistance, ρ is resistivity, L is length, and A is cross-sectional area of the sample. The resistivity is initially that of martensite at room temperature, whereas the length and cross-sectional area

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were derived in the initial step. In subsequent iterations the resistivity gradient is necessary. The resistivity gradient relates the change in temperature with the change in resistivity and is lattice-phase-dependent.

$$R = \rho_i \frac{L_i}{A_i} \tag{3.3}$$

where,

R = resistance

ρ_i = resistivity

L_i = initial length

A_i = initial cross-sectional area

Step 2 || Calculation of current

The current through the sample is defined as $I = V/R$, where V is the applied voltage and R is the sample resistance derived in the previous step. This is the variable that is output by the model.

$$I = \frac{V}{R} \tag{3.4}$$

where,

I = current

V = applied voltage

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Step 3 || Calculation of self-induced heat

The Joule heating is calculated through $\Delta Q = I^2 \, R \, \Delta t$, where ΔQ is the heat created by current I, R is the resistance of the device and Δt the time interval between successive iterations.

$$\Delta Q = I^2 \, R \, \Delta t \tag{3.5}$$

where,

ΔQ = generated heat

Δt = time interval

Step 4 || Calculation of change in temperature due to self-heating

The increase in temperature due to self-heating is calculated as $\Delta T = \Delta Q/(c \, m)$, where ΔQ is the net change in energy, c is the specific heat capacity, and m the sample mass.

$$\Delta T^{+} = \frac{\Delta Q}{c \, m} \tag{3.6}$$

where,

ΔT^{+} = change in temperature due to self-heating

c = specific heat capacity

Step 5 || Calculation of change in temperature due to ambient heat loss

The ambient heat loss is calculated through the heat loss curve extracted from simulation, shown in Fig. 3.7. Curve-fitting is performed on the data through nonlinear regression using the Levenberg-Marquardt algorithm in the Origin® platform.

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Additionally, the time derivative of the resulting curve is calculated. Thus, it becomes possible to calculate the new temperature as a result of heat losses. The new temperature is calculated through $\Delta T = T' \Delta t$, where T_i is the initial temperature and T' is the temperature gradient with respect to time.

$$\Delta T^{-} = T' \Delta t \tag{3.7}$$

where,

ΔT^{-} = change in temperature due to heat losses

T' = temperature gradient with respect to time

Step 6 || Calculation of new dimensions

The new temperature is calculated using the changes due to self-heating and heat loss. The new dimensions are calculated (length, cross-sectional area) using the change in temperature, the Poisson ratio, and the linear expansion coefficient, which depends on the lattice phase. These are fed back to the first step for the next iteration.

$$\Delta T = \Delta T^{+} + \Delta T^{-} \tag{3.8}$$

where,

ΔT = total change in temperature

$$T = T_i + \Delta T \tag{3.9}$$

where,

T_i = initial temperature

T = new temperature

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$$a_L = \begin{cases} 1.1 \times 10^{-5}\ \mathrm{K}^{-1}, & \text{if } T \geq T_{th} \\ 6.6 \times 10^{-6}\ \mathrm{K}^{-1}, & \text{if } T < T_{th} \end{cases} \quad (3.10)$$

where,

a_L = linear expansion coefficient

T = temperature threshold

$$\Delta L = L_i\, a_L\, \Delta T \quad (3.11)$$

where,

ΔL = change in length

$$L = L_i - \Delta L \quad (3.12)$$

where,

L = new length

$$\Delta d = d_i\, \nu\, \frac{\Delta L}{L} \quad (3.13)$$

where,

Δd = change in diameter

d_i = initial diameter

ν = Poisson ratio

$$A = A_i + \frac{\pi}{4}\left[(d_i + \Delta d)^2 - {d_i}^2\right] \quad (3.14)$$

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where,

A = new cross-sectional area

Step 7 || Calculation of new resistivity

The new resistivity is calculated using the resistivity gradient with respect to temperature, which depends on the lattice phase. This is fed back to the first step for the next iteration. Given the resistivity gradient as

$$\rho' = \begin{cases} 5.0 \times 10^{-10}\ \Omega \cdot \mathrm{m\ K^{-1}}, & \text{if } \mathrm{T} \geq \mathrm{T_{th}} \\ 2.3 \times 10^{-9}\ \Omega \cdot \mathrm{m\ K^{-1}}, & \text{if } \mathrm{T} < \mathrm{T_{th}} \end{cases} \tag{3.15}$$

where,

ρ' = resistivity gradient,

then the new resistivity is calculated as

$$\rho = \rho_{th} - [\rho'\ (T_{th} - T)] \tag{3.16}$$

where,

ρ = new resistivity

ρ_{th} = resistivity at T_{th}.

Factor contribution

Using Eq. 3.3 ($R = \rho\, L/A$), the contribution of each factor - resistivity and dimensions - to the change in resistance, can be calculated. Change in resistivity with respect to temperature is given by the resistivity gradient in Eq. 3.15. Change in length with respect to temperature is defined by the linear expansion coefficient in Eq. 3.10. Change in cross-sectional area with respect to temperature is defined by:

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$$\frac{\Delta A}{A_i \, \Delta T} = -2\,\nu\,a_L + \nu^2\,a_L^2. \tag{3.17}$$

This entails two different contributions; above and below the temperature threshold. Using Eq. 3.3 we can calculate the two contributions as a percentage of the total change in resistance per degree K. Hence, if $T \geq T_{th}$, the resistivity contribution to the change in resistance is 0.0134%, otherwise, if $T < T_{th}$, the resistivity contribution to the change in resistance is 0.102%. Thus, the change in resistance is predominantly a geometric effect.

Software implementation

The algorithm was coded in Verilog-A HDL in Cadence environment. The resulting module describes a NiTi device through all its possible transitions, i.e. any combination of Joule heating and convective cooling. As a component in a larger system it proved reliable, with no convergence issues that can be common with Verilog-A components in analog simulations.

A circuit simulating a standard voltage sweep was implemented in Cadence Virtuoso. Inserting the NiTi module into the circuit, a simulation of an I-V sweep is run. The result, shown in Fig. 3.13, shows the response of the NiTi module. The Verilog-A code for the NiTi model is available in full in Appendix C.

Fig. 3.14 depicts the corresponding measurement from a NiTi sample taken using a Keithley 4200-SCS without forced heating. The result shows the expected hysteresis at room temperature.

The matching of the measured and simulation results is confirmed in Fig. 3.15, where they are plotted together.

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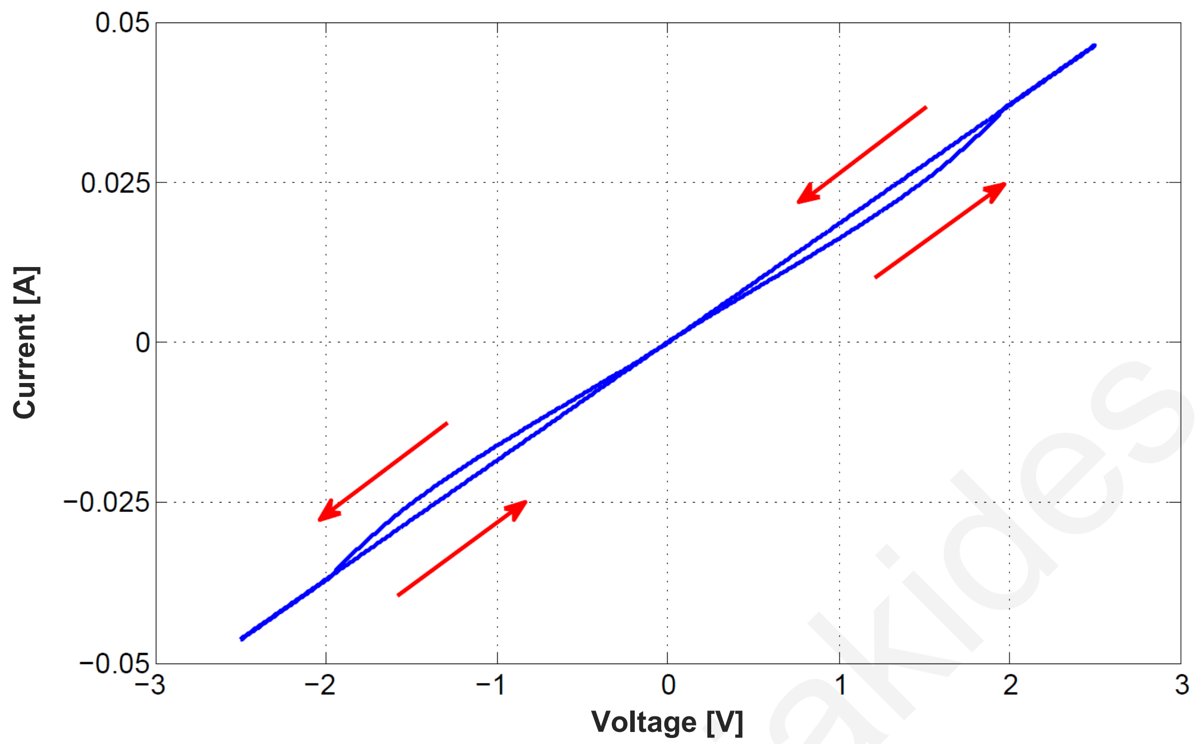

Figure 3.13: Simulation of I-V sweep applied to a 4 cm NiTi device using Verilog-A model.

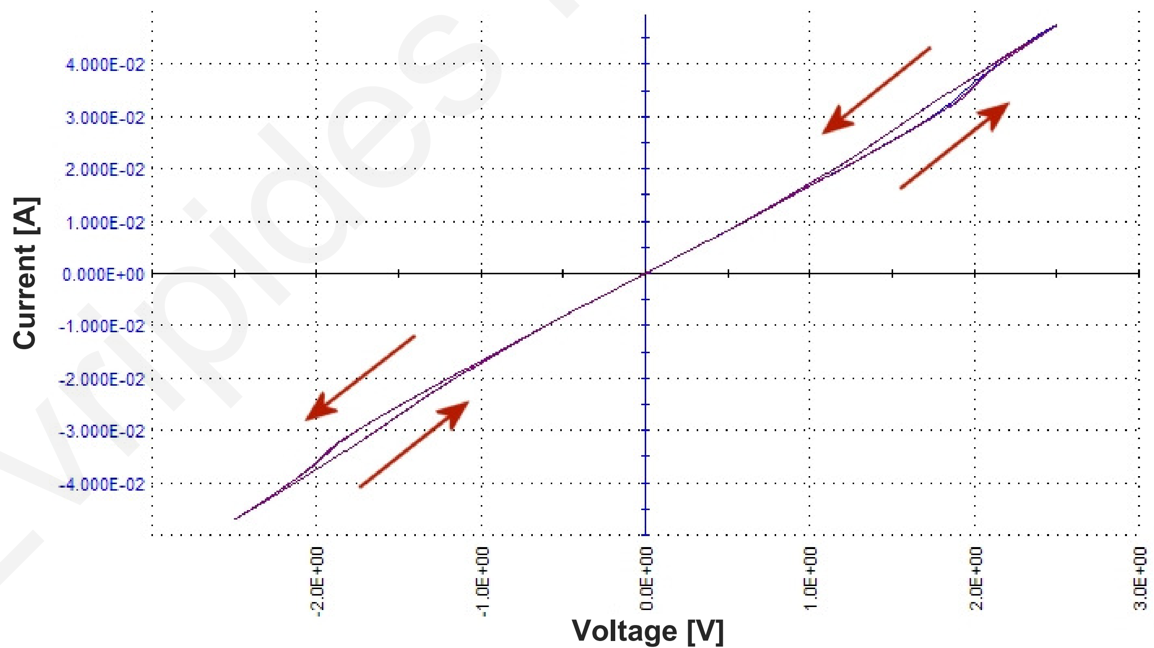

Figure 3.14: I-V sweep measurement of a 4 cm NiTi device showing hysteresis.

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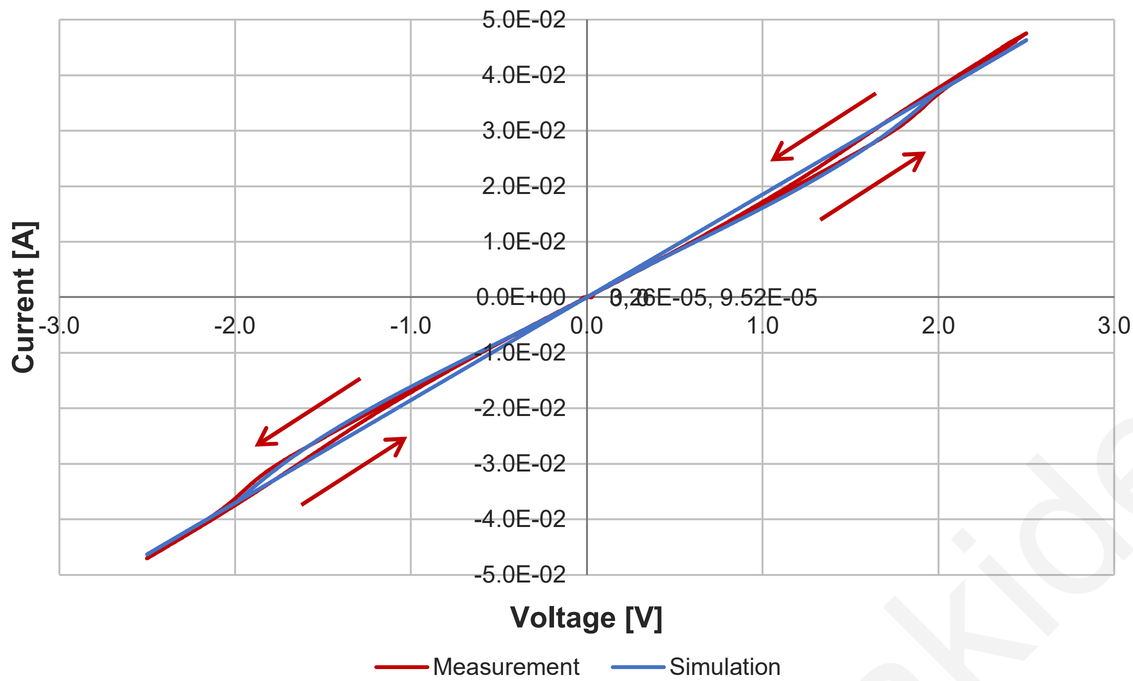

Figure 3.15: Comparison of I-V sweep measurement with simulation obtained using the coded Verilog-A model for a 4 cm NiTi device. Both measurement and simulation show the anticipated hysteresis.

3.4.5 Discussion

A memristive device based on NiTi scales well to smaller feature sizes, since less energy will be necessary to heat the device. The resistance can be increased by decreasing the ratio of cross-sectional area to length, thus providing larger changes in voltage across the device. It is, however, anticipated that as the size goes down, and becomes comparable to the crystal dimensions, new effects will start to appear [103] that will need further investigation.

NiTi thin films can be deposited on wafers in a graphoepitaxial co-sputtering process or by basic co-sputtering of two targets onto an unheated wafer. Both methods are CMOS-compatible. The latter method requires annealing to produce a crystal structure out of the amorphous NiTi, a step which can be performed within CMOS-compatible post processing parameters. Alternatively, millisecond flash annealing is available for newer, more sensitive CMOS technologies. The structures need to be thin enough so as not to have the

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mechanical strength to significantly stress the chip. The time constants associated with the heating and cooling of the NiTi devices are directly related to their shape and cross-sectional area permitting direct correlation to design specifications. These films can be wet etched, with access to the underlying CMOS circuits provided through vias.

An example below will illustrate the practical feasibility of a NiTi memristive device. Using a conservative minimum photolithography feature size could yield a wire of width 0.18 μm, thickness 0.1 μm, and length 100 μm. A voltage pulse of amplitude 48 mV and width 0.5 ms is applied to the wire segment. Using $\Delta Q = Ii^2\, R_i\, \Delta t$, where ΔQ is the heat created by current I_i, R_i is the initial resistance of the device and Δt the time interval under consideration, the heat created is 32.1 nJ. Subsequently, the change in device temperature induced by ΔQ is calculated.

Using $\Delta T = \Delta Q/(c\, m)$, where c is the specific heat capacity of NiTi and m the device mass, the final device temperature is 348 K (75 °C). Therefore, a 0.5 ms pulse can drive the device to a low resistance state.

The aforementioned device can remain in the lowest resistance state (above 328 K) for 15.9 ms, but takes up to 180 ms to completely return to the martensite form (the low resistance state is preserved according to the timescales associated with cooling). Depending on the non-volatility one wants to specify for a given device, one can change the dimensions and geometry of the device or alter the surrounding material with low thermal conductivity passivation layers.

Regularly spiking neurons, could maintain the memristive device in a particular state, whilst the geometrically-adjusted retention time of the memristive device could be used to build neural oscillators. The inclusion of nano-heaters [104] can be used to maintain the ambient chip temperature constant.

3.5 Conclusion

This chapter has described the fabrication of a NiTi memristive structure. The specific device was chosen for fabrication due to its unique characteristics that result in memristive effects.

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The fabrication method involved enclosing NiTi alloy in borosilicate glass through heat treatment. The NiTi devices were characterized for their change in resistance with respect to temperature, while heat loss was mapped using a multi-physics platform. Ab initio calculations in conjunction with simulation results were then joined to create a Verilog-A mathematical model. Finally, simulations run with the NiTi model have been shown to agree with respective measurements.

The following chapter repeats the same procedure, with a different methodology, for the Cu/Ta_2O_5 structure.

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Chapter 4

Cu/Ta_2O_5 Device

4.1 Introduction

This study aims to explore the use of memristive devices in bioinspired circuits. For this purpose, two devices were fabricated. The devices' behavior had to be fully understood for their inclusion in such circuits. However, similar to NiTi, Cu/Ta_2O_5 devices are still at a preliminary phase of development and have only recently been identified as memristors. Therefore, extensive characterization had to be performed on the fabricated Cu/Ta_2O_5 devices.

The Cu/Ta_2O_5 devices were designed and fabricated in a cleanroom facility. A series of fabrication steps, involving wet oxidation, evaporation, lift-off, sputtering, and dry etching, were used to construct the devices. Due to the intricate fabrication process, a verification of the desired structural result was performed. Optical microscopy and SEM/FIB imaging were thus used to verify the successful creation of the structures.

The fabricated devices had to be characterized and modeled before they could be incorporated into circuit design simulators. This process is described below, following the methodology and equipment used. The results are subsequently presented and categorized, where appropriate. Lastly, the results are described mathematically to produce a behavioral model. The model is evaluated through comparison to electrical characterization data. The model is then coded in a HDL module, permitting its use in neural circuit design.

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4.2 Choice of Cu/Ta_2O_5 structure

Various possible implementations were looked into before deciding on the final structures to be fabricated. Two different implementations were decided upon, each for the advantages it bears that can lead to novel application circuits. Besides NiTi, other elements that would give reversible processes such as copper and lead were investigated. The first published implementation of a memristor, which involves TiO_2, was considered, however, TiO_2 appears to have direct repeatability issues. Another possibility was NiO-based devices. However, that was eliminated due to the tainting nature of nickel. Nickel requires dedicated equipment due to contamination issues in relation to the sputtering process. Thus, unless specially prepared, cleanrooms cannot handle metals such as nickel that contaminate machines, leaving traces when used with other materials. Organic implementations were discarded due to complicated fabrication procedures that make them incompatible with CMOS fabrication. Potential patent infringement forced a rejection of other promising implementations, such as a-Si-based structures. PCMO devices carry most of the characteristics required for neuromorphic applications, yet carry a distinct disadvantage in area; size being an important consideration for future scaling. Copper-migration-based atomic switches fulfil the majority of requirements with reference to the scope of this thesis. Since their behavior shows strong similarities with memristive traits (e.g. hysteresis, switching, bipolarity) the devices will be tested for adherence to memristive constraints.

All parameters considered, the Cu/Ta_2O_5 implementation was chosen for development. This implementation consists of a sandwich device employing an ion-sourcing top electrode of copper and a solid electrolyte - the Ta_2O_5 layer - above the bottom platinum electrode. The copper electrode sources ions into the solid electrolyte layer depending on the current polarity. A resulting filament formation induces a change in resistivity of up to three orders of magnitude. In so doing, the device exhibits bipolar resistive switching. This structure is in its primary research stages and has not yet been used as a memristive device. Additionally, the elements of this structure are already integrated into standard CMOS fabrication processes.

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4.3 Fabrication of Cu/Ta_2O_5 devices

The Cu/Ta_2O_5 device consists of a sandwich structure employing an ion-sourcing top electrode of copper and a solid electrolyte above the bottom platinum electrode. The copper electrode sources ions into the solid electrolyte layer depending on the current polarity. A resulting filament formation induces a change in resistivity up to three orders of magnitude. The operating principle of this structure is shown in Fig. 4.1.

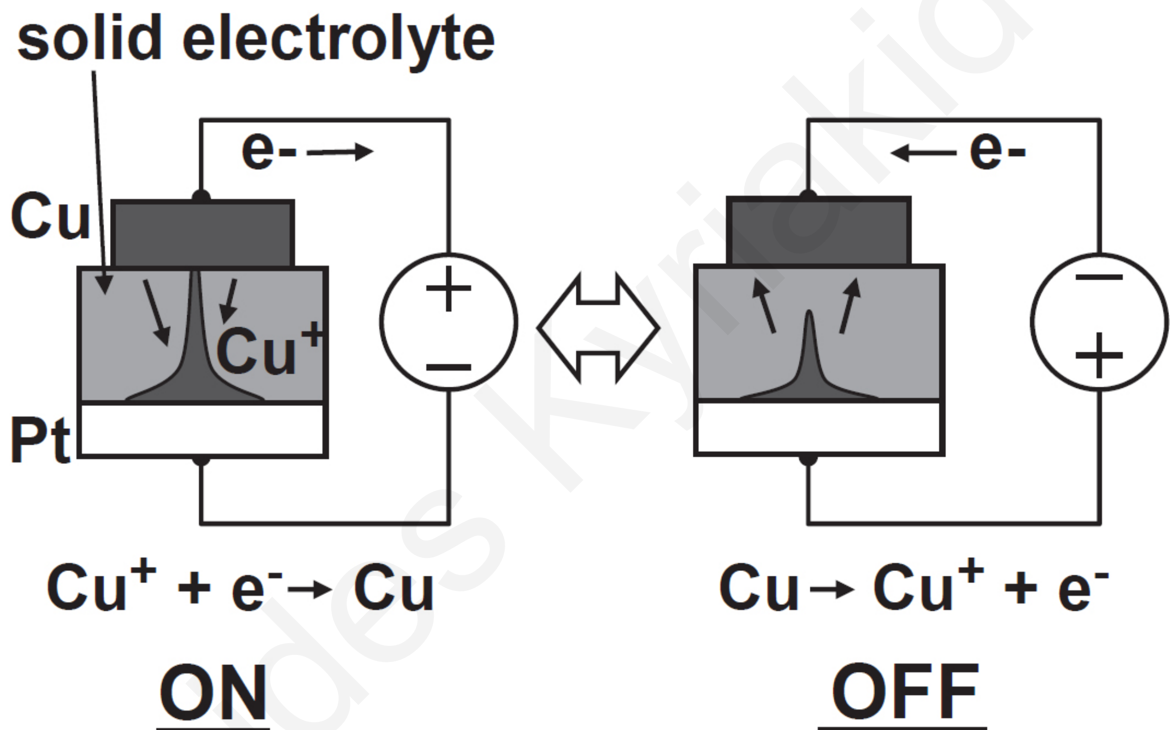

Figure 4.1: Operating principle of Cu/Ta_2O_5 device. A Cu^+ filament formation and dissolution is responsible for the ON and OFF states.

The major fabrication steps of the proposed Cu/Ta_2O_5 device are shown in Fig. 4.2, whereas the layouts are shown in Fig. 4.3. The fabrication methods necessary are described in the following subsection, concluding with the detailed process flow. Using metrology and imaging equipment, such as profilometers and microscopes, the fabricated devices were checked at various stages of the fabrication. Microscope images from intermediate steps of the fabrication process are also presented. SEM images were taken for both the virgin state and the post-formed region of the completed devices. An initial electrical characterization on the fabricated devices took place immediately after fabrication to

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confirm the expected results. The extensive characterization measurements were concluded with ultra-sensitive (femtoamp-resolution) equipment following the completion of the fabrication phase and are described in detail in the following chapter.

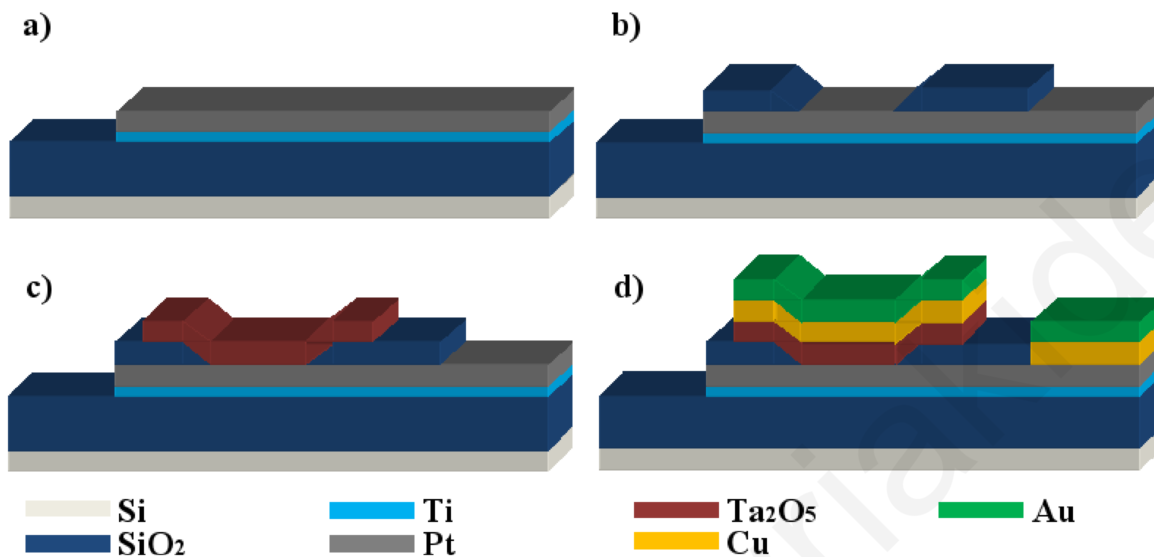

Figure 4.2: Major fabrication steps of Cu/Ta_2O_5 device: (a) Bottom electrode, (b) Interlayer dielectric, (c) Ta_2O_5 layer, and (d) Top electrode. For clarity purposes, the illustrations are not drawn to scale.

In order to investigate the effects of interface area between the top electrode and the dielectric layer, geometry variation analysis has been included in the devices to be investigated (Fig. 4.3). This produced different area openings (active device area) in the contact-limiting SiO_2 layer. The segmentation of the active device area was included as another variation to investigate possibly diverging effects with respect to a single opening of the same area. Some devices featured lateral positioning of the top and bottom electrodes. Devices with no top electrode were also fabricated to verify the contribution of the top electrode to observed behavior. With the parameters of the device defined, the layouts to be used for device fabrication were completed ahead of fabrication.

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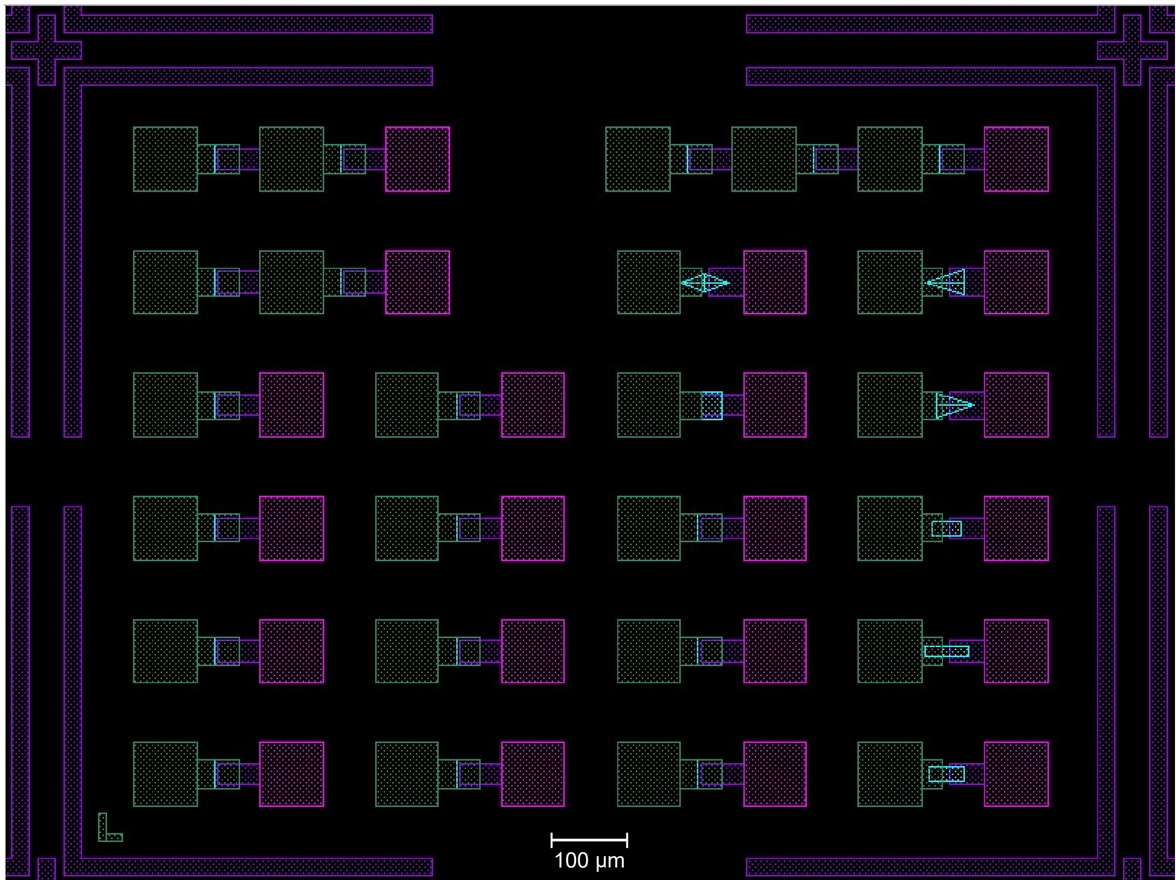

Figure 4.3: Top-level layout of a cell of Cu/Ta_2O_5 devices extracted from Cadence Virtuoso design environment. Devices included in each cell feature a variation in their active region geometry. The cell is repeated across the available wafer.

The following procedure describes the fabrication steps (process flow) for the $Cu/Ta_2O_5/Pt$ device. The device uses SiO_2 as an interlayer dielectric, thereby defining the active device region. This device provides for a probe window to the platinum bottom electrode. Gold is added on top of the copper electrode to avoid oxidization of copper. Dry etching is used for the Ta_2O_5 patterning. Lift-off is used for the Pt/Ti and Au/Cu patterning.

The main technologies used are mask fabrication, sputtering, evaporation, lift-off, dry etching, wet etching, and dicing. For each mask, the critical dimension is defined as the smallest dimension, either feature or distance, on the mask. Additionally, the critical alignment represents the maximum error possible in mask alignment between masks. The wafer is made of p-type Si, with Miller Indices <100>. The wafers measure 100 mm in diameter and 525 µm in thickness. Their resistivity ranges between 0.1 and 0.5 Ω·cm. The basic parameters of fabrication, namely technologies used, photolithography masks, and substrate type, are summarized in Tab. 4.1.

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Technologies Used			
Mask fabrication, Sputtering, Evaporation, Positive resist, Lift-off, Dry/Wet etching, Dicing			
Photolithography Masks			
Mask	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	131.5 μm	First Mask	Bottom electrode structuring
2	1.5 μm	5 μm	Active device region and probe window structuring
3	21.5 μm	10 μm	Tantalum Pentoxide structuring
4	21.5 μm	10 μm	Top electrode structuring
Substrate Type			
Silicon <100>, Ø 100 mm, 525 μm thick, Single side polished, Prime, p-type, 0.1 - 0.5 Ω·cm			

Table 4.1: Basic fabrication parameters of Cu/Ta_2O_5 devices.

The layout of the devices shown in Fig. 4.3 was extracted from Cadence Virtuoso. The extraction resulted in four photolithography masks included in a GDS file. Each of the four masks was then compiled for use by an optical pattern generator. The optical pattern generator transferred each mask onto a chromium mask.

The wafer is initially prepared by generation of an oxide layer to serve as substrate. Then, for each mask necessary, a PR layer is spin-coated onto the wafer. The PR is exposed to produce the mask patterns. Depending on the required step, the wafer is then taken through deposition or etching. The successive deposition and etching leads to the formation of the structure on the wafer. To complete the process, the wafer can be checked and diced to create dies for use with peripheral components.

4.3.1 Fabrication methods

The cleanroom methods used for the fabrication process of the Cu/Ta_2O_5 devices are hereby described. The equipment used for each fabrication step, which is part of the Center of MicroNanoTechnology [105] of the École Polytechnique Fédérale de Lausanne, is described in detail in Appendix A.

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Mask generation

The GDS files generated at the design stage are written onto chromium masks. These masks are later used with a mask aligner to transfer design patterns onto a wafer. The design is written on blank chromium mask plates using a laser scanner. Each photolithography step requires a different mask. This process achieves μm resolution in the best resolution mode. For higher resolution, e-beam lithography must be used.

Wet oxidation

The first step in the processing of a silicon wafer, wet oxidation, is performed in a dedicated furnace. Wet oxidation is used to obtain thick oxide layers (0.5 - 2.0 μm) to be used as a mask or barrier layer for deep silicon etching. The oxidation rate is much higher as compared to the dry route. However, the fixed charge density is higher in wet oxide than in a dry oxide, making wet oxide inadequate as gate oxide for MOS transistors.

Resist processing

For each layer deposition, layer etching or lift-off process, a photoresist (PR) layer must be spin-coated onto the wafer. The resist processing "recipe" is commonly programmed into a cluster system that uses a robotic arm to transfer the wafer through stages, following the defined steps. These steps include alternating steps of PR deposition, spinning cycles, and baking steps.

PR exposure

PR exposure is the process by which the PR previously spin-coated onto the wafer is exposed. This is the step by which features are created onto the wafer. The exposure through a mask leaves two areas on the wafer; those where the PR has been exposed and those where it has not. Depending on whether positive or negative PR has been used, a subsequent chemical bath step will remove one of the two types of PR (exposed or not).

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The exposure step is completed using a mask aligner. The printing is performed through controlled gap proximity using ultraviolet (UV) light illumination of the photosensitive resist. The whole wafer is exposed in a single flash for a few seconds. Due to the feature sizes involved, exact mask alignment is critical. The key limit of the process accuracy is light diffraction through the mask opening. The disadvantages of this exposure method are the sensitivity to PR thickness homogeneity and damage induced by the presence of dust particles between the mask and the wafer's top surface.

Evaporation

The evaporation technique involves evaporating a material placed in a crucible by heating it to a high temperature. This is accomplished either by a current flowing through a resistive nacelle (Joule effect), or by bombardment with an electron beam. The process takes place at a high vacuum level (~10^{-7} mbar). Evaporation can deposit metallic or insulating layers.

The advantage of the technique of deposition by evaporation over the sputtering technique is limited contamination because of the level of vacuum achieved in the equipment. Compared to the sputtering technique, vapor deposition of alloys is complex and the composition of the deposited layer is difficult to control.

Sputtering

The sputtering technique is used to deposit metal or insulating layers on wafers. Sputtering is the term describing the mechanism by which atoms are stripped from the surface of a material by a collision with high energy particles.

The deposition material, called the target, can be a pure metal, an alloy, or a dielectric material. Depositing oxide or nitride layers can be achieved with a metal target in the presence of oxygen or nitrogen. These deposits are called reactive (reactive sputtering).

Pre-cleaning of the surface of the wafer is done by ion bombardment under vacuum just prior to deposition. This is important in the cases where it is deemed necessary to ensure the total removal of a native oxide or to ensure a surface that improves adhesion of the

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deposited layer. Cleaning of the target just before vacuum deposition is essential to ensure a good quality layer.

Sputtering is advantageous with respect to evaporation deposition due to: (a) Good thickness uniformity of the deposited material on the plates by using large area targets, (b) Better alloy composition control than by evaporation, and (c) The substrate surface can be cleaned under vacuum before deposition.

Conversely, the shortcomings of this type of deposition are mainly: (a) Low deposition rate for some materials, such as SiO_2 or Si, (b) Some materials (e.g. organic materials) do not support ion bombardment, (c) The vacuum level in the equipment is higher in sputtering than by evaporation deposition, and (d) The possibility of inserting impurities in the deposited layers is increased with the sputtering method.

Etching

Etching is the process of selective removal of deposited layers from a wafer. Deep reactive-ion etching (DRIE) is the type of etching process used in this case. DRIE is a type of dry etching technique. Dry etching uses a plasma, whose energetic neutral free radicals attack the wafer surface. As opposed to wet etching, DRIE is highly anisotropic, thus able to etch away high-aspect-ratio features, such as deep trenches. Recent advancements in CMOS fabrication, such as Through-Silicon Vias (TSVs) are created using DRIE.

Wet bench chemistry

Chemical processing is used with a variety of fabrication steps, most commonly with PR lift-off. This is performed at a dedicated wet bench. The wafer containing the processed PR is taken through a series of baths at the wet bench to remove the PR. Ultrasonic activation is often used to assist in the PR dissolution. At completion, special cleaning cycles are used to remove residual metal particles from the wafer.

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Imaging

In addition to optical microscopy, other methods for verifying the fabrication results and the device operation can be employed. Using an SEM/FIB setup, it becomes possible to probe into a nano-scale device and gain valuable insight. Since the device involves the movement of ions during its operation, changes in the lattice can be observed. Using a Focused Ion Beam (FIB) column, the device can be etched across its active region area, thereby revealing a cross-section of all layers. A Scanning Electron Microscopy (SEM) can then be used to closely observe the layers. By repeating this procedure before and after a device has been electroformed and switched, changes in the originally deposited layers can be sought.

4.3.2 Process outline

The following figures describe the fabrication steps, as performed in sequence, for the construction of the Cu/Ta_2O_5 device. The index of materials used for fabrication is presented in the chart in Fig. 4.4.

The process begins with wet oxidation of the silicon wafer to create an insulating oxide layer. This is followed by the Lift-Off Resist (LOR) process. This process entails the deposition of thin films over patterned PR. By lifting off the PR, the film is removed wherever PR was present or remains otherwise. This is followed by the deposition of the interlayer dielectric through sputtering and its structuring through dry etching. Sputtering and dry etching is subsequently repeated for the Ta_2O_5 layer. A second LOR process is performed for the Au/Cu bilayer to complete the process.

Crystalline Ta_2O_5 has been shown to have negligible ionic conductivity. Conversely, the use of sputtering for Ta_2O_5 deposition creates an amorphous layer, which may enhance ionic conductivity [106]. The importance of ionic conductivity will be delved into in subsequent sections.

Following Step 10 (Fig. 4.15), a profile scan was performed to determine the etching depth due to the relatively unknown fabrication parameters of Ta_2O_5. The scan, shown in

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Fig. 4.16, was successful in verifying the expected etch rates for the oxide. Verification using an optical microscope was also performed, as shown in Fig. 4.17.

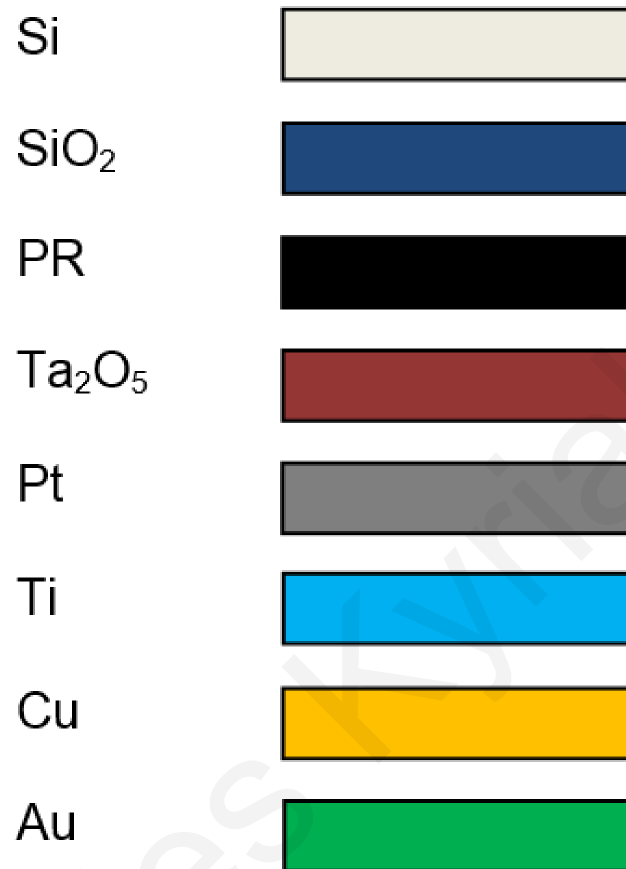

Figure 4.4: Material color chart for Cu/Ta_2O_5 fabrication.

Step	Process description	Cross-section after process
1	**Process**: Wet Oxidation **Machine**: Centrotherm **Substrate**: Si **Thickness**: 0.5 µm	0.5 µm

Figure 4.5: Step 1 is the wet oxidation of a silicon wafer to create a SiO_2 layer upon which the fabrication will take place.

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Step	Process description	Cross-section after process
2	**Process**: Photolithography LOR **Machine**: EVG 150 **Photoresist**: LOR 400nm + AZ 1512HS 1.1 µm **Mask 1**: CD = N/A	131.5 - 140 µm

Figure 4.6: Step 2 is the first step of the LOR process, namely, the LOR deposition.

Step	Process description	Cross-section after process
3.1	**Process**: Metal Evaporation **Machine**: LAB 600 H **Metal**: Ti **Thickness**: 10 nm	10 nm

Figure 4.7: Step 3.1 continues the LOR process, which involves the evaporation of two metals serving as the device's bottom electrode. In the first part, titanium is evaporated to serve as adhesive layer using LAB 600 H.

Step	Process description	Cross-section after process
3.2	**Process**: Metal Evaporation **Machine**: LAB 600 H **Metal**: Pt **Thickness**: 50 nm	50 nm

Figure 4.8: Step 3.2 is the second part of metal evaporation for the bottom electrode. Here, platinum is evaporated using LAB 600 H.

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Step	Process description	Cross-section after process
4	**Process**: Lift-off **Machine**: Plade Solvent **Metal**: Pt/Ti	

Figure 4.9: Step 4 completes the LOR process. The LOR is chemically lifted in a wet bench, leaving behind the desired bilayer of Pt/Ti.

Step	Process description	Cross-section after process
5	**Process**: Sputtering **Machine**: SPIDER 600 **Material**: SiO_2 **Thickness**: 50 nm	50 nm

Figure 4.10: Step 5 is the sputtering deposition of the SiO_2 interlayer dielectric.

Step	Process description	Cross-section after process
6	**Process**: Photolithograp hy **Machine**: EVG 150 **Photoresist**: AZ 1512HS 1.1µm **Mask 2**: CD = 5 µm	1.5 - 10 µm 80 µm 15 µm 30 µm 5 µm

Figure 4.11: Step 6 is the application of the second mask, with critical dimension 5 µm. This step defines the active device region and the access window to the bottom electrode.

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Step	Process description	Cross-section after process
7	**Process**: Dry Etch **Machine**: AMS 200 **Material**: SiO_2 **Depth**: 50 nm	

Figure 4.12: Step 7 is the dry etching of the SiO_2 layer to reveal the bottom electrode, thus defining the device’s active region.

Step	Process description	Cross-section after process
8	**Process**: Sputtering **Machine**: Spider 600 **Material**: Ta_2O_5 **Thickness**: 15 nm	15 nm

Figure 4.13: Step 8 is the reactive sputtering of the Ta_2O_5 layer using Spider 600.

Step	Process description	Cross-section after process
9	**Process**: Photolithograp hy **Machine**: EVG 150 **Photoresist**: AZ 1512HS 1.1µm **Mask 3**: CD = 10 µm	5 µm 21.5 - 30 µm 105 µm

Figure 4.14: Step 9 is the deposition of PR to define the areas where Ta_2O_5 is to be etched.

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Step	Process description	Cross-section after process
10	**Process**: Dry Etch **Machine**: AMS 200 **Material**: Ta_2O_5 **Depth**: 15 nm	

Figure 4.15: Step 10 is the dry etching of the Ta_2O_5 layer.

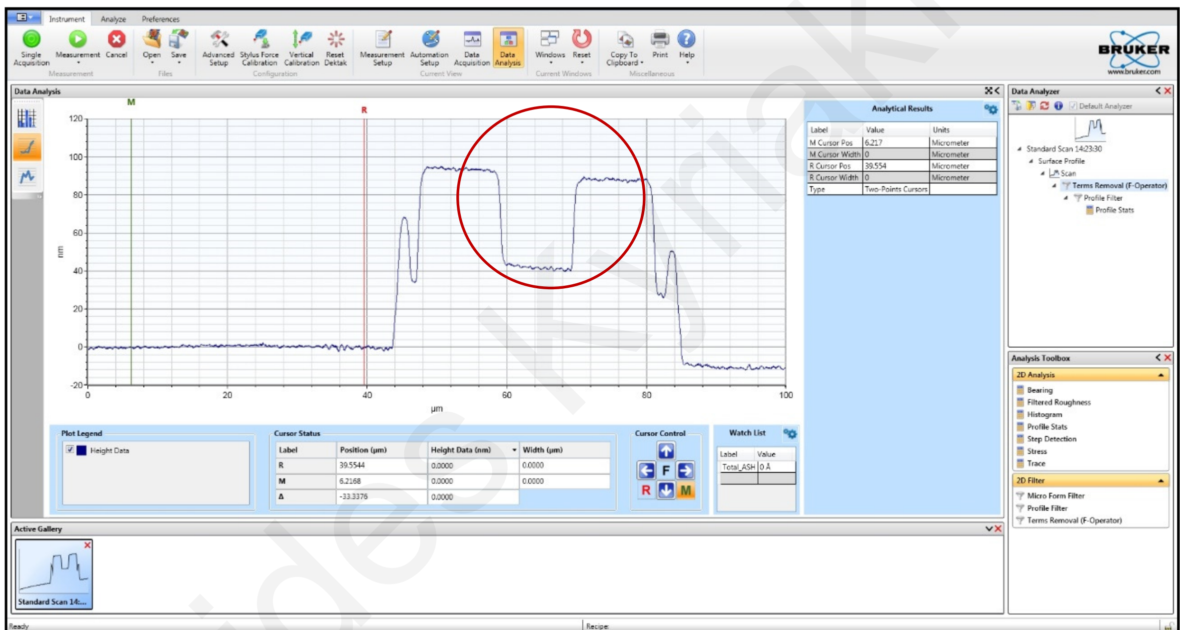

Figure 4.16: Profilometer analysis of a fabricated device after Step 10. The trench (circled) represents the device's active region, verifying the expected structure profile shown in Fig. 4.15. This ensures no overetching or underetching took place.

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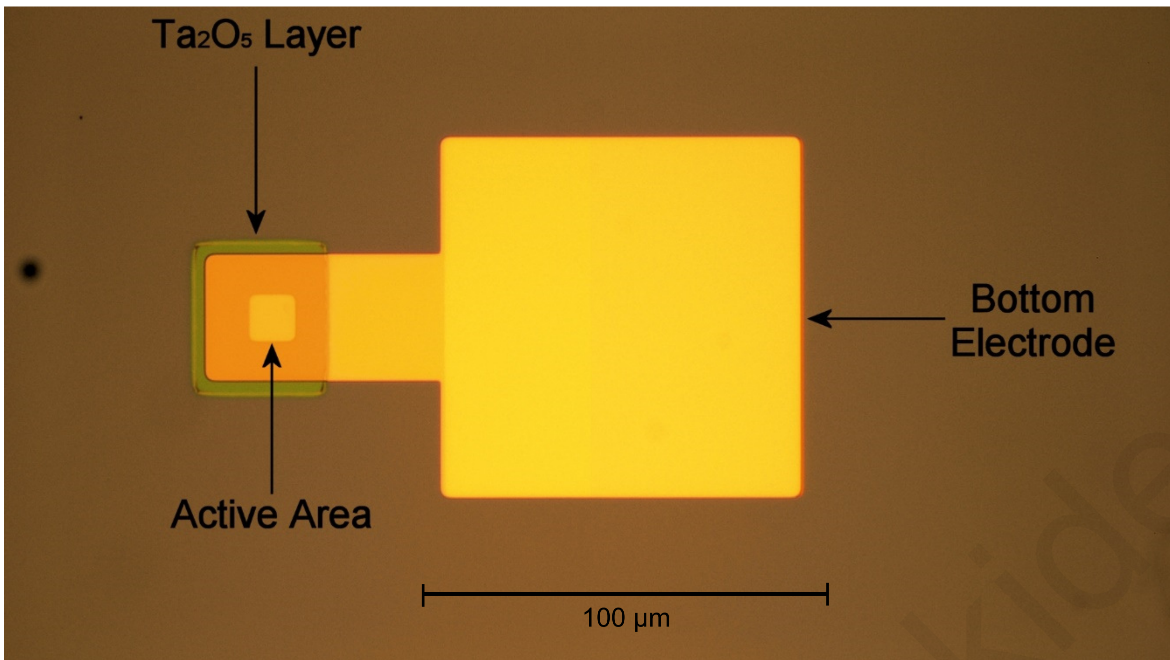

Figure 4.17: Microscope image of the device as intermediate verification after Step 10. The Ta_2O_5 layer is covering the device's active region on the left. The bottom electrode is visible on the right.

Step	Process description	Cross-section after process
11	**Process**: Photolithograp hy LOR **Machine**: EVG 150 **Photoresist**: LOR 400 nm + AZ 1512HS 1.1 µm **Mask 4**: CD = 10 µm	

Figure 4.18: Step 11 is the first part of the top electrode fabrication. LOR is deposited to define where the top electrode is to be lifted off.

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Step	Process description	Cross-section after process
12.1	**Process**: Metal Evaporation **Machine**: EVA 600 **Metal**: Cu **Thickness**: 50 nm	50 nm

Figure 4.19: Step 12.1 continues the LOR process, which involves the evaporation of two metals serving as the device's top electrode. In the first part, 50 nm-thick copper is evaporated using the EVA 600.

Step	Process description	Cross-section after process
12.2	**Process**: Metal Evaporation **Machine**: EVA 600 **Metal**: Au **Thickness**: 30 nm	30 nm

Figure 4.20: Step 12.2 is the second part of metal evaporation for the top electrode. Here, gold is evaporated using the EVA 600.

Step	Process description	Cross-section after process
13	**Process**: Lift-off **Machine**: Plade Solvent **Material**: Au/Cu	

Figure 4.21: Step 13 completes the LOR process. The LOR is chemically lifted in a wet bench, leaving behind the desired bilayer of Au/Cu.

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4.3.3 Fabrication results

The device is completed according to the structure shown in Fig. 4.22. To confirm whether the fabricated devices conformed to the design, microscope verification was performed. The results are shown in Figs. 4.23 - 4.27. Primarily two methods were employed: an optical microscope and a SEM.

Using an optical microscope, a top-level layout of a cell of devices, as shown in Fig. 4.23, and a detailed image of a single device, as shown in Fig. 4.24, were captured.

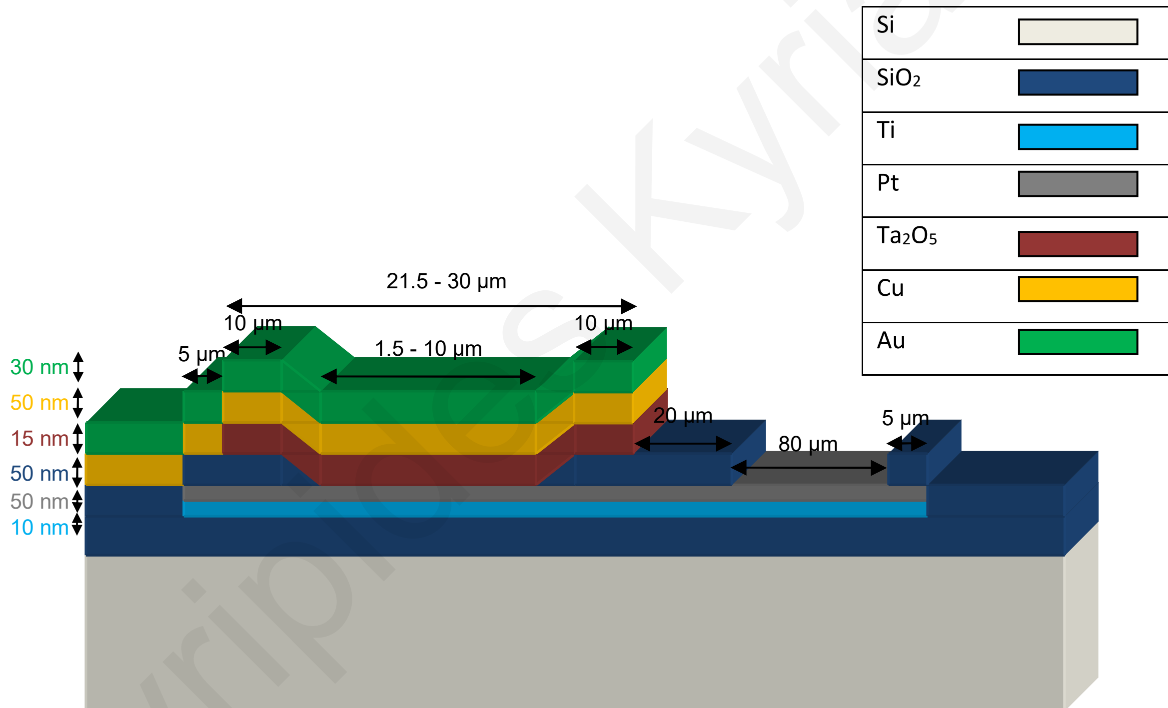

Figure 4.22: Representation of final fabricated Cu/Ta_2O_5 device. The layer thicknesses are colored in accordance with the respective materials for clarity.

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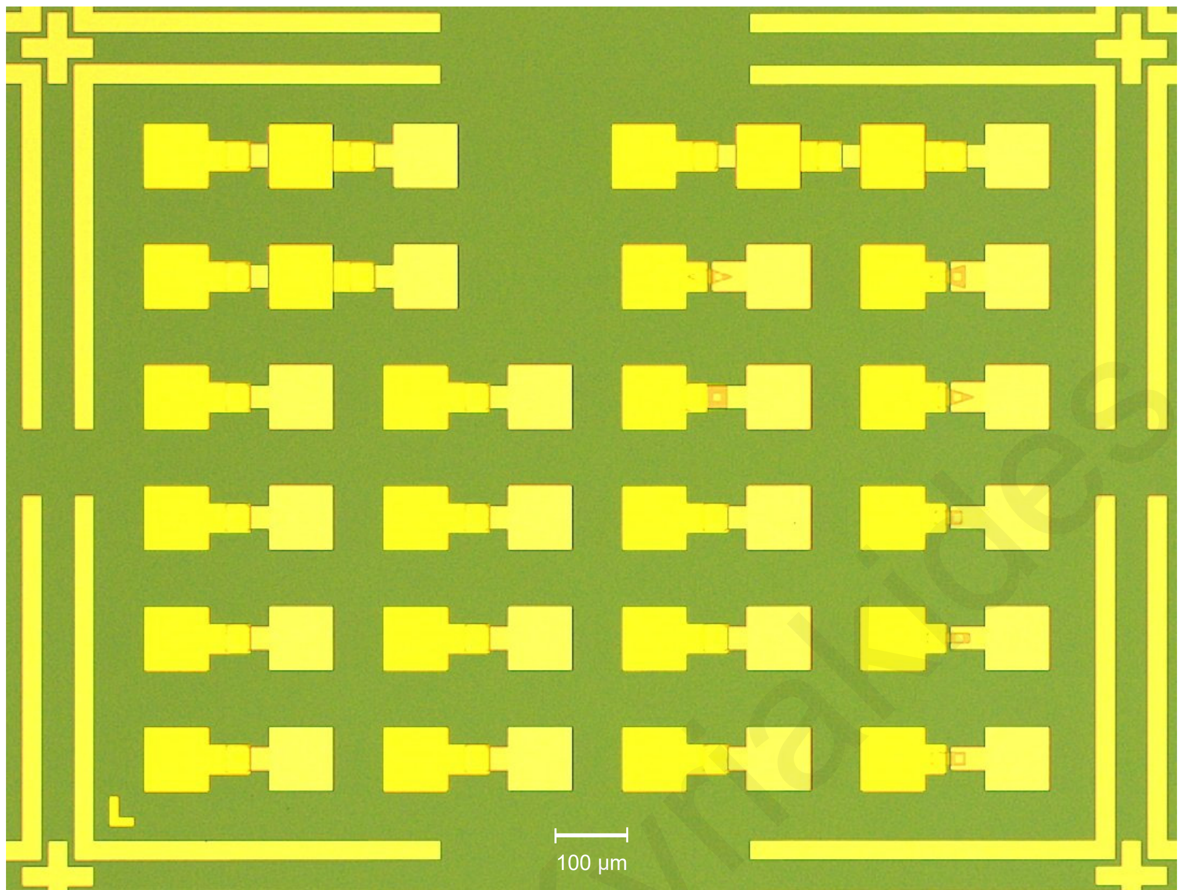

Figure 4.23: Microscope image of fabricated cell of Cu/Ta_2O_5 devices. Each cell contains a library of structures with geometrical variations.

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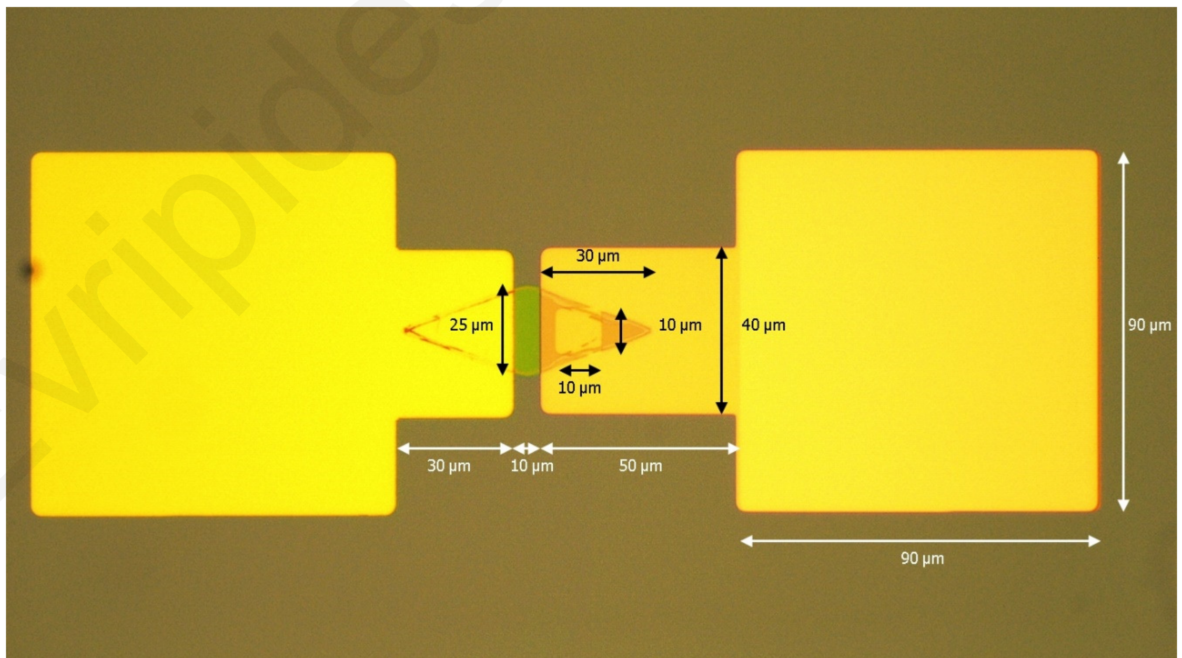

Figure 4.24: Microscope image of a single Cu/Ta_2O_5 device.

The SEM/FIB procedure was used to get cross-sectional images of the fabricated devices. The procedure starts with the deposition of a platinum layer to preserve the active region, as shown on the top image of Fig. 4.25. It is followed by etching of the area of interest using a focused ion beam. This is accomplished by series of etching steps of progressively smaller patterns, as shown on the bottom image of Fig. 4.25.

When the FIB tapered etching procedure has been completed, the SEM column is employed. At a sample inclination of 52°, the SEM can capture images of the "dissected" device. Images captured using aforementioned procedure are shown in Figs. 4.26 - 4.27. The observations can verify the correct deposition of layers, including accurate thickness measurements.

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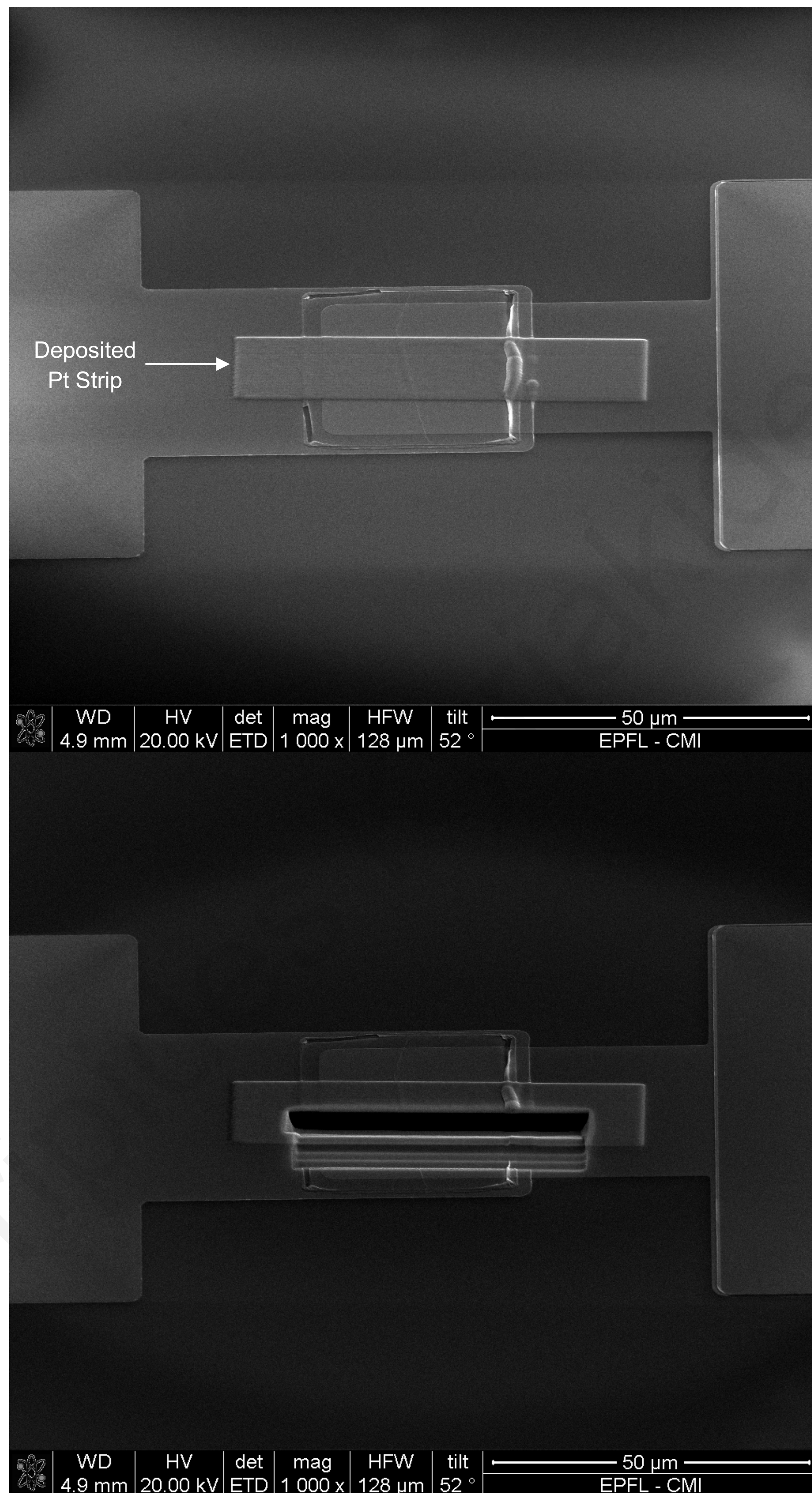

Figure 4.25: Top: Platinum deposition during FIB procedure shown as a horizontal strip across active device region. Bottom: Successive etching steps of smaller areas results in tapered etching of the active device region during the FIB procedure.

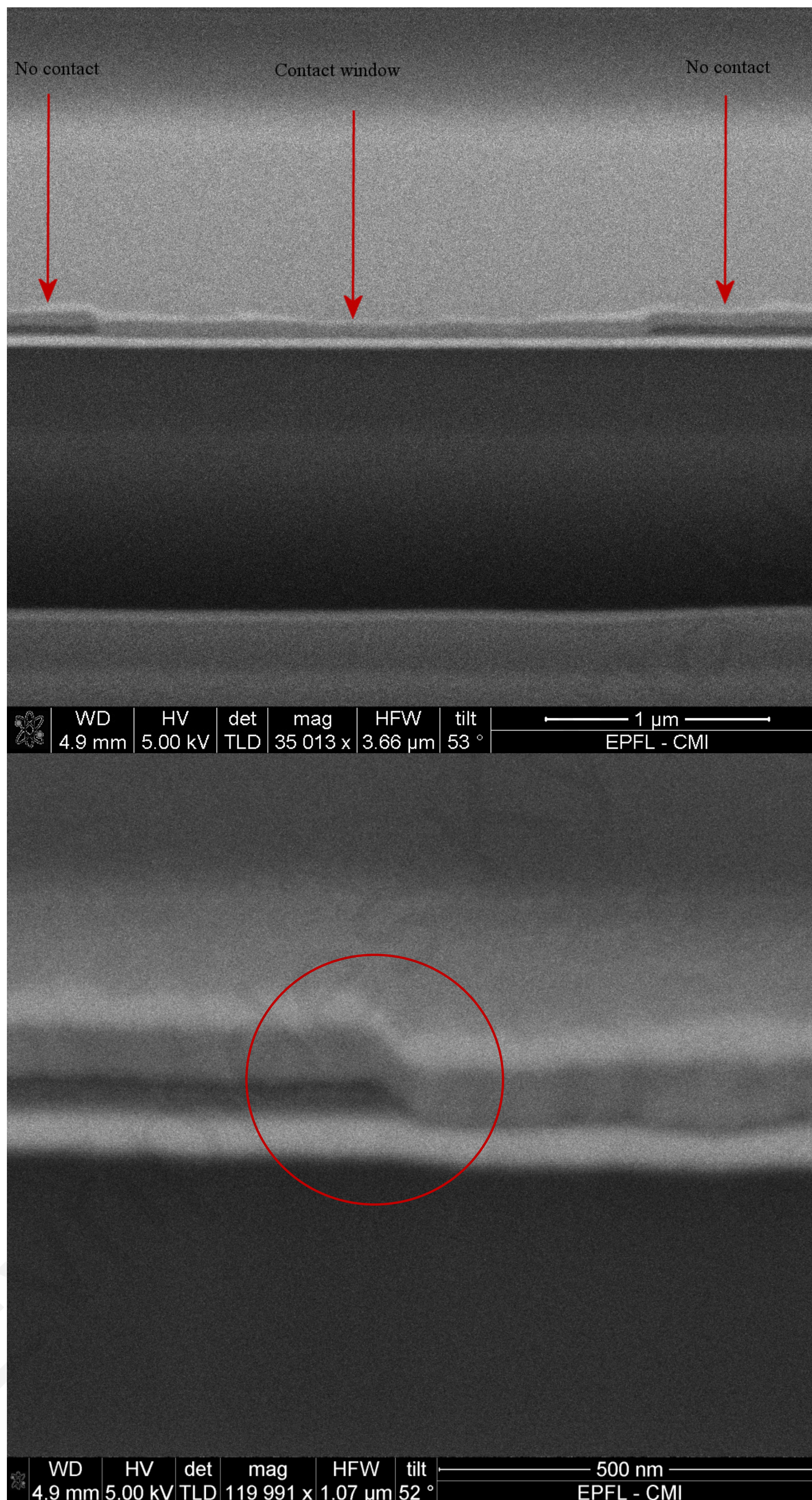

Figure 4.26: SEM/FIB image of a device cross-section. Top: Definition of the active device region. Bottom: The SiO_2 layer to the left of the junction edge (circled) acts as an interlayer dielectric between the Ta_2O_5 and platinum layers.

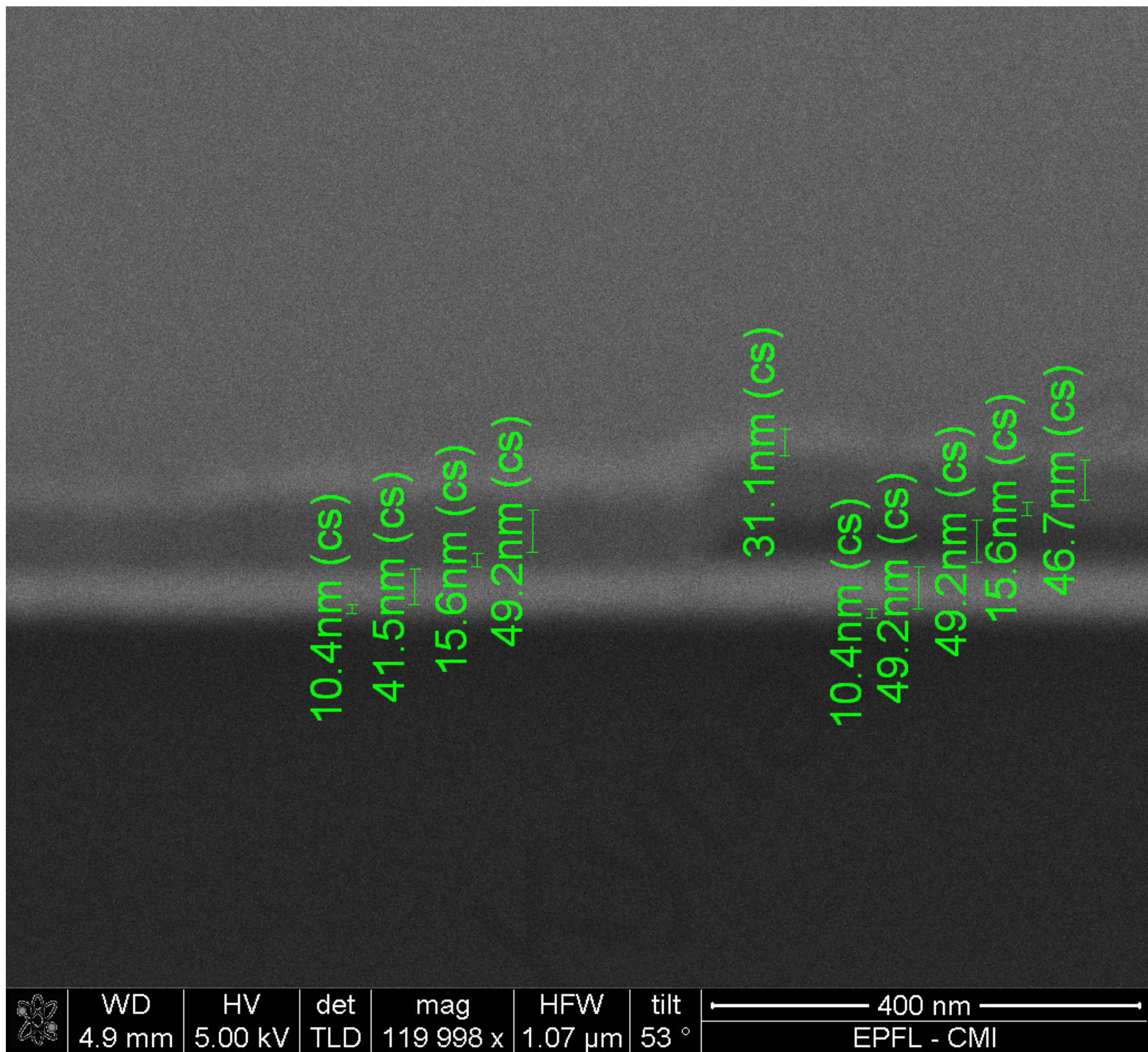

Figure 4.27: Verification of layer thicknesses becomes possible using the SEM imaging capabilities.

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4.3.4 Discussion

The critical failure mode of Cu/Ta_2O_5 device fabrication is the etching of the Ta_2O_5 layer. In this case, the Ta_2O_5 layer was initially overetched during a fabrication run. However, subsequent runs corrected the error and intermediate checks were introduced for validation. Following the dry etching step, a profile scan was performed to confirm the active region trench depth. SEM imaging at the end of the fabrication verified that the devices were completed according to specifications. As shown in the images above, the alignment and

thicknesses of the deposited layers were precise. Therefore, the fabrication of Cu/Ta_2O_5 is deemed successful.

Initial electrical characterization of the devices confirmed the elementary expected behavior. Initially the devices exhibit very high resistance resulting in picoamp-scale currents. Through electroforming, the devices exhibit switching behavior. The forming parameters were unknown at the time of fabrication. Initial trial-and-error attempts were later replaced by with the procedure detailed in the following chapter. However, the devices seemed to undergo electrical breakdown. The analysis of the electrochemical process takin place during device operation led to the use of current compliance to avoid breakdown. As expected, devices fabricated without top electrode could not be formed and showed no signs of hysteresis. This confirms the involvement of copper in device operation.

Since operation of the device involves ion movement and nucleation, high-resolution imaging can trace induced changes in the lattice. Hence, to confirm device operation, SEM/FIB imaging can be carried out on electroformed devices. This would show evidence of the filament creation and confirm the stated hypothesis, as shown later.

As, indicated earlier, the fabrication methods and materials used for the Cu/Ta_2O_5 device are CMOS compatible. This enables straight-forward integration with current processes in order to produce complete networks, such as those shown subsequently. It should also be noted the limits on device size are set by the need for contact pads and the lithography method. Although UV lithography was used for the fabrication of these devices, e-beam lithography could also be used for the smallest device feature, i.e. the active region. This lowers the resolution limit (< 10 nm) leading to the prospect of highly dense arrays. The active region size is thus investigated in the following chapter.

4.4 Characterization and modeling of Cu/Ta_2O_5 devices

Characterization of the Cu/Ta_2O_5 devices was initially conducted using a Signatone S-1160 probe station that allows a large number of devices on the wafer to be independently measured. The Signatone probes were connected to a Keithley 4200-SCS Parameter Analyzer to measure the electrical response of the devices to different stimuli. Behavior of

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the various geometries before and after electroforming has been investigated. The AC response from sinusoidal input and pulse excitation have also been examined.

The Cu/Ta_2O_5 devices, shown in Fig. 4.28, rely on a filament formation to vary conductivity. Cu^+ cations diffuse into the insulating Ta_2O_5 layer as a result of the electric potential gradient, aided by the solubility of Cu^+ cations in Ta_2O_5 and limited by the diffusion coefficient of Cu^+ cations in Ta_2O_5 [107]. A high concentration of Cu^+ cations at the Ta_2O_5/Pt interface causes nucleation through a reduction reaction, which in turn leads to the formation of a conductive filament of copper atoms extending between the two electrodes. The forming and dissolution of this conductive path results in the memristive behavior observed [106, 107].

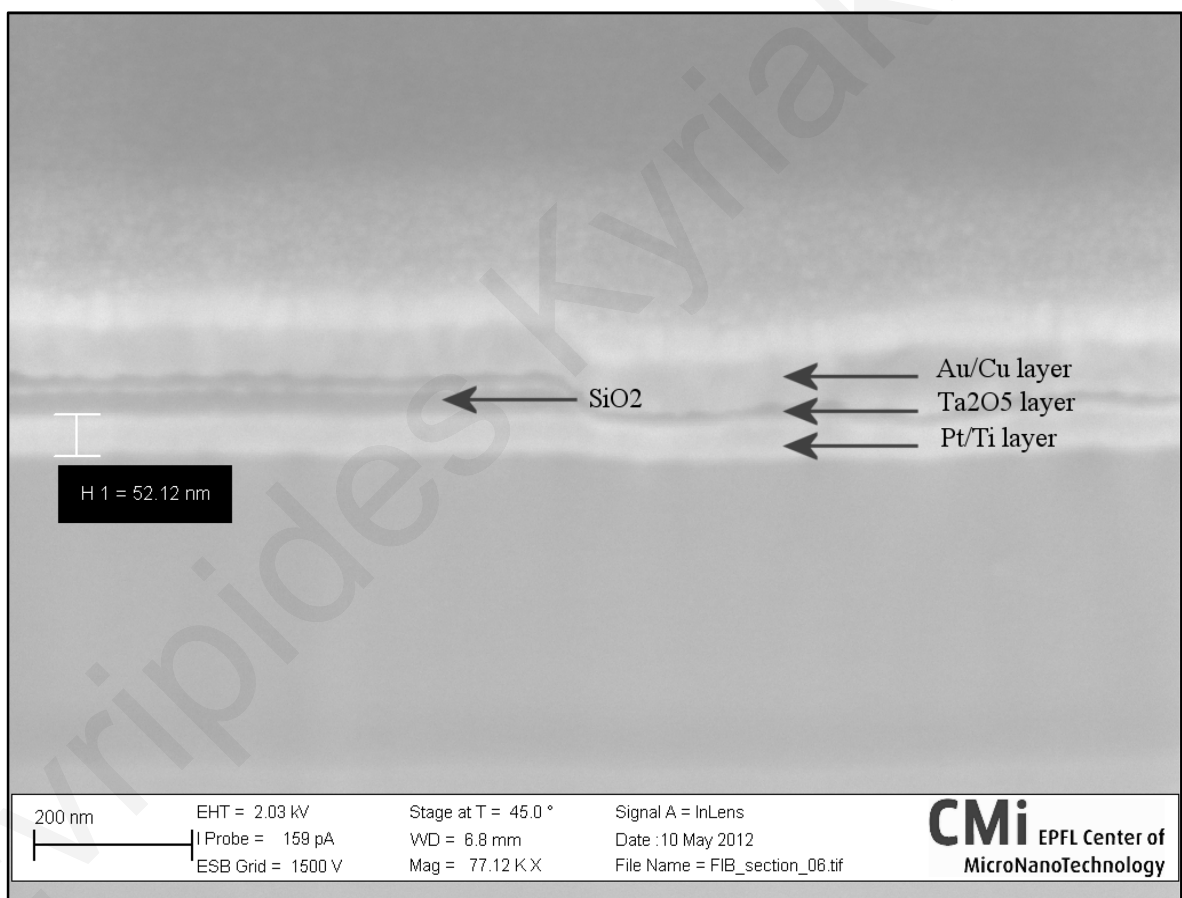

Figure 4.28: Junction edge and material designation taken through a SEM. The structure is believed to owe its behavior to electrochemical processes taking place in the Ta_2O_5 layer.

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It was previously assumed that the device in question required a forming step for the initial filament formation to behave like a resistive switch or memristor. The forming process involves a large voltage being applied to the top electrode to generate the electric field required for the Cu^+ cation diffusion. The voltage required for the forming of the fabricated devices can be above 5 V, a value that entails a high voltage supply. If this step is to be carried out without using external sources on a "learning chip", substantial additional circuitry will be required on-chip, in addition to the requirement of a costly high voltage technology. Thus, the forming process is commercially unattractive. It is hereby shown that Cu/Ta_2O_5 devices can also be used at below-forming voltages as a bipolar hemi-memristor, without compromising the hysteretic behavior required in biomimetic circuits. Thus, two regions of operation are defined: pre-forming and post-forming.

In the post-forming domain, AC measurements are performed to investigate frequency response. Additionally, the devices are subjected to pulse measurements to enable their use spiking neural networks. With the aim of modeling the devices, the threshold voltage is defined and measured.

The fabricated devices' forming process, as well as their pre-forming and post-forming behavior, are hereby presented. The threshold voltage, pulse, and AC measurements presented in the subsequent sections, lead up to the device model. Behavioral modeling was completed for the Cu/Ta_2O_5 device in a similar manner to that previously reported for the NiTi device. The electrical measurements were used in conjunction with ab initio calculations to create a model in Verilog-A HDL in Cadence Virtuoso environment.

4.4.1 Methods

The electrical measurements were performed at a constant ambient temperature of 26 °C and humidity of 40%. A Keithley 4200-SCS, shown in Appendix B, with femtoamp resolution was used to source voltage and measure current through the devices. The probe station used was a Signatone 1160, shown in Appendix B. The fabricated wafer was placed on the 6 in probe station chuck and probed using triaxial cables extending from the Keithley Source Measurement Units (SMUs) to the probe tips. The probe tips touch down on the devices' 100 μm × 100 μm pads. The set-up is shown in Fig. 4.29.

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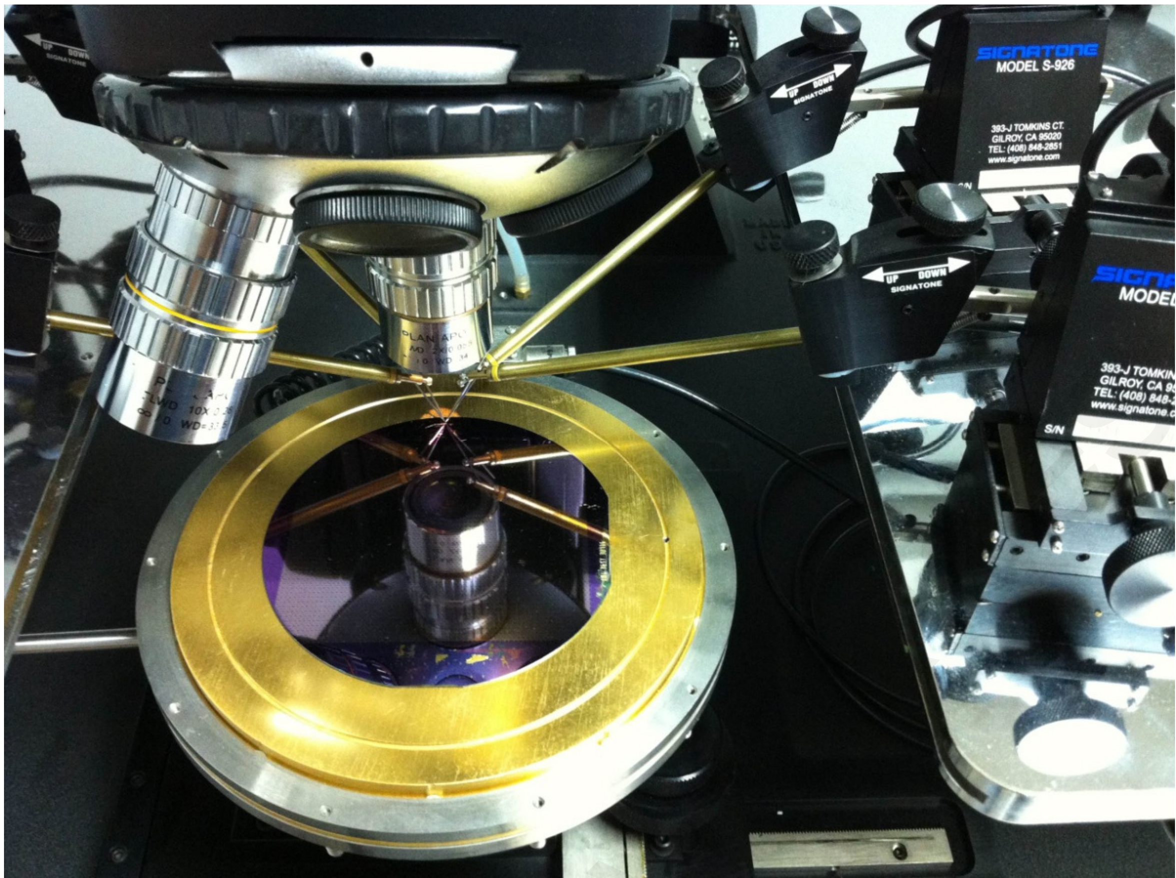

Figure 4.29: Wafer during characterization at the Signatone 1160 Probe Station. Four tips in total allow contact to the 100 μm × 100 μm device pads.

Although the high-precision characterization systems described thus far (Keithley 4200-SCS, Signatone S-1160) give resolution of up to femtoamp scale, they are limited in the frequency spectrum. To overcome any such limitations, a custom measurement module was assembled. The setup, comprising a transimpedance amplifier, is illustrated in Fig. 4.30. This system is built around an OPA128 op-amp. Negative feedback through three resistors, with only one active at a time, gives a voltage output from a current input. Using high resistances, it becomes possible to translate very low currents to a standard voltage range with the high precision offered by the OPA128 op-amp. The setup uses two battery sources of +15 V and -15 V to ensure low variation in the supply. The low-level current input uses triaxial configuration to limit losses. The module is also fully enclosed in a metal casing to insulate it from external noise sources, as shown in Appendix B.

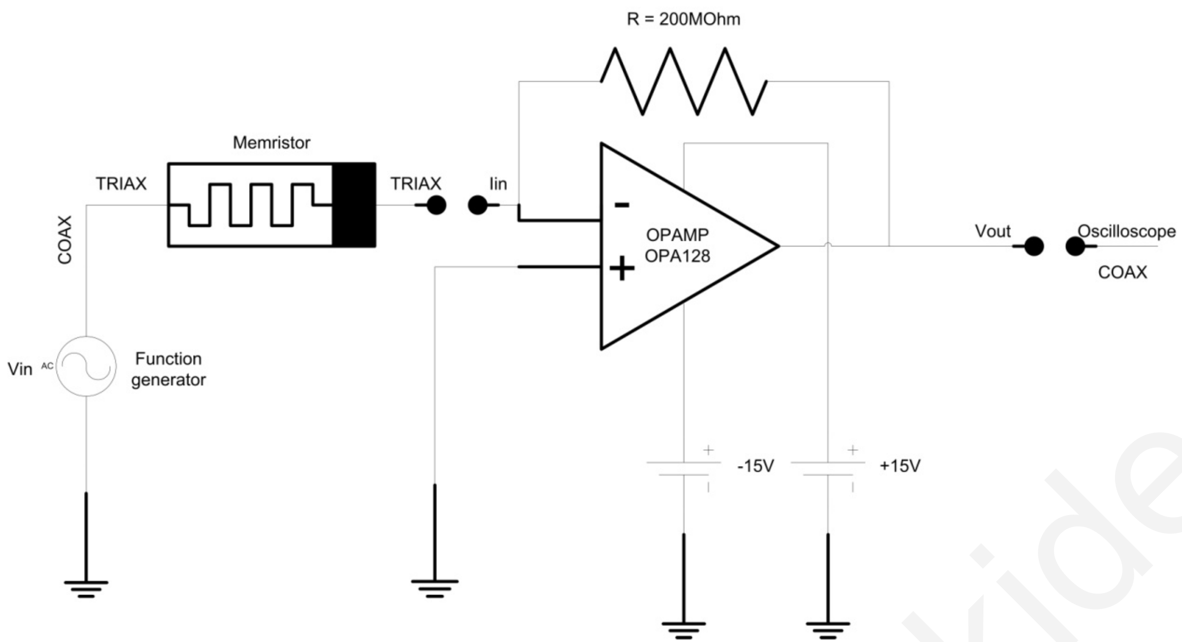

Figure 4.30: Block diagram of custom-made measurement module.

This module's output can be connected to a DMM for measurement. A National Instruments PCI-4462 was chosen to determine the output voltage. The NI PCI-4462, shown in Appendix B, is a high-accuracy data acquisition board. It features 24-bit sigma-delta Analog-to-Digital Converters (ADCs). It also features 118 dB dynamic range and six gain settings for input ranges from ±316 mV to 42.4 V. The analog inputs can be sampled at up to 204.8 kS/s.

4.4.2 Pre-forming region

Choosing a low voltage operation region due to power consumption considerations, the devices were taken through voltage sweeps of ±3.3 V (Fig. 4.31), well below the forming threshold. The hysteresis effect is very consistent, through a variety of device geometries with very high repeatability.

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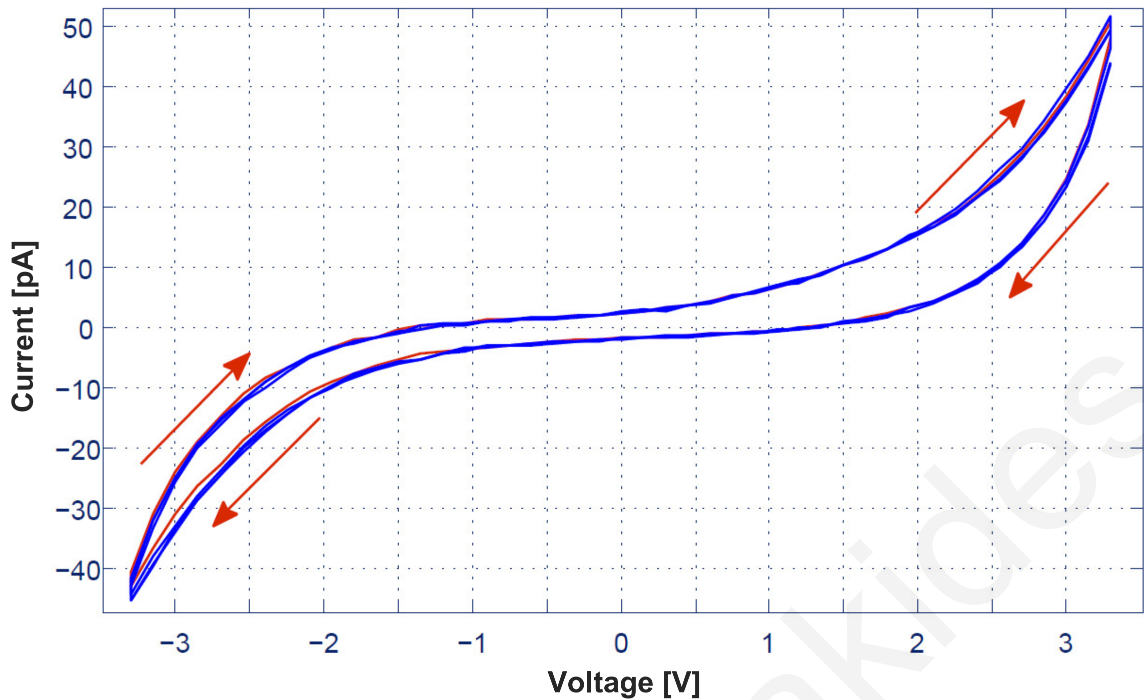

Figure 4.31: Pre-forming I-V hysteresis loop comprising four sweeps.

In order to probe into the mechanisms causing this hysteretic behavior, some devices that omitted the top electrode layer copper layer were designed. In these cases the resistivity of the Ta_2O_5/Pt heterostructure did not exhibit any memristive behavior. This led to the deduction that the observed behavior of the full device is based on Cu^+ ionic diffusion. To investigate this assumption further, cyclic voltammetry experiments with varying triangular voltage sweep rates (0.05 - 0.10 Hz) were conducted. Frequency measurements clearly show a dependence of peak conductivity and hysteresis on frequency, as shown in Fig. 4.32; however these show an opposite trend to an idealized memristor, hence the use of the term "hemi-memristor" [108]. Furthermore, increasing sweep rates yield increasing peak currents. More specifically, the Cottrell equation is verified in peak current vs. sweep rate, as shown below.

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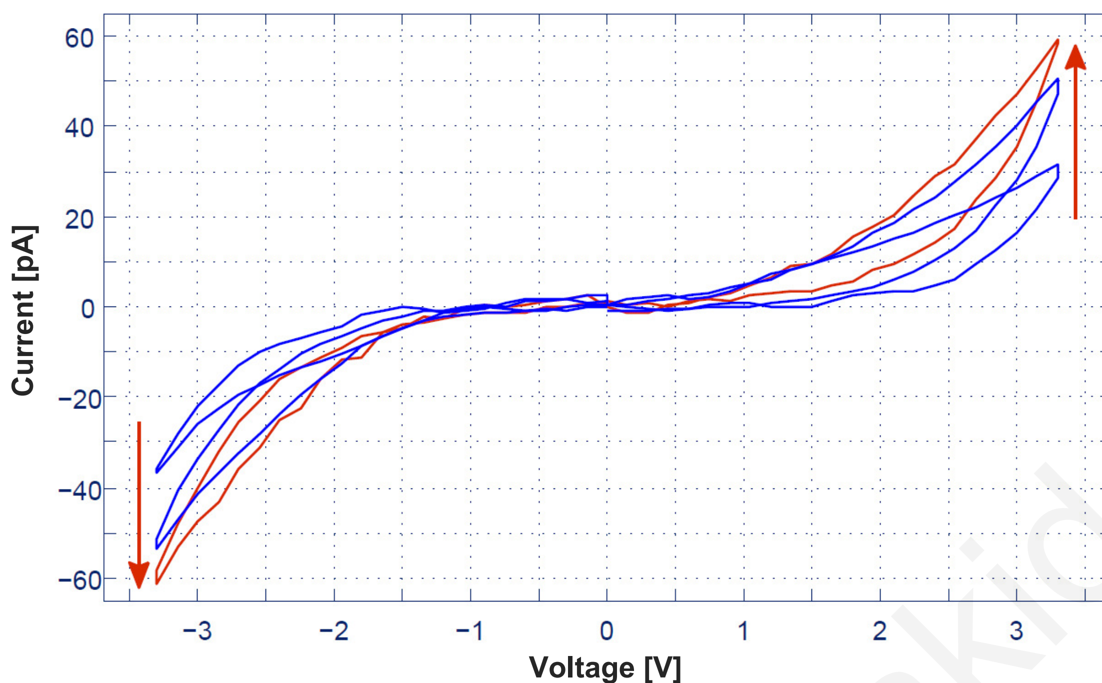

Figure 4.32: Sweep frequency variation. Red arrows indicate increasing frequency.

The Cottrell equation is primarily used in electrochemistry to calculate the change in electric current with respect to time in controlled potential experiments. Though mostly used in potential-step setups, it is also useful in voltage ramp experiments. The equation for a planar electrode is:

$$i = \frac{n\,F\,A\,c_j^0\,\sqrt{D_j}}{\sqrt{\pi\,t}} \tag{4.1}$$

where,

i = current [A]

n = number of electrons (to reduce/oxidize one molecule of analyte j)

F = Faraday constant [96,485 $C \cdot mol^{-1}$]

A = area of (planar) electrode [cm^2]

c_j^0 = initial concentration of reducible analyte j [$mol \cdot cm^{-3}$]

D_j = diffusion coefficient for species j [$cm^2 \cdot s^{-1}$]

t = time [s].

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Defining k to replace the constants for a given system (n, F, A, c_j^0, D_j, π), the Cottrell equation can be written as

$$i = k\, t^{-1/2} \tag{4.2}$$

and $t^{-1/2}$ can be replaced by $\sqrt{(Scan\ Rate)}$.

If the current is limited by the diffusion of the analyte species to the electrode surface, then the peak current will be proportional to the square root of the scan rate. Tab. 4.2 lists measurements of scan rates and peak currents. Plotting the peak current versus the square root of the scan rate (Fig. 4.33) reveals the type of relationship between the two variables. The plot of Fig. 4.33, which includes two sets of data, reveals a linear relationship $Peak\ Current$ vs. $\sqrt{(Scan\ Rate)}$ indicating a diffusion-limited redox reaction.

√(Scan Rate) [1/√s]	Peak Current [pA]	√(Scan Rate) [1/√s]	Peak Current [pA]
0.589256	33.45	0.576390	31.44
0.492665	30.28	0.482805	28.79
0.437688	28.77	0.429141	27.28
0.398094	27.49	0.389841	26.25
0.367359	26.4	0.359908	25.27
0.345857	25.87	0.335957	24.91
0.305566	24.89	0.299476	23.92
0.278315	24.05	0.272874	23.29

Table 4.2: Two sets of scan rate and peak current measurements in pre-forming region.

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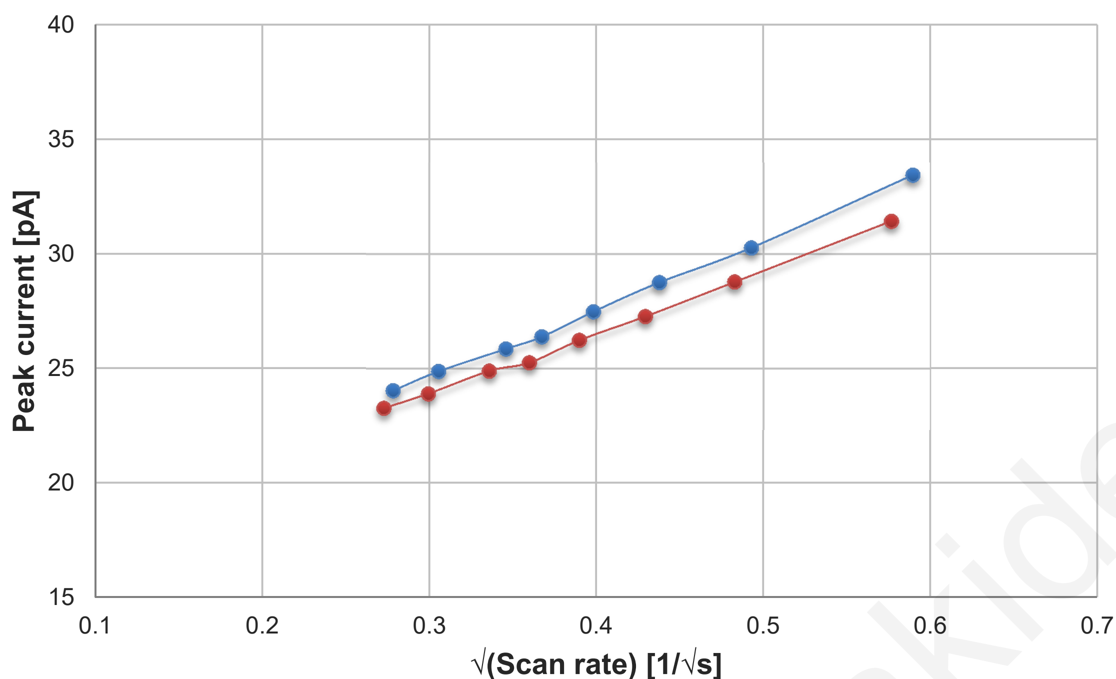

Figure 4.33: Plot of peak current versus square root of scan rate from Tab. 4.2.

Taking the above into account, along with the lack of current peaks in the voltage sweeps at the copper standard redox potentials of 0.153 V and 0.521 V, it is evident that no redox reactions take place [109]. Moreover, the slightly asymmetric I-V curve further attests to diffusion between dissimilar electrodes. Hence, the low currents, limited by the tantalum oxide dielectric, ensure the electrochemical reaction at the platinum bottom electrode does not occur [107], thereby preventing the subsequent Cu^+ nucleation and filament creation from taking place. Therefore, in this region of operation only the Cu^+ ion migration mechanism through the solid electrolyte layer is observed. This matches the expected behavior at below-forming voltages and could account for the non-zero current at 0 V, as explained below.

With the formation of the filament mentioned previously and described in detail later, the dominant source of charge transport is electron tunneling. However, with the absence of necessary conditions for filament formation in the pre-forming region, filaments cannot be created. Therefore, in this region, an electric field is present in the electrolyte layer which is responsible for the Cu^+ ionic transport. This field is also responsible for a capacitive effect in the device, which in this region approximates a capacitor through its metal-insulator-metal structure. This gives rise to the impedance responsible for the lack of pinched hysteresis loop in the pre-forming region, as shown in Fig. 4.31.

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To further investigate the transient behavior of the devices after the removal of a voltage stimulus, the current across the devices was monitored after an applied voltage was removed. The voltage initially at 0 V, is increased at 1 V/s, reaching a constant level of 2 V and then instantly moving to 0 V. The graph in Fig. 4.34 depicts the applied voltage and measured current across the device as a function of time. It is apparent from the graph that the device shows evidence of two transient characteristics: (a) an initial oversaturation of Cu^+ exhibited by the decreasing current for a constant voltage of 2 V [106], and (b) the discharge of a stored charge once the voltage returns to 0 V. The latter characteristic illustrates the mechanism behind the nonzero current observed at zero voltage during I-V sweeps.

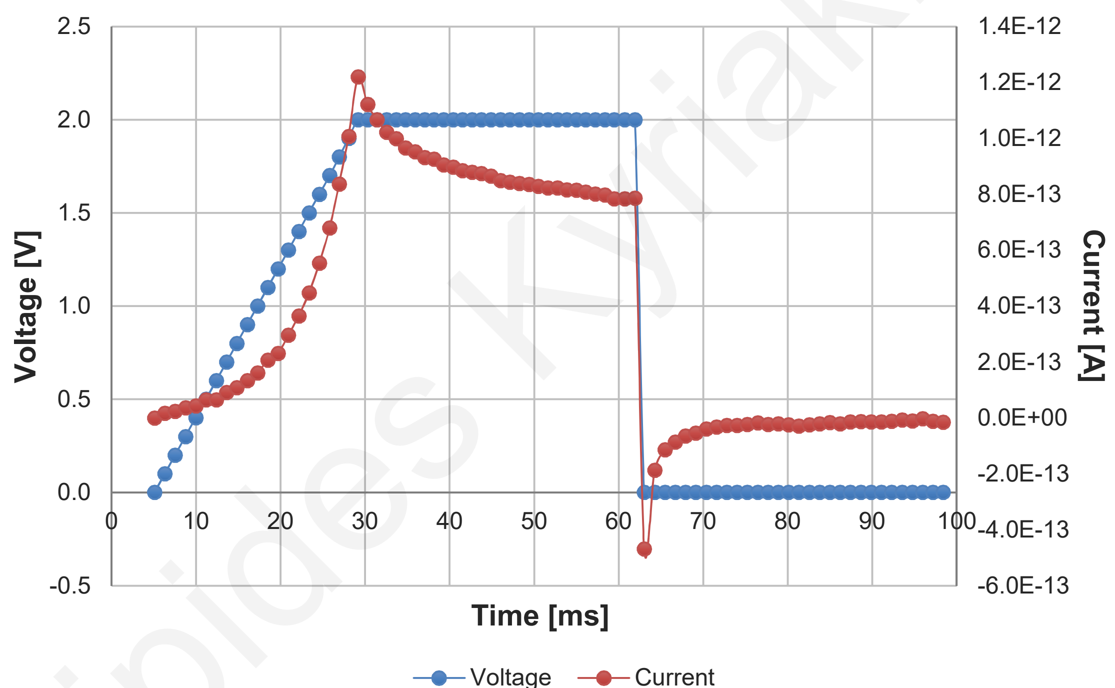

Figure 4.34: Current and voltage across device as a function of time illustrating current discharge.

Different devices were fabricated in order to investigate the effect of active shape/area on device behavior. As shown in Fig. 4.35, each device in a cell had a different active device shape and area. These variations are listed in Tab. 4.3 and include rectangular and circular apertures. Varying aperture areas were included. Alternatively, devices have been designed to feature active areas which are split in two, whereas others have no overlap between top and bottom electrode through lateral positioning of the two layers. This was

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modified through the SiO_2 layer that confines the contact between Ta_2O_5 and Cu. The aperture type and area were investigated through peak current measurements in the pre-forming region. The devices in each cell were subjected to the same measurement procedure. The comparison of peak currents is logged in Tab. 4.3 and plotted in Fig. 4.36.

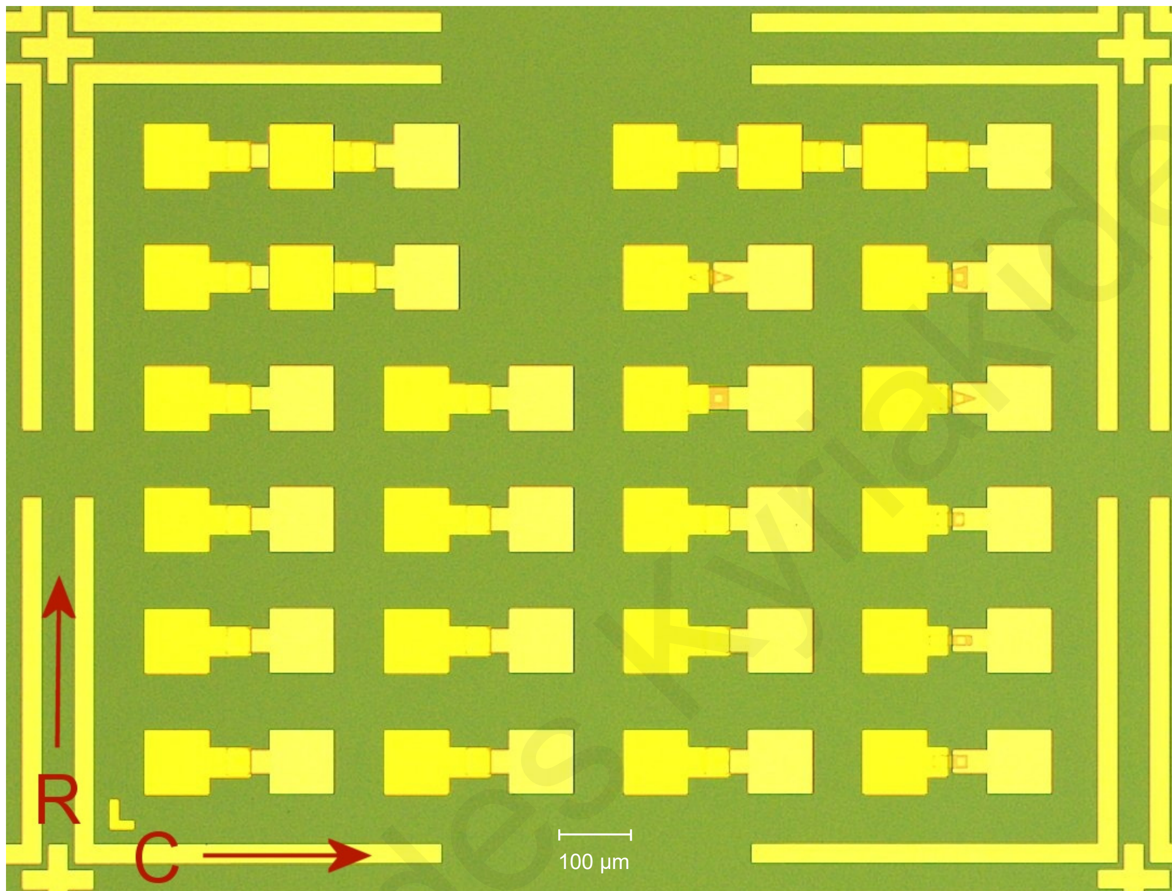

Figure 4.35: Microscope image of fabricated "cell" of Cu/Ta_2O_5 devices. Each "cell" contains a library of structures with geometrical variations. The naming convention follows C for column left to right and R for row bottom to top, e.g. the bottom left device is designated as C1R1.

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	C1R1	C1R2	C1R3	C1R4	C2R1	C2R2	C2R3	C2R4	C3R1	C3R2	C3R3
I [pA]	12.57	12.79	11.91	12.84	10.05	10.49	10.85	9.04	6.94	8.68	6.96
I [pA]	35.41	32.70	28.38	34.06	27.24	22.21	27.33	29.22	21.41	22.98	21.67
I [pA]	35.85	34.07	33.25	35.11	30.15	28.84	33.13	28.38	33.89	38.73	36.82
I [pA]	34.78	16.37	17.55	17.78	8.69	21.48	26.52	19.52	19.61	23.20	27.33
I [pA]	30.94	28.85	31.99	28.55	27.01	33.95	27.26	30.21	31.33	29.87	28.85
Av/ge [pA]	29.91	24.96	24.62	25.67	20.63	23.39	25.02	23.27	22.64	24.69	24.33
Median [pA]	34.78	28.85	28.38	28.55	27.01	22.21	27.26	28.38	21.41	23.20	27.33
Dim/ns [μm]	10x10	7x7	4x4	3x3	2x2	1.5x1.5	d=8	d=4	d=2	4x4 x2	2x2 x2
Area [μm]	100.00	49.00	16.00	9.00	4.00	2.25	50.27	12.57	3.14	32.00	8.00

Table 4.3: Peak current measurements for Cu/Ta_2O_5 devices in pre-forming region. Five measurements were made for each device. Their average and median is calculated. The aperture dimensions and area are listed for each device type.

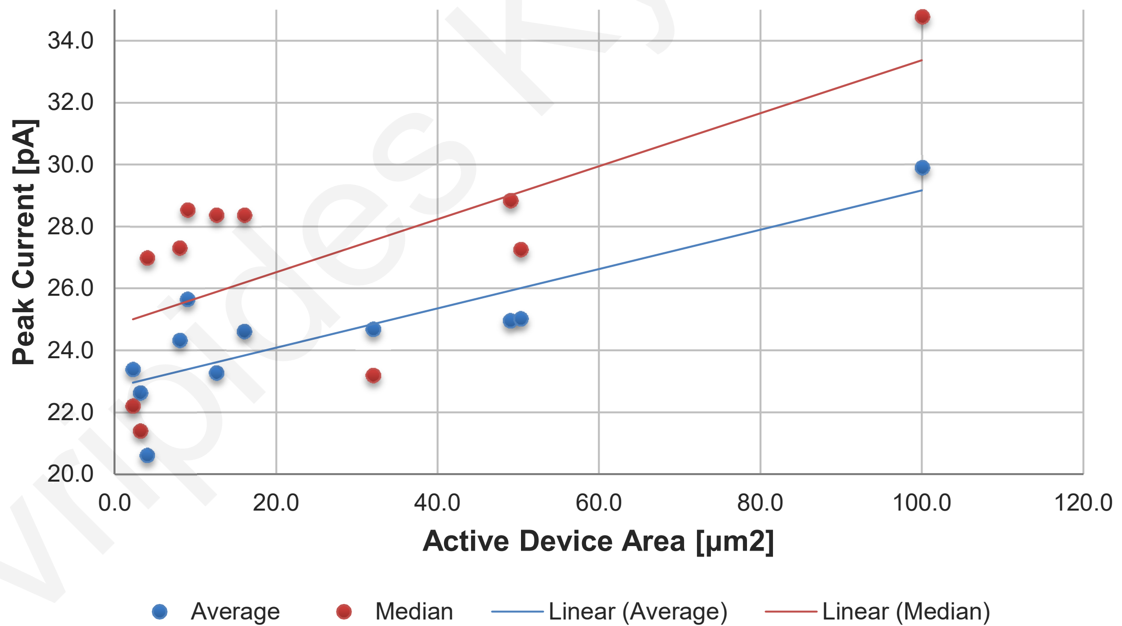

Figure 4.36: Chart of peak current versus active device area for devices in Tab. 4.3. Blue markers indicate average values, whereas red markers indicate median values. A linear regression fit is shown for each set of data.

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The chart in Fig. 4.36 plots peak current in pre-forming I-V sweeps for each device in a fabricated cell. It includes the average of five measurements on each type of device and the median. Devices connected in series (C1R5, C1R6, and C3R6) are individually identical to C1R1 and thus were not included in the specific measurements. Devices with lateral positioning of top and bottom electrodes (C3R4, C3R5, C4R1, C4R2, C4R3, C4R4, and C4R5) showed no measurable conductance. Linear regression is attempted on the data collected from overlapping devices to explore the trend. The coefficient of determination was calculated as $R^2 = 0.70$ for the average and $R^2 = 0.48$ for the median. Although a trend can be perceived, a correlation between active device shape/area and pre-forming conductivity cannot be safely established, particularly taking into account the coefficients of determination.

4.4.3 Forming process

The device forming procedure involves the application of a voltage in the range of 2 - 12 V to form the conductive filament within the dielectric sheet. The voltage being applied to the top electrode generates the electric field required for the Cu^+ cation diffusion. Cu^+ cations diffuse into the insulating Ta_2O_5 layer under the applied electric field. A high concentration of Cu^+ cations at the Ta_2O_5/Pt interface causes nucleation through a reduction reaction. This drives the formation of a conductive filament consisting of copper atoms extending from the bottom to the top electrode. This process is best illustrated through the current and voltage across the device as forming takes place, as shown in Fig. 4.37.

In order to define the forming conditions, namely, voltage, current, and application time, pertinent to the fabricated devices, value levels deduced from the relevant bibliography were used. Hence, forming voltage of 12 V and corresponding compliance current of 1.5 nA were used. However, the devices were undergoing hard-breakdown - an undesirable and irreversible process that results in Ohmic behavior. The region of operation was therefore reduced until a soft-breakdown - a process that brings the device to a state that allows switching - took place. To this end, the lowest voltage levels suggested in the bibliography, namely, 2 V, were initially employed. Through a stepwise increase, the optimal conditions of 4.69 V and 225 pA were arrived at, as explained below. Reverse

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polarity forming negative voltages did not succeed in forming the devices, as expected from the relevant bibliography.

Fig. 4.37 shows a typical I-V curve during device forming. At 80 pA a sudden increase in current takes place. The compliance current is roughly three times the current at that voltage. Assuming a near vertical increase in current, the forming voltage is defined to be the voltage level where the jump in current takes place.

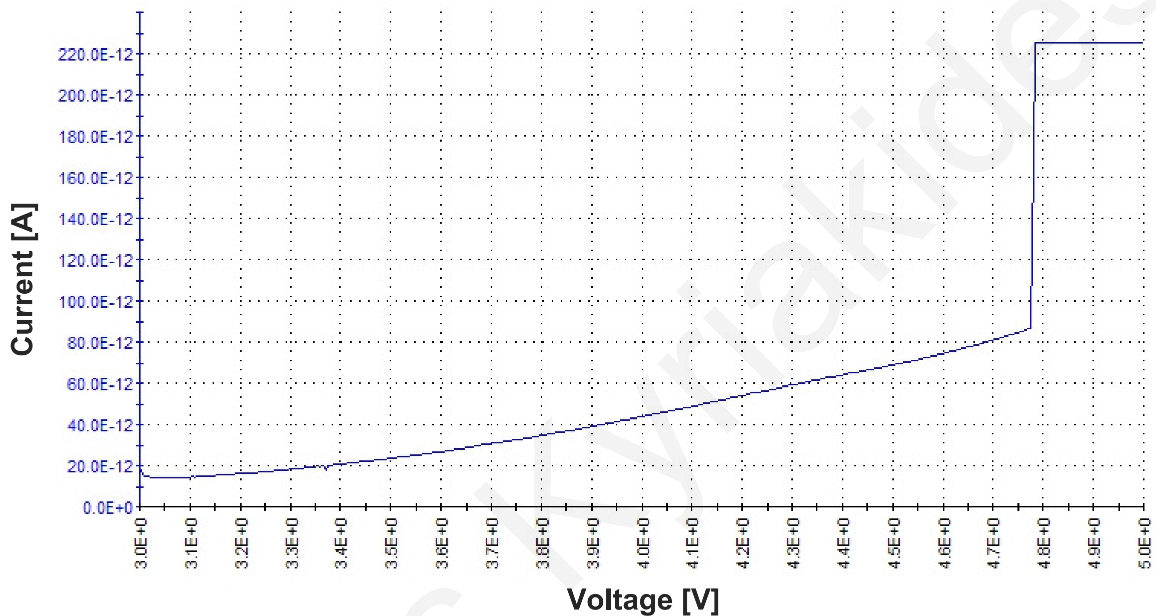

Figure 4.37: Typical I-V curve during device forming.

After recursive testing of the forming conditions required, the optimal parameters were conclusively defined as follows: A slow voltage sweep with a step of 5 mV (at an average rate of approximately 6 samples/second) and spanning from 3.5 to 5.5 V is applied to the top electrode. The compliance current is set at 225 pA. When compliance is reached, at an average value of 4.69 V, a sudden increase in current indicates, as shown in Fig. 4.37, that the devices have been formed. This signifies that the Cu filament has reached the Cu electrode interface.

However, stopping the forming process immediately after forming takes place is not always creating sustainable forming. The dissolution of the filament relies heavily on thermal effects and the creation of the filament relies on a nucleation process that increases the filament diameter with time. It is therefore assumed that the nano-bridge created was not wide enough in diameter for it to be sustained through subsequent cycling. On the other

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hand, a filament too wide in diameter would result in an indestructible filament that would show Ohmic rather than switching behavior [110]. Thus, the compliance current continued to be applied for a period of time after compliance was reached in order to create a filament that was thick enough to sustain repetitive cycling, yet thin enough to allow switching. This hold period was defined empirically as 16 s.

The exact voltage at which forming takes place varies between devices. This can be attributed to the scales involved - the dielectric layer is 15 nm in the vertical direction - and the fabrication variations are inevitable in microelectronics fabrication. This is illustrated in Fig. 4.38, which displays a histogram of the voltage necessary for 225 pA to be reached. Evidently, the devices form predominantly at a voltage ranging between 4.5 and 4.8 V. The mean value was 4.69 V with standard deviation 0.239 V. This voltage application process has a duration of ~2 min.

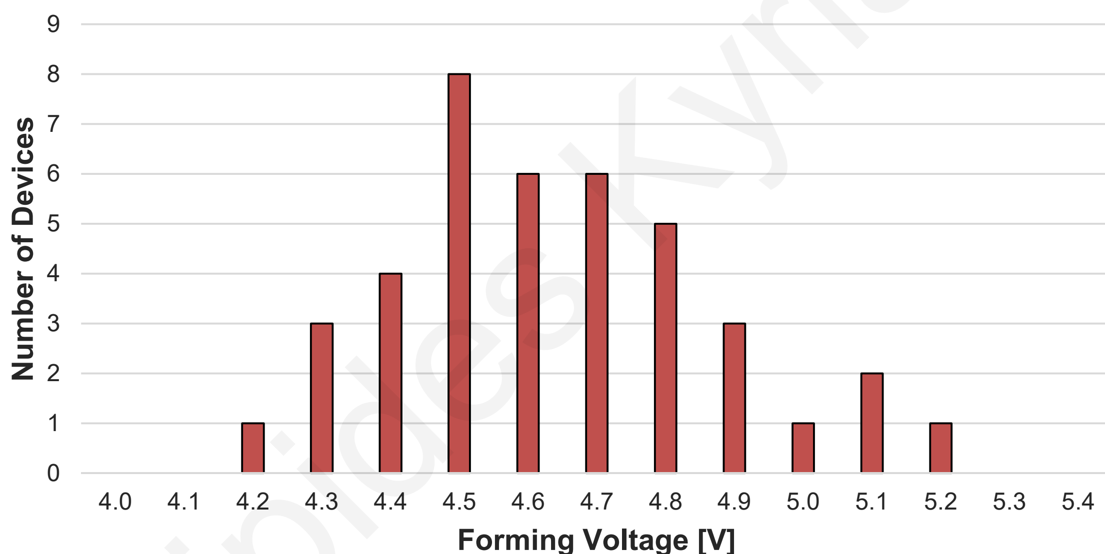

Figure 4.38: Forming voltage histogram. The mean value was 4.69 V with standard deviation 0.239 V.

A Field Emission Scanning Electron Microscope (FESEM) image of the filament extending in the dielectric layer between the two metals is shown in Fig. 4.39.

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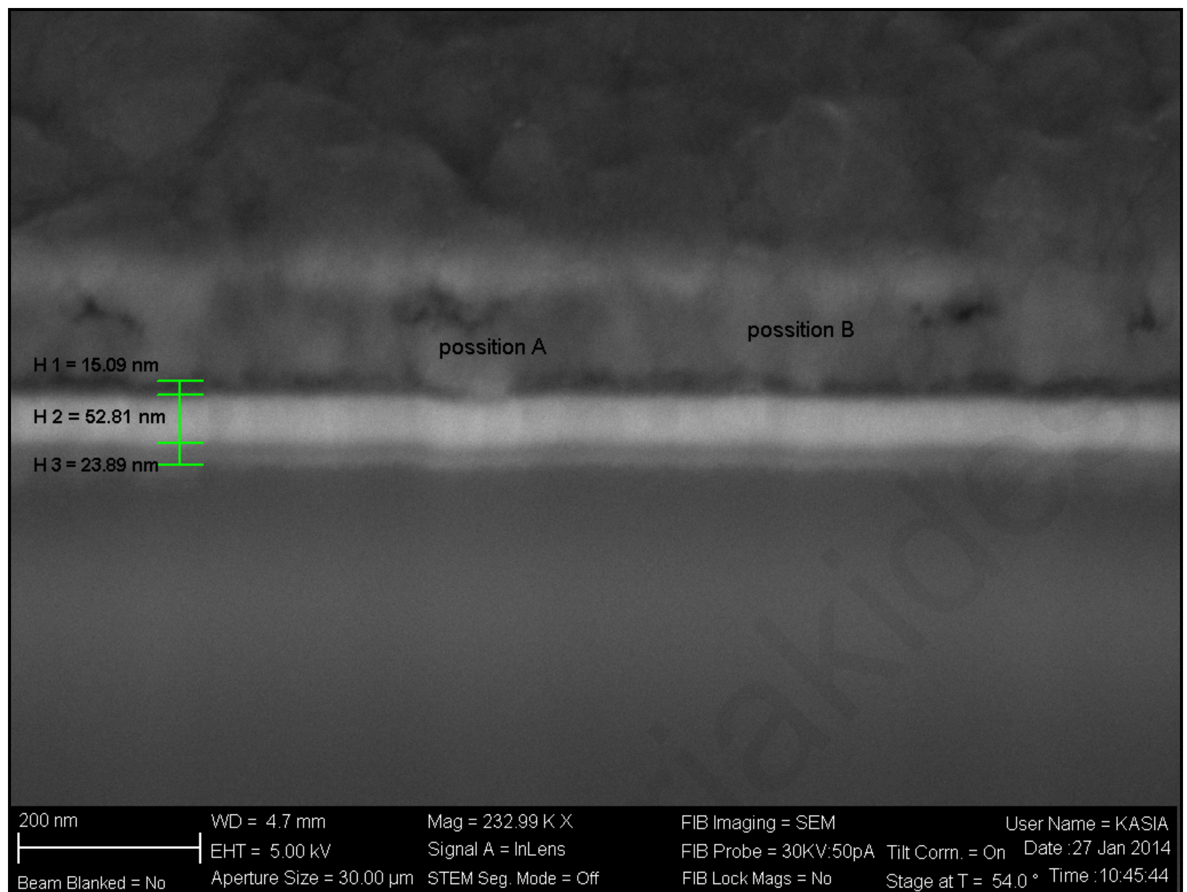

Figure 4.39: FIB/FESEM image of copper filament formed in the Ta_2O_5 layer. The copper filament extending from the top to the bottom electrode is visible in positions A and B.

4.4.4 Post-forming region

Once formed, the devices under investigation exhibit memristor characteristics. Voltage sweeps reveal the pinched hysteresis loop, shown in Fig. 4.40, as predicted by Chua [63].

Even though the devices exhibit bow-tie hysteresis loops with currents up to 1 mA, a lower compliance current is used in order to extend the repeatability of the post-forming behavior. With a range of -2.2 V to +2.4 V and a compliance current of 50 pA, the devices exhibit memristor behavior with high repeatability. The most common failure mode of the devices is a hard-breakdown leading to Ohmic behavior.

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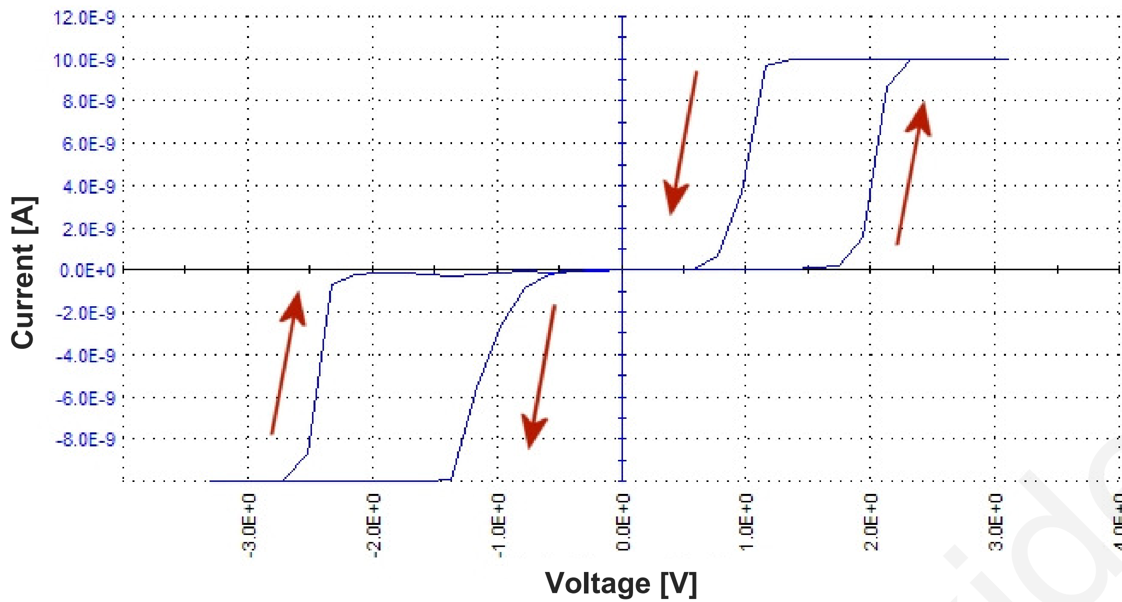

Figure 4.40: Typical bow-tie loop evident in the post-forming region. The voltage sweep range is ±3 V and the current compliance set at 10 nA.

Further tests were employed to confirm the memory capabilities, or plasticity effect, of this structure. As shown in Fig. 4.41, successive positive voltage sweeps (1 - 3) in the first quadrant increase the conductivity of the device as revealed by the shifting of the curves to the left. A negative sweep (4) then decreases the device conductivity to lower levels illustrated by the shifting of the curve in the following sweep (5) to the right. Subsequent positive voltage sweeps not shown here increase the conductivity once again.

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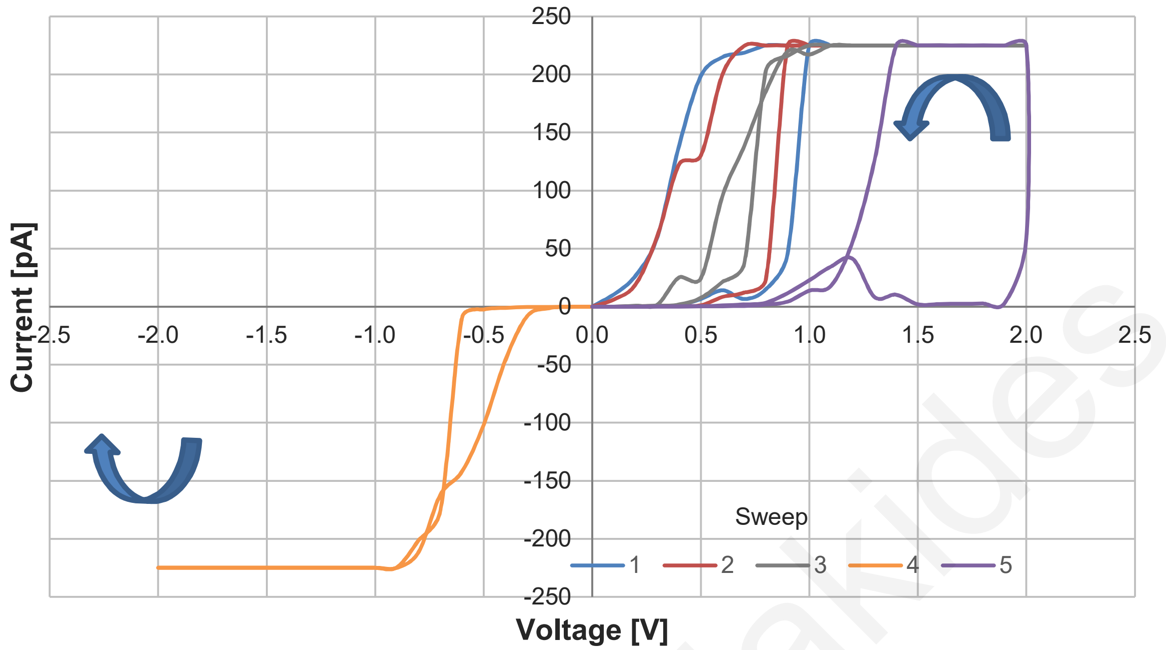

Figure 4.41: I-V sweeps of devices in the post-forming region with ±2 V sweep range and 225 pA compliance current. The order of voltage sweeps is shown in the index on the bottom right of the plot.

Fig. 4.42 illustrates the same behavior with more emphasis on the 3rd quadrant. Initially, positive sweeps shift the loop to the left, indicating an increase in conductivity. Successive negative sweeps (4 - 6), shift the loop to the left, indicating a drop in conductivity. As a result, the subsequent positive sweep (7) approaches the conductivity of the first positive sweep (1).

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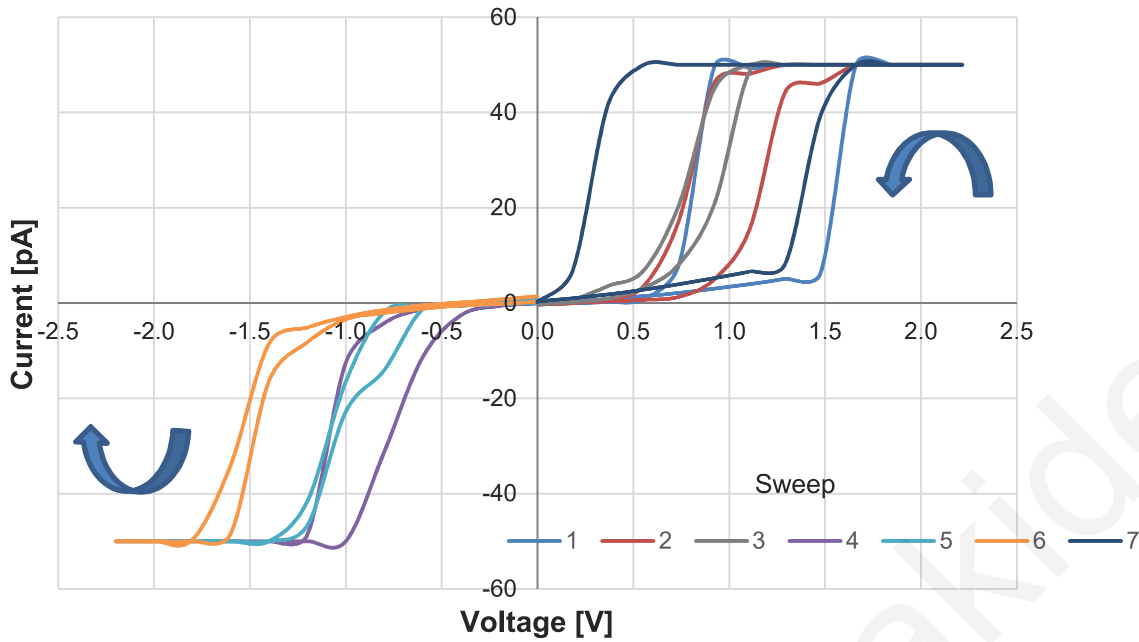

Figure 4.42: I-V sweeps of devices in the post-forming region with ±2.25 V sweep range and 50 pA compliance current. The order of voltage sweeps is shown in the index on the bottom right of the plot.

4.4.5 Threshold voltage designation

With the aim of modeling the devices and extraction of Verilog-A code for use in analog design, metrics need to be defined for the post-forming behavior. Hence the threshold voltage is defined as the point at which the post-forming current through the device begins to deviate from the pre-forming I-V trace (Fig. 4.43). Some devices consistently exhibit desired thresholds between 1.0 - 1.8 V. However, undesired behavior is also observed, whereby the threshold current quickly drops to 0 V. This attests to hard switching, a case where the filaments are created permanently, leading to Ohmic behavior.

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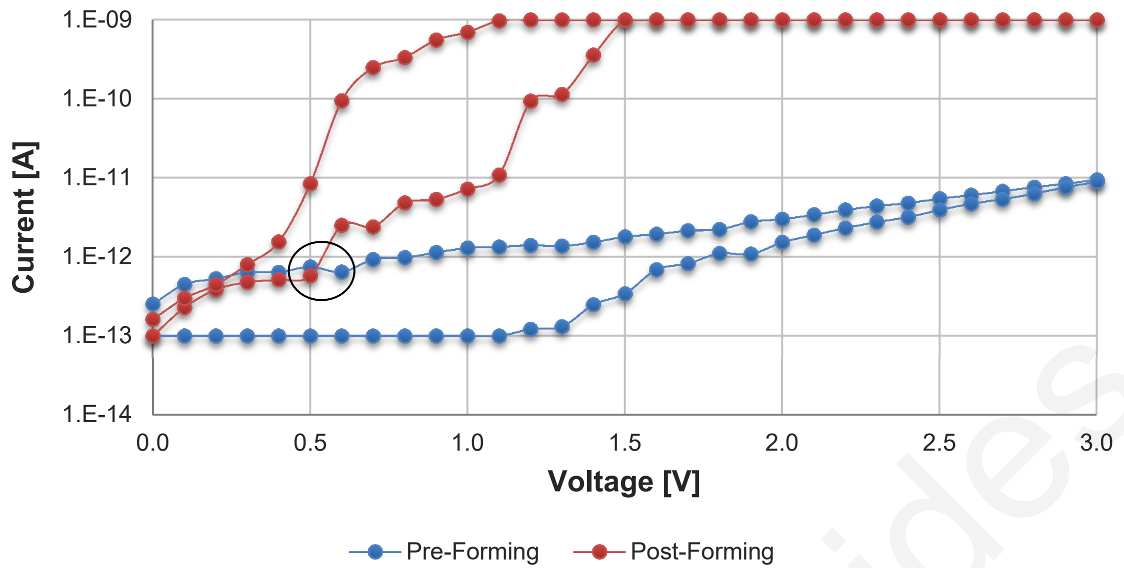

Figure 4.43: Semilogarithmic graph for definition of threshold voltage with the threshold voltage circled.

Threshold voltage histograms and evolution for different devices, with compliance current set at 250 pA, can be seen below. The undesired behavior is exhibited by device A, whereas the desired behavior is exhibited by devices B and C.

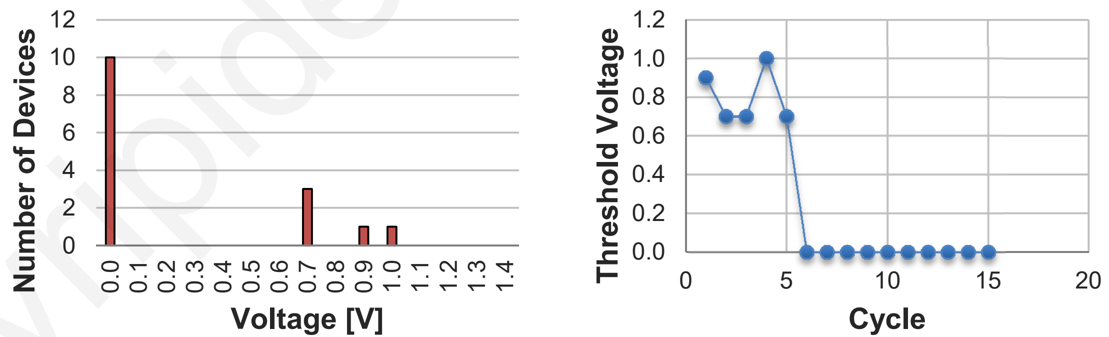

Figure 4.44: Threshold voltage histogram (left) and threshold voltage evolution (right) for device A.

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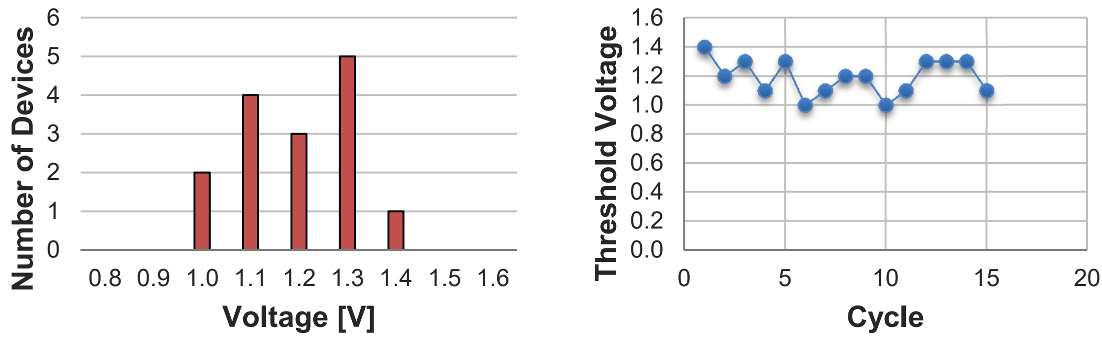

Figure 4.45: Threshold voltage histogram (left) and threshold voltage evolution (right) for device B.

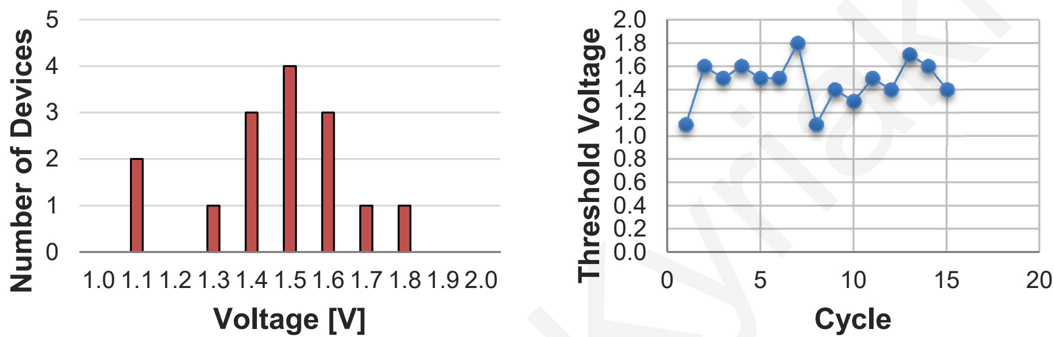

Figure 4.46: Threshold voltage histogram (left) and threshold voltage evolution (right) for device C.

The measurements illustrated in Figs. 4.44 - 4.46 above lead to the extraction of the devices' threshold voltage. This is defined from the median as 1.55 V and will be used in the device modeling detailed in later sections. The same procedure was carried out in the opposite polarity, yielding a value of 0.9 V for the negative threshold. It should be noted that the threshold is just a figure of merit, a discreet observation phenomenon in an otherwise continuous process. It is the result of compounding two exponential processes, namely the filament growth and electron tunneling.

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4.4.6 Pulse measurements

Pulses were used to test the response of the devices in a pulse-driven circuit. The input was chosen as current and the output measured in voltage. This enables limiting the current input to the devices to avoid irreversible breakdown.

The first observation that was made during the measurements was the unexpected ripple in the signal (Fig. 4.47).

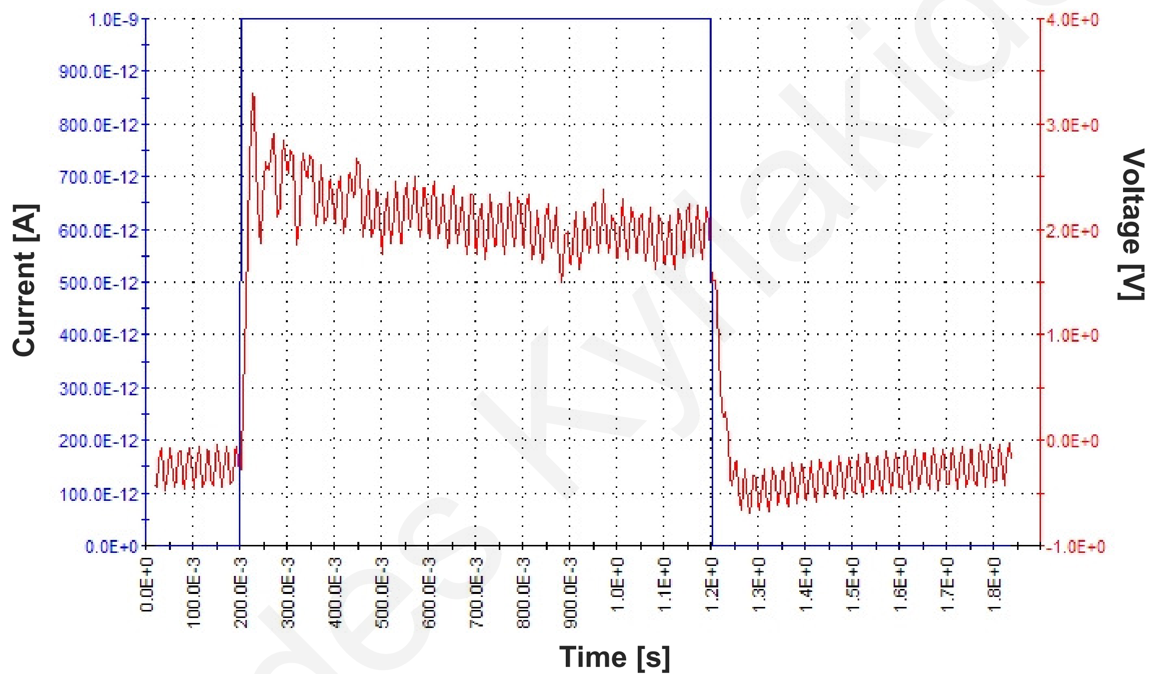

Figure 4.47: Typical response of DUT under pulse input.

To verify that the ripple is noise-induced, Fourier analysis was performed on the signal. With no current or voltage input to the Device Under Test (DUT), the Power Spectral Density yields a clear source of noise at 50 Hz (Fig. 4.48). This can be attributed to the electrical power supply. There is also another minor source of noise at 5 Hz which is assumed to be equipment-related, also visible in Fig. 4.48.

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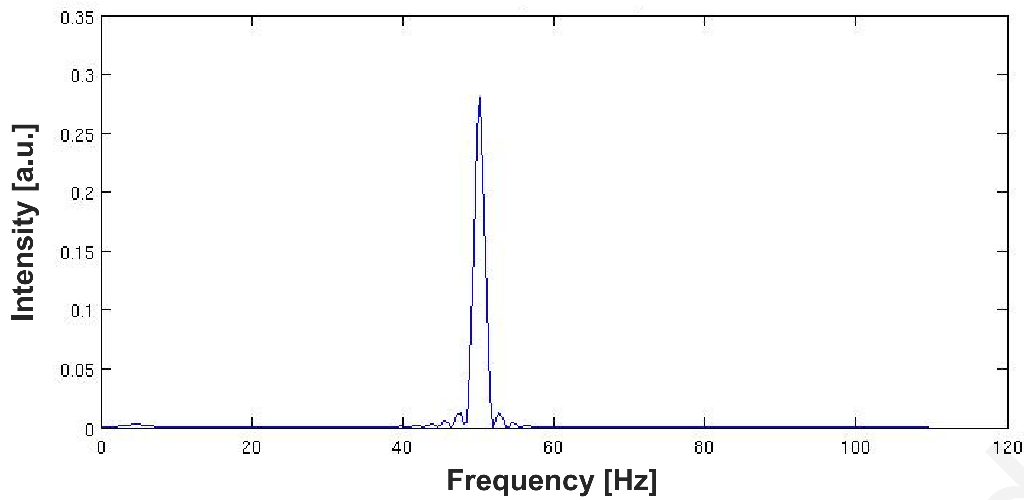

Figure 4.48: Power Spectral Density of DC signal.

The DUTs were driven with 1 nA, 1 s pulses. Although the response has shown some variability, the general behavior can be extracted. Before forming the DUTs, the voltage measured during the pulse increases (Fig. 4.49).

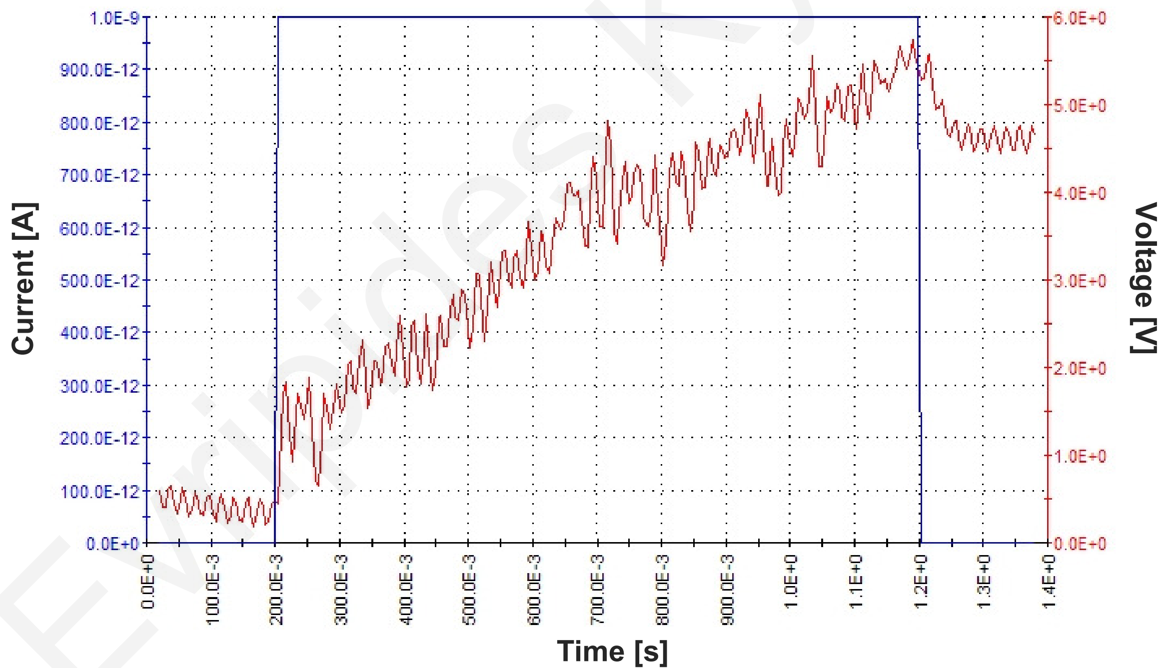

Figure 4.49: Pulse applied to device in pre-forming region.

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After forming the DUTs, the response to a 1 nA, 1 s pulse is a drop in voltage, implying a drop in resistance of the device, as shown in Fig. 4.50. The peak voltage, settling voltage, and settling time observed vary from 1.2 V to 6.5 V, 1.5 V to 3 V, and 100 ms to 1 s, respectively. The average peak voltage, settling voltage, and settling time are 4.09 V, 1.8 V, and 455 ms, respectively (Figs. 4.51 - 4.53). The standard deviation for the peak voltage, settling voltage, and settling time is 1.52 V, 0.51 V, and 0.19 s, respectively.

Given the above, the expected shape of the desired waveform would have the shape of Fig. 4.50 with an initial peak of 4.09 V and settling at 1.8 V after 455 ms.

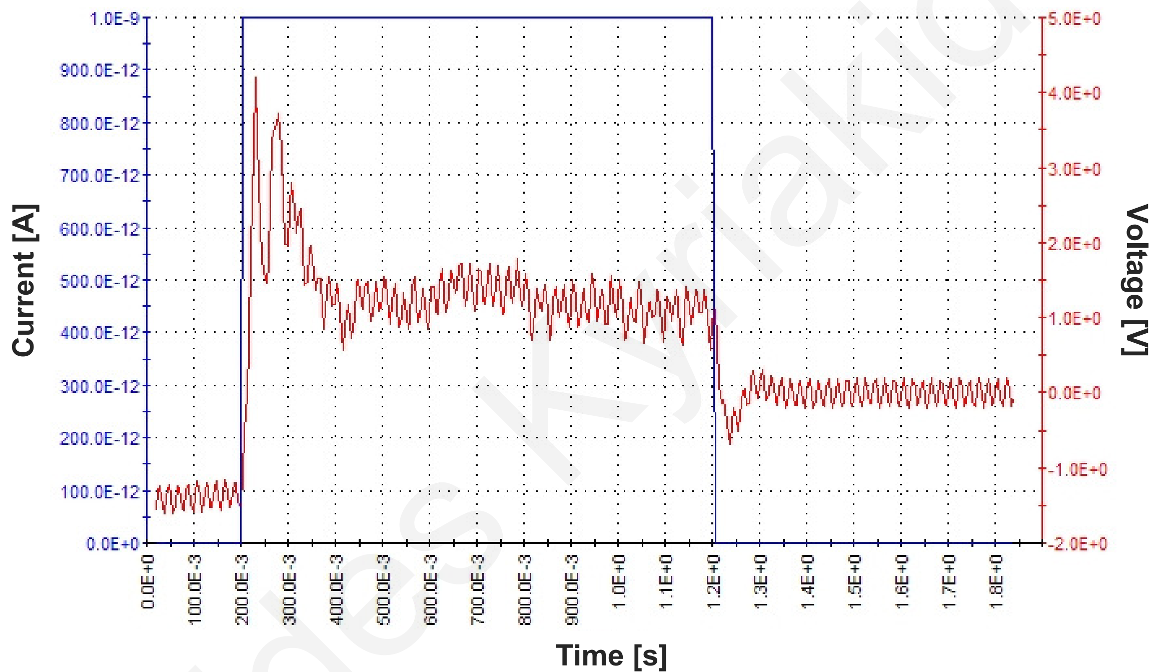

Figure 4.50: Pulse applied to DUT in post-forming region.

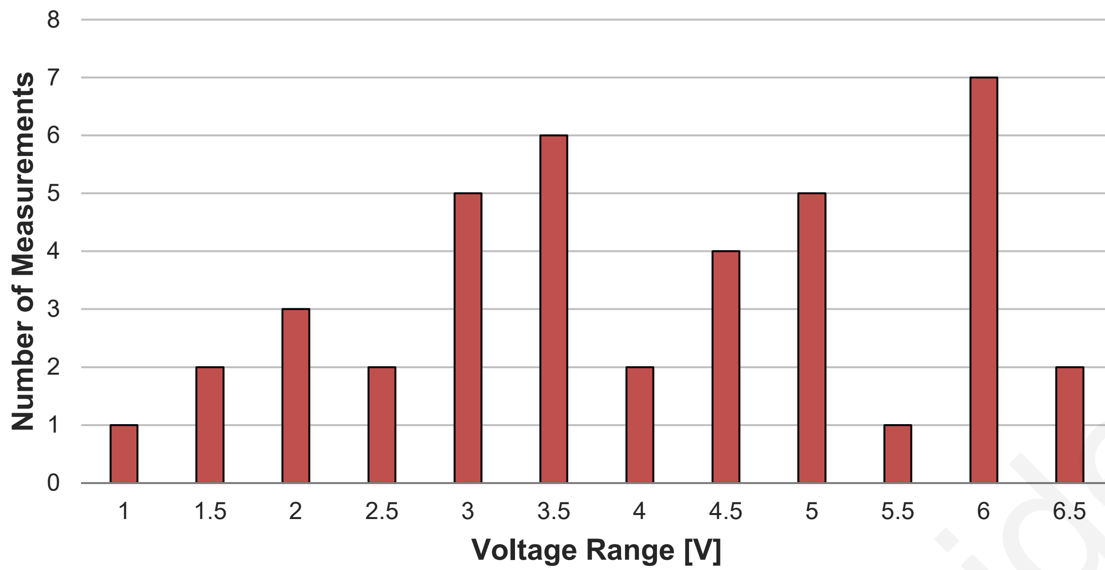

Figure 4.51: Histogram of peak voltage range count.

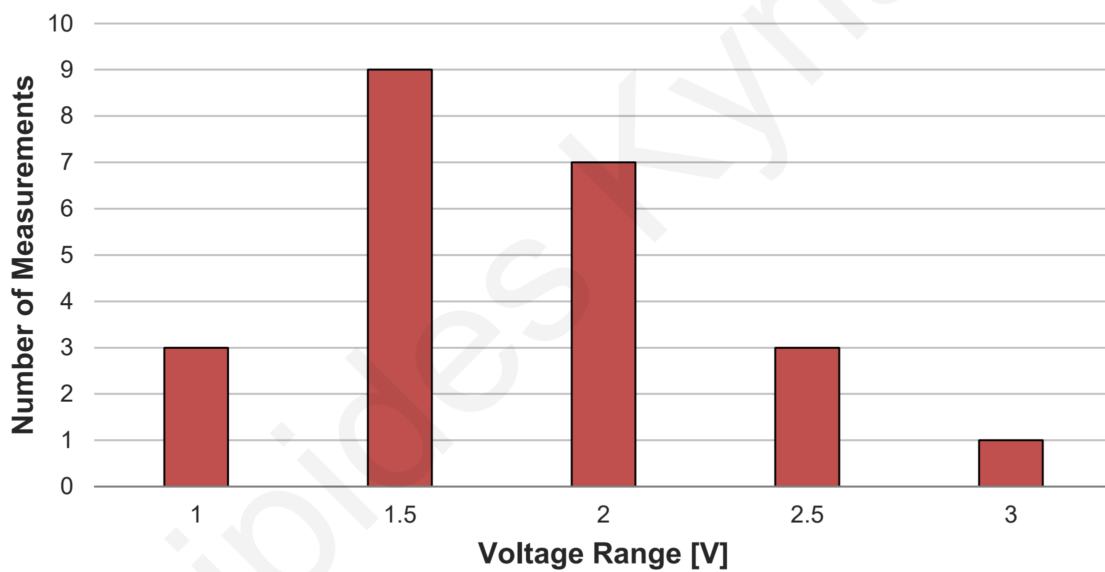

Figure 4.52: Histogram of settling voltage range count.

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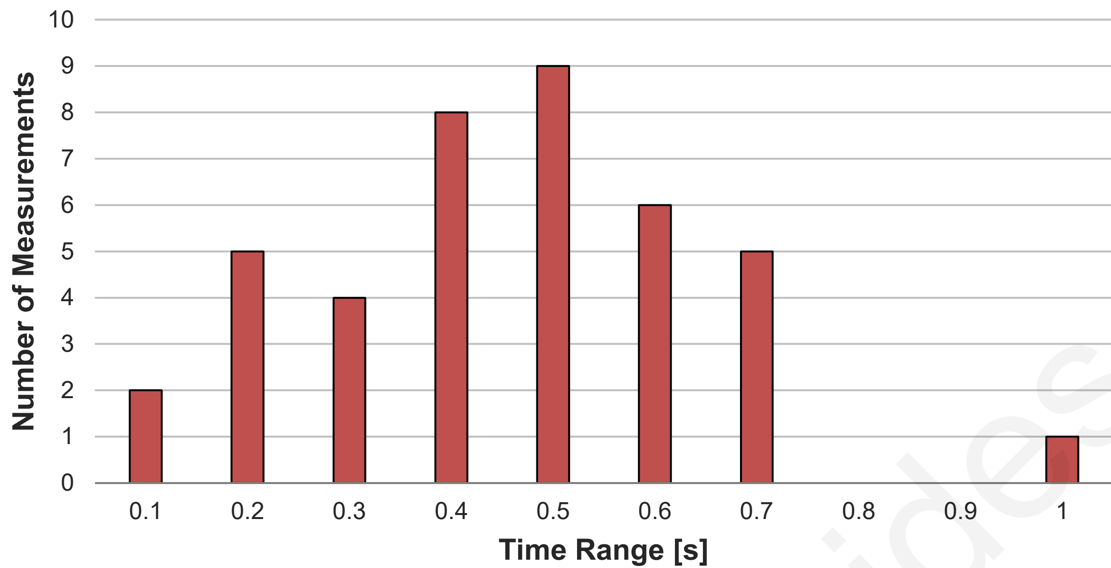

Figure 4.53: Histogram of settling time range count.

4.4.7 AC measurements

Using the measurement module, shown in Fig. 4.30, and the NI PCI-4462 acquisition board as a current-to-voltage transducer, AC measurements were made. The results of the measurements successfully showed hysteresis in the I-V domain. Fig. 4.54 shows a typical measurement depicting a sinusoidal voltage sweep.

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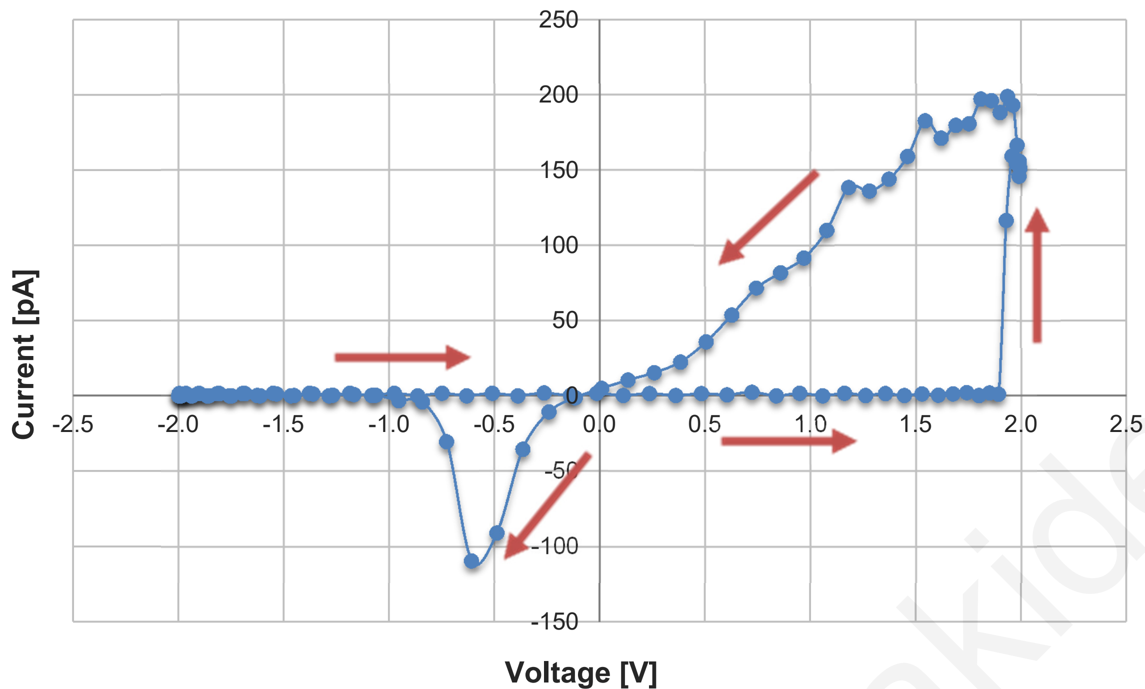

Figure 4.54: AC measurement using custom-made measurement module at 10 Hz, with ±2 V sweep range and 200 pA compliance current, showing bow-tie hysteresis loop.

4.4.8 Behavioral modeling

A variety of memristor models have been proposed in the literature. The most prominent ones are treated analytically in [111]. The simplest models assume linear ion drift. This type of model was first applied to the HP TiO_2-based device [112]. The model assumes two physical regions of uniform resistance within the device. It also assumes Ohmic conductance and equal average ion mobility of ions. These assumptions make it unfit for the Cu/Ta_2O_5 device. The nonlinear ion drift model of [113] is more appropriate for the Cu/Ta_2O_5 device but does not include voltage thresholds and suffers from low accuracy compared to existing devices. A very accurate model is the Simmons tunnel barrier model [114]. However, this model suffers from high complexity, making it computational inefficient and is current-controlled rather than voltage controlled. The TEAM model [111] is sufficiently accurate, adaptable, and provides for thresholds. However, these are current thresholds, this being a current-controlled model. A variation of that model is the VTEAM, a voltage-controlled model featuring simplicity, computational performance and adaptability. Nevertheless, a less adaptable model includes the features best fitted for the

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current approach. The model by Yakopcic et al. [115] does not offer the adaptability of the VTEAM model or the accuracy of the Simmons model. It can, however, be used as a starting point since, as shown below, it can capture the necessary attributes of the Cu/Ta_2O_5 device despite its simplicity.

The model of the device was extracted using the results from the measurements investigated thus far. To this end, analysis tools were used to model the measured electrical behavior. Origin® data analysis software was used to fully capture the equations describing the fabricated devices in their differential form. The equations extracted were then used in conjunction with diffusion models to mimic the devices' function in an analog design suite.

The Cu/Ta_2O_5 device functionality is based on diffusion of metal ions into a dielectric layer. Diffusion models, which can account for the diffusion of Cu into the Ta_2O_5 layer, can thus form the necessary platform for the deduction of an accurate device model. Such a model has been proposed by Yakopcic et al.. However, both experimental results and ab initio calculations show that the particulars of the model have to be adjusted and new variables have to be added in order to match the observed response.

Device characterization clearly shows the need for a threshold voltage in the model. Furthermore, different threshold voltages are evident for the positive and negative domains. Hence, the exponential form proposed in [115] is used instead of the hyperbolic sine proposed in [116], which allows for two distinct programming voltages for each polarity. A hyperbolic sinusoid is expected to correctly implement the current equations. The hyperbolic sinusoid is typical of electron tunneling [69] and is predicted by the results reported in previous sections on these devices.

Several aspects have to be taken into account to proceed with a first-principle approach to device modeling. Breaking down the factors that contribute to the observed electrical response leads to the simplification of a seemingly complex behavior.

The electrochemical process starts with the formation of a filament from the bottom electrode. The applied electric potential oxidizes copper atoms to Cu^{+} and Cu^{2+} cations from the top electrode, which is acting as a cation reservoir. The potential gradient then drives them to the Ta_2O_5/Pt interface through the Ta_2O_5 electrolyte layer. Ta_2O_5 in its crystalline form appears to show negligible ionic conductivity. However in its amorphous state, as is the case with the devices under consideration, it facilitates ionic conduction along grain boundaries and other defects, such as dangling bonds [117].

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The cations are subsequently electrodeposited (a process also known as inhomogeneous nucleation) on the platinum bottom electrode. This leads to the preferential formation of filaments of copper atoms from the bottom electrode growing towards the top electrode. The growth of this filament, or filaments, is accomplished via the electroforming process described before. The process of fine-tuning the electroforming time and voltages, as outlined previously, amounts to creating filaments of the appropriate length. Ideally, filaments need to approach the top electrode to the point of facilitating tunneling of electrons. Excessive forming leads to either a multitude of filaments and/or filaments of large radius which persist under switching, a condition known as hard switching. Through measurements on filamentary devices, a universal equation has been derived for forming time [110]. The average time is given as:

$$\tau_w = \frac{1}{\nu}\, e^{\frac{E'_a}{k_B\,T}} = \frac{1}{\nu}\, e^{\frac{E_a}{k_B\,T}}\, e^{\frac{-\alpha\,E}{k_B\,T}} \tag{4.3}$$

where E'_a is the activation energy for ion transport under the applied electric field, E is the applied electric field, ν is the attempt frequency of ion hopping, k_B is the Boltzmann constant, T is the absolute temperature, and α is a positive fitting parameter determined by material properties. The effective activation energy E'_a is related to the material-dependent activation energy at zero field E_a with the relationship $E'_a = E_a - \alpha\,E$ due to the barrier lowering effect. Eq. 4.1 relates the forming time with the electric field but also predicts the temperature dependence of the forming time [118].

Successful electroforming renders a device that can switch when a voltage sweep or AC signal is applied. Switching the device entails the extension of the copper filament by positive voltage. Negative voltage causes the contraction of the filament, or its segmentation through Joule heating at high currents.

The growth rate of the filament can be calculated by considering the drift velocity of the ion at the top of the filament [119]. This is defined as:

$$\frac{dl}{dt} = d\,\nu\,e^{\frac{-q\,U_a+(q\,V\,d)\,/\,(2\,(h-l))}{k\,T}} - d\,\nu\,e^{\frac{-q\,U_a-(q\,V\,d)\,/\,(2\,(h\,-\,l))}{k\,T}} \tag{4.4}$$

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where l is the filament length, d is the distance between adjacent hopping sites, ν is the characteristic ion hopping attempt frequency, U_a is the activation potential, k is Boltzmann's constant, T is the temperature, q is the electron charge, and h is the dielectric thickness. The right side of the equation contains two terms to differentiate between the probabilities that the ion hops forward (first term) and backward (second term). This equation can be modified as follows:

$$\frac{dl}{dt} = d\,\nu\,e^{\frac{-q\,U_a}{k\,T}}\,e^{\frac{q\,V\,d}{k\,T\,(2\,(h-l))}} - d\,\nu\,e^{\frac{-q\,U_a}{k\,T}}\,e^{\frac{-q\,V\,d}{k\,T\,(2\,(h-l))}} \tag{4.5}$$

In the case of high electric fields or small gaps between filament and top electrode, the gap dependence can be approximated by a free ranging parameter given as $d_{1,2} = \pm k\,T\,2\,(h-l)/(q\,d)$ [118]. Further defining $c_{1,2} = \pm d\,\nu$, and $V_{p,n} = \pm q\,U_a/(k\,T)$, the relationship can be written as:

$$\frac{dl}{dt} = c_1\,e^{-V}\,e^{\frac{V}{d_1}} + c_2\,e^{V}\,e^{\frac{V}{d_2}} = c_1\,e^{\frac{V}{d_1}-V_p} + c_2\,e^{\frac{V}{d_2}+V_n} \tag{4.6}$$

The relationship described above can be mapped to the pair of coupled equations defining the voltage-controlled memristor relationship. The first equation is given by:

$$\frac{dw}{dt} = f(w, v) \tag{4.7}$$

where the first derivative of the memristor's internal state can be defined in terms of the internal state and voltage. Therefore the length of the filament can be considered as the memristor's internal state.

According to the second memristor equation:

$$i(t) = G(w, v)\,v(t) \tag{4.8}$$

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the current is a function of the device's state variable and the voltage across it. The dominant source of current in these devices is the tunneling of electrons between the tip of the filament and the top electrode. Tunneling current is a hyperbolic sine function. Using parameters a and b to account for material-specific parameters and using the normalized length as the state variable, the current can be expressed by:

$$I(t) = a\, w\, sinh(b\, V(t)) \tag{4.9}$$

Thus far the parameters have been considered identical when dealing with either polarity. This is not always the case, as noted for example with d, the distance between adjacent hopping sites. This is also evident in measurements. To account for the mismatch between polarities, the hyperbolic sine in the state variable equation is broken into exponentials which allow for separate parameters to be specified for each polarity. Similarly, the current equation can potentially be defined according to polarity. Hence, with $V(t)$ the voltage applied to the memristor, the current $I(t)$ is given as:

$$I(t) = \begin{cases} a_1\, w\, sinh\big(b_1\, V(t)\big), & if\;\; V(t) \geq 0 \\ a_2\, w\, sinh\big(b_2\, V(t)\big), & if\;\; V(t) < 0 \end{cases} \tag{4.10}$$

where $a_i, b_i > 0$ are constants, and $0 < w < 1$ is the state variable of the memristor.

The state variable w is defined through its time derivative as:

$$\frac{dw}{dt} = c_1\, e^{\frac{V(t)}{d_1} - V_p} - c_2\, e^{\frac{V(t)}{d_2} + V_n} \tag{4.11}$$

where $c_i, d_i, V_{p,n} > 0$ are constants.

Joule heating becomes increasingly important as secondary effects are taken into consideration. Once the filament covers the entire span of the dielectric layer, lateral expansion starts taking place. The filament continues to grow laterally, further decreasing device resistance. However, the decrease in resistance and inverse increase in current result in higher power dissipation. This in turn increases the Joule heating which becomes,

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through segmentation by increased ionic drift, the primary cause for taking the device back to HRS. These effects can be included in a more rigorous approach of device modeling. However the first approximation is shown to adequately simulate device behavior.

Verilog-A was preferred over Analog Hardware Descriptive Language (AHDL) for coding the governing equations due to better convergence of differential equations. The result is a model of the device that can fully describe its transfer function, even under stimuli not yet measured.

The equations extracted were subsequently used to mimic the devices' function in Cadence analog design suite. A typical simulation result, describing the Cu/Ta_2O_5 device electrical response while taking into account the input history, can be seen in Fig. 4.55. The Verilog-A code used for the model is included in Appendix C. Fig. 4.56 shows a typical response of the model with an AC signal.

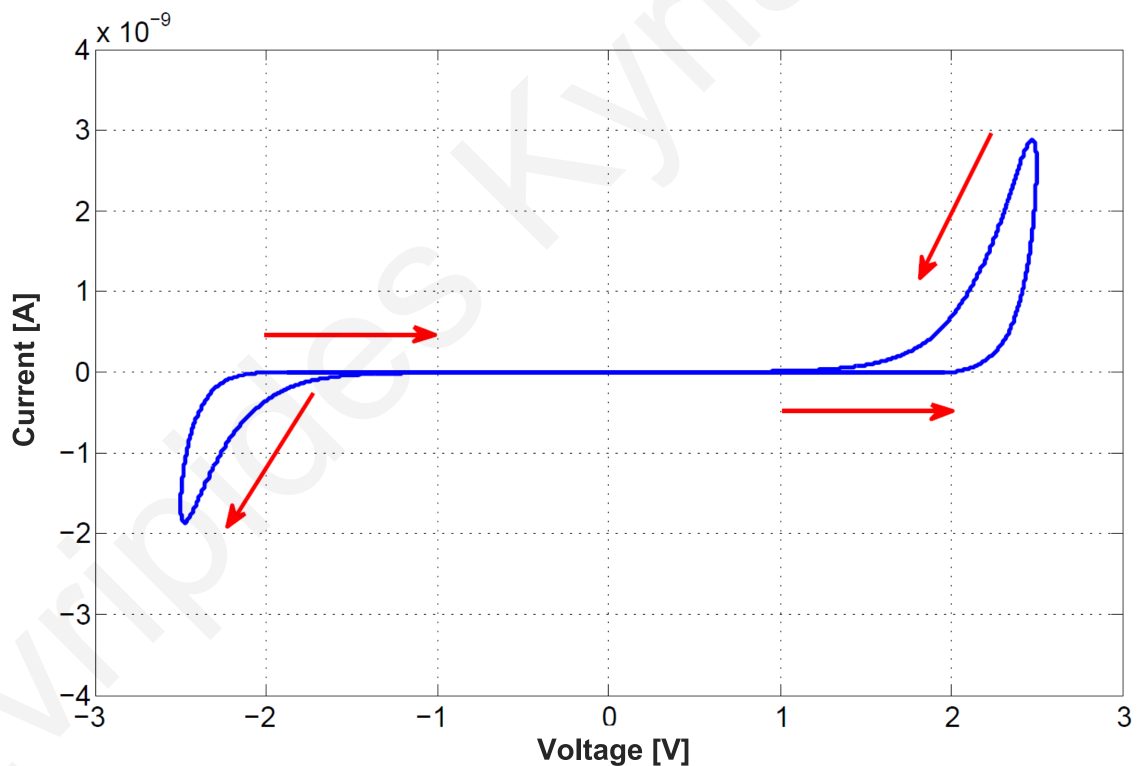

Figure 4.55: Extracted response of Cu/Ta_2O_5 Verilog-A model in Cadence environment for 2.5 V, 1 kHz sinusoidal excitation. Simulation parameters are: $a_1 = 8\times10^{-5}$, $a_2 = 1.5\times10^{-6}$, $b_1 = 4$, $b_2 = 4.5$, $c_1 = 2\times10^{-5}$, $c_2 = 2\times10^{-5}$, $d_1 = 1$, $d_2 = 1$, $V_p = 1.55$, and $V_n = 0.9$.

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For comparison and verification, measurements from the device post-forming response to a 1 kHz AC signal, can be seen in Fig. 4.56. The simulation correctly captures the key traits of Cu/Ta_2O_5 devices. They both result in zero-pinched bow-tie hysteresis curves - although a closer inspection around the origin reveals that the measured curve does not cross the x-axis at zero current. This is attributed to measurement error, especially considering that both positive and negative crossings occur at positive y-axis values, as opposed to the examined pre-forming case. In contrast with NiTi, measurements and simulations confirm the crossing property for this device. In other words, a bipolar sweep will produce lobes of opposite rotation; clockwise and counterclockwise. Most importantly, the asymmetry between positive and negative polarity, the operation thresholds, and the steep exponential change in current beyond the thresholds, are also evident.

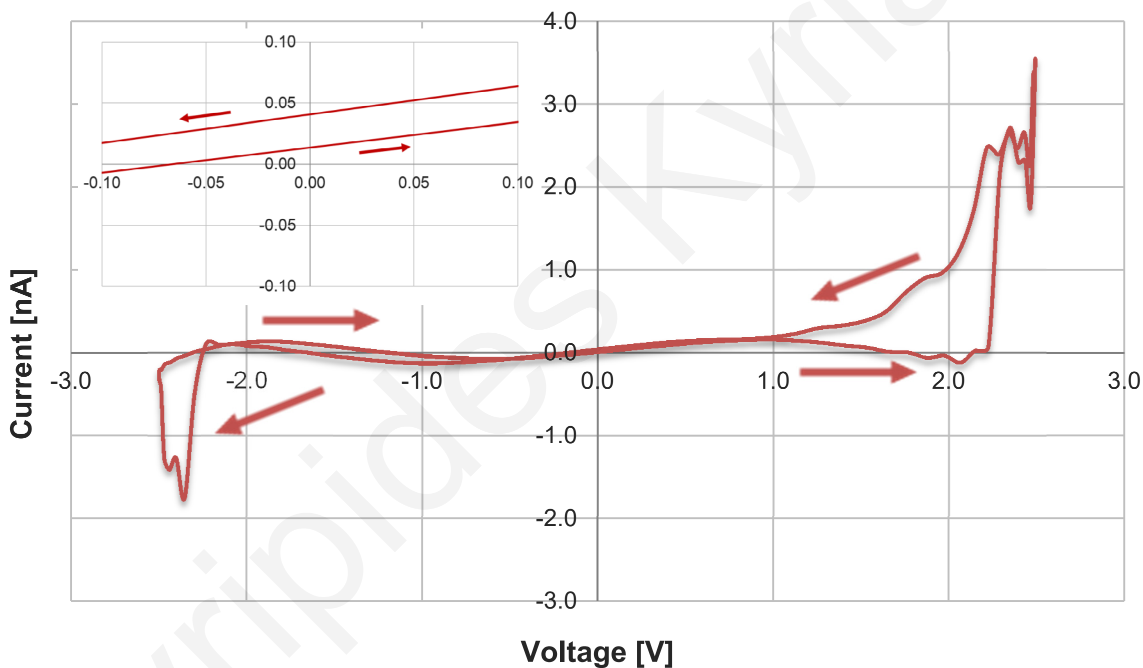

Figure 4.56: Measured post-forming AC behavior of Cu/Ta_2O_5 device at 2.5 V, 1 kHz. Inset: Magnification of curve around the origin region.

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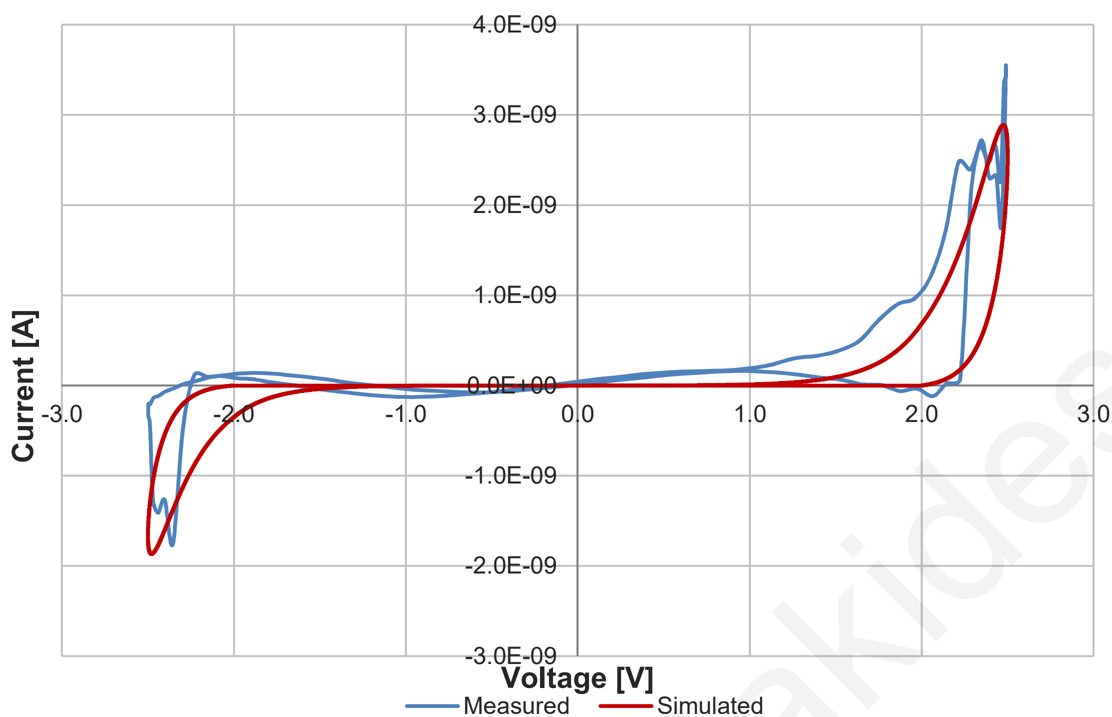

Figure 4.57: Comparison of measured and modeled post-forming AC behavior of Cu/Ta_2O_5 device at 2.5 V, 1 kHz.

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4.4.9 Discussion

Analysis of Cu/Ta_2O_5 devices commanded a variety of characterization tests to fully explore their functionality. The most challenging aspect of characterization was the scale of currents involved, which required special attention. The solutions applied were successful in producing the required results.

The characterization described in the preceding sections revealed two regions of operation, which have been extensively studied. The origin of each region is examined and reveals the electrochemical mechanisms involved.

In studying the Cu/Ta_2O_5 structure, the necessity for inclusion of the top electrode was first established. The role of the top electrode was subsequently investigated by a series of measurements. Through cyclic voltammetry experiments, it has been shown that the devices exhibit a hysteresis curve in the pre-forming region. The Cottrell equation was thus applied to the I-V traces. Redox reactions were discarded in this region due to the lack of specific markers. Therefore, an explanation is offered for the pre-forming behavior, in the

form of cation diffusion, which is supported by measured results. Nonzero current at zero voltage is explained through charge retention in the dielectric layer. Measurements comparing the different active device regions have not produced significant variations or a clear trend. This is consistent with filamentary operation.

A proposed method of electroforming has been proposed. The metrics used can transfer the device to the post-forming region without causing hard switching. FIB/FESEM verifies the forming process through high-resolution imaging.

Post-forming behavior conforms to the Chua definition of a memristor, in the form of a zero-pinched now-tie hysteresis loop. It also shows the plasticity effect in this structure, where positive and negative voltage sweeps are used to potentiate and depress the device, respectively. In this region of operation the thresholds are calculated for the device to be subsequently used in modeling. Finally, pulse measurements show how the device can be used in a neuromorphic circuit.

The modeling results of Cu/Ta_2O_5 devices have been extracted through the process described above. A first-principles study is developed and, in conjunction with extracted data, produces a model for the device. A comparison between measured and simulated results shows the expected agreement, thus enabling the further exploitation of Cu/Ta_2O_5 devices.

Cu/Ta_2O_5 memristors provide characteristics useful for biomimetic circuit design. Although the frequency dependence of the pre-forming hysteretic response is not compliant with the strict memristor definition [18], these devices can be employed as synapses in Hebbian learning neural circuits or STDP synapses [120, 121].

For the case where the post-forming behavior is desired, the forming process and functional characteristics have been extensively described. The devices have shown that in this region of operation they possess the attribute of plasticity such that they can be used as electronic synapses in neuromorphic circuits.

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4.5 Conclusion

This chapter has described the electrical characterization and modeling of fabricated Cu/Ta_2O_5 devices. The characterization results were used to develop a behavioral model. The model were subsequently compared to measured data of the device to assure matching.

The forming procedure for Cu/Ta_2O_5 devices has been described and two regions of operation, namely pre- and post-forming, have been introduced. The array of measurements performed on the devices has been described and a mathematical model implemented in Verilog-A has been derived for the post-forming behavior of the devices. Finally, simulations with the coded model have been shown to agree with respective measurements.

The following chapter builds on the characterization and modeling results presented thus far to facilitate the design of bioinspired circuits.

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Chapter 5

Bioinspired System Demonstration

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5.1 Introduction

Although memristive devices have been around, both theoretically and physically for a long time, they have not been adequately exploited in computational infrastructure [13, 66, 122]. It is hereby demonstrated how memristive devices can be used to implement synaptic and other neural components that are required in the next generation of neuromorphic systems.

This chapter builds upon the work completed in the previous chapters in presenting circuit applications based on memristor devices. This is intended as a first step in utilizing memristive devices either to improve current circuits or exploit their unique properties to design novel circuits. The first application is a memristor-based oscillator. The main advantage of such a design over an RC oscillator is the significant reduction in chip footprint. The second application is a neural circuit exhibiting learning. The circuit utilizes artificial neurons to generate spikes that train memristors. The system has the ability to learn, resulting in an output that is modified according to past inputs.

5.2 Memristor oscillator

Memristive devices display some unique properties that can, depending on the specific application, be used in a variety of disciplines. It has been shown that their hysteresis can be used in neural networks. More specifically, in a two-fold manner they can be used as the ion conductances in the Hodgkin-Huxley model of the axon membrane potential [59, 123],

or replacing the entire synapse in spiking network applications [124]. Their non-volatility can be used in RRAM applications with potentially significant advantages over current technologies [125]. In this instance their polarity-dependent change in resistance is employed in order to design a reactance-less relaxation oscillator without using space-consuming capacitors [126].

For the purpose of designing a circuit prototype, a well-studied memristor device is preferred over newer and less researched devices. This eliminates the ambiguity of similar devices whose physical operation is not yet fully understood. The aim of showcasing the advantages of using memristors in rethinking existing approaches is thus better served. The HP memristor has been extensively studied and is well understood. Furthermore, it has a small footprint that leads to significant reduction in chip area. Additionally, it can be incorporated in a CMOS process. However, other types of memristors are expected to integrate similarly into the circuit, since the basic property that leads to oscillation is the polarity-dependent change in resistance.

The oscillator is designed using a memristor model deduced through the formulations described in Chapter 2. The memristor is used to substitute the function of a capacitor in an equivalent RC oscillator. The voltage across the memristor changes according to the quantity and polarity of the current passing through, thus substituting the changing voltage across a capacitor in the equivalent RC oscillator. The memristor has the advantage of occupying much less area than the equivalent capacitor, which may be important when trying to build on-chip oscillators for portable or medical applications.

Low frequency oscillators are widespread in biological interfacing applications and embedded systems [127, 128]. Biomimetic architecture can potentially achieve immense processing power through the use of parallelism while keeping low frequencies of operation. Since the frequency of operation of relaxation oscillators is inversely proportional to the time constant, $\tau = R\,C$, low-frequency operation requires either high capacitance (frequently leading to off-chip placement of the capacitor) and/or high resistance. That entails a large chip area being dedicated to these elements. In this case, we provide the equivalent function of the capacitor through the use of a significantly smaller memristor. Although memristor-based oscillators have been proposed, they either include reactive elements [129, 130], other complicated gates [131, 132], or are purely theoretical [133]. The relaxation oscillator using a memristor is hereby presented. The oscillator is designed for output oscillation at 10 kHz, the upper limit of biological system computation [134].

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Oscillators are intricately associated with integrate-and-fire neurons. Neurons may be considered a type of relaxation oscillator or astable multivibrator. Input excitation leads to output firing, which is an oscillation between action potential peak and resting potential. A lack of input leaves the output at resting potential. Likewise, a relaxation oscillator will oscillate between two output states with the application of voltage input and remain idle otherwise.

Both single neurons and groups of neurons can generate oscillatory activity. In individual neurons, oscillations can appear either as sub-threshold oscillations in membrane potential or as rhythmic patterns of action potentials [135, 136, 137]. This has been treated in the FitzHugh–Nagumo model, which contains the van der Pol oscillator as a special case [138]. At the same time, a great deal of research is aimed at deciphering the role of group oscillations of neurons in the mechanism of cognitive functions [139, 140, 141]. Thus, in addition to the aforementioned applications, this oscillator could thus be integrated into neural networks or used for large-scale cortical emulations.

5.2.1 Memristor model

The proposed circuit uses the HP memristor model [112]. The model, entailing linear dopant drift, calculates the device parameters based on the time integral of current through the device. Without loss of generality, a window function is added to restrict the thickness of the TiO_2 layer between the device's physical limits.

The equations describing the used model are derived starting from Chua's original definition of a memristive system [142, 143]. Such a system is defined by:

$$\frac{du}{dt} = f(x, u, t) \tag{5.1}$$

$$y = g(x, u, t)\, x \tag{5.2}$$

where x, y, and u represent the input, output and state of the system, respectively.

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In the special case of a current-controlled time invariant one-port element these reduce to:

$$\frac{du}{dt} = f(u, i) \tag{5.3}$$

$$v = R(u)\, i \tag{5.4}$$

where v and i represent the voltage across and the current through the device, respectively.

The HP memristor can thus be described, using w, the TiO_{2-x} layer width, as the state variable with:

$$\frac{dw}{dt} = f(w, i) \tag{5.5}$$

$$v = R(w)\, i \tag{5.6}$$

The rate of change of w with respect to time is given by:

$$\frac{dw(t)}{dt} = \frac{\mu_v\, R_{on}\, i(t)}{D} \tag{5.7}$$

where μ_v is the dopant drift mobility, R_{on} is the resistance at LRS, and D is the device length.

Since the time-integral of current gives the charge through the device, the resulting expression is:

$$w(t) = \frac{\mu_v\, R_{on}\, q(t)}{D} \tag{5.8}$$

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Therefore, the resistance exhibited by the device is equivalent to the memristance:

$$M(q) = \frac{R_{on}\, w(t)}{D} + \frac{R_{off}\,[1 - w(t)]}{D} \tag{5.9}$$

Here, μ_v is taken as the mobility of oxygen vacancies, 10 $fm^2 \cdot V^{-1} \cdot s^{-1}$, R_{on} and R_{off} are the boundary resistances, taken as 4.2 Ω and 1.6 kΩ, respectively, and D is 10 nm.

The model, based on data extracted from real devices, was implemented in Verilog-A and tested for correct representation of the bow-tie hysteresis curve, which is considered a key memristor fingerprint [63], before utilization in the circuit (Fig. 5.1).

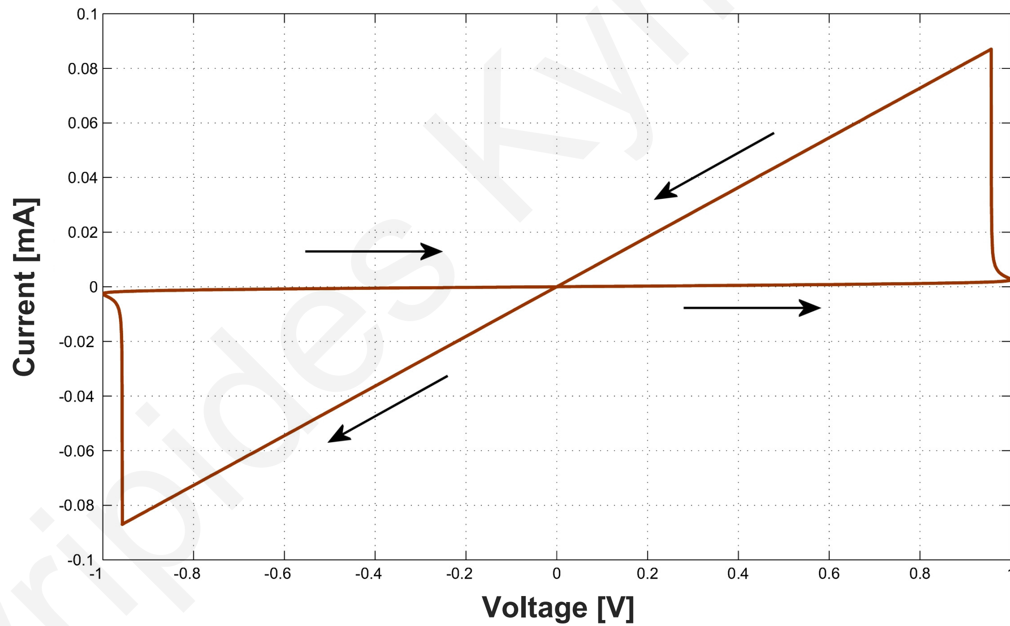

Figure 5.1: Hysteresis curve of memristor element resulting from Verilog-A model run in Cadence environment.

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5.2.2 Circuit design

An oscillator can be implemented according to Fig. 5.2. It consists of feedback to the op-amp inputs through two voltage dividers, one of which contains a memristor, whose instantaneous resistance depends on the past charge flow. In the past a similar function has been accomplished through the voltage divider formed by a capacitor and a resistor that is fed back to the op-amp. A bidirectional change in voltage across the memristor can be accomplished as a result of a polarity-dependent change in the memristor's resistance (Fig. 5.3).

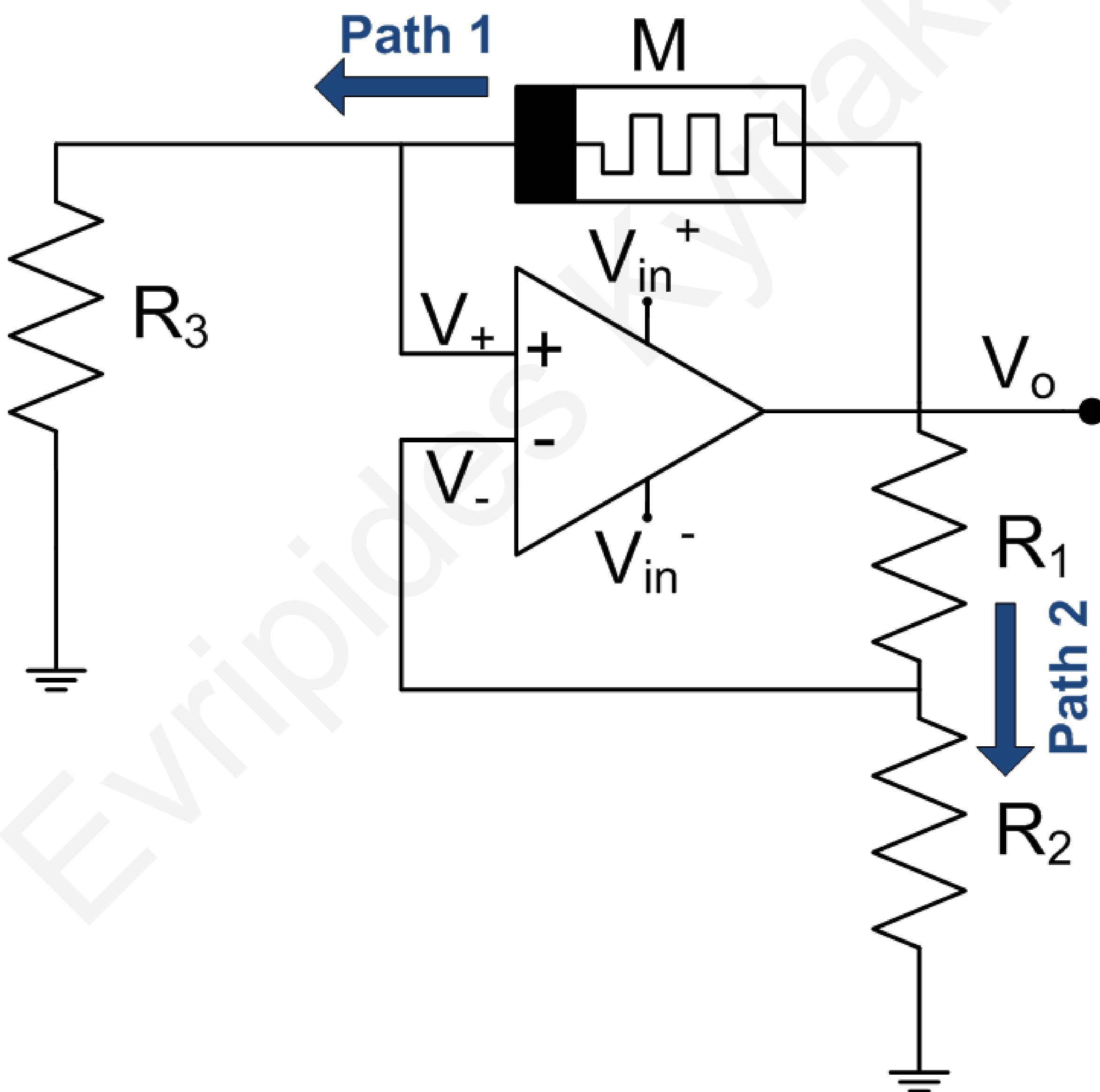

Figure 5.2: Schematic of the proposed oscillator circuit.

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The circuit in Fig. 5.2 was implemented in Cadence Virtuoso, incorporating the Verilog-A memristor model reported in the previous subsection. In the proposed topology, the memristor is connected to the positive feedback of the op-amp such that positive voltage across it causes an increase in resistance, thus dropping the fraction of the output voltage seen at the positive terminal. As the voltage drops below that of the negative terminal the output becomes negative and a current flows through the memristor in the opposite direction (Fig. 5.4). This increases the fraction of the output voltage appearing at the positive terminal, until it inverts the output voltage again and starts a new cycle. Repeating this indefinitely produces the oscillatory behavior seen in Fig. 5.5.

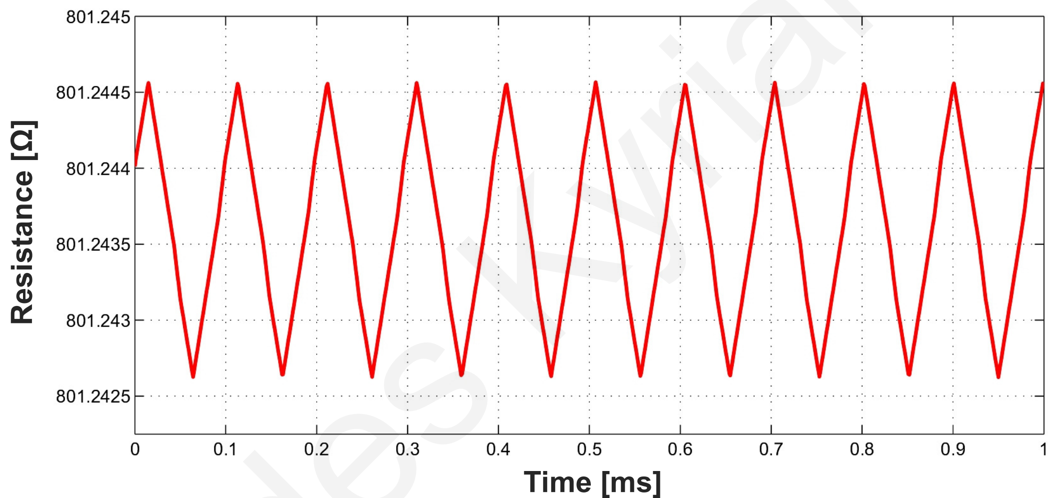

Figure 5.3: Resistance variation of memristor during oscillation.

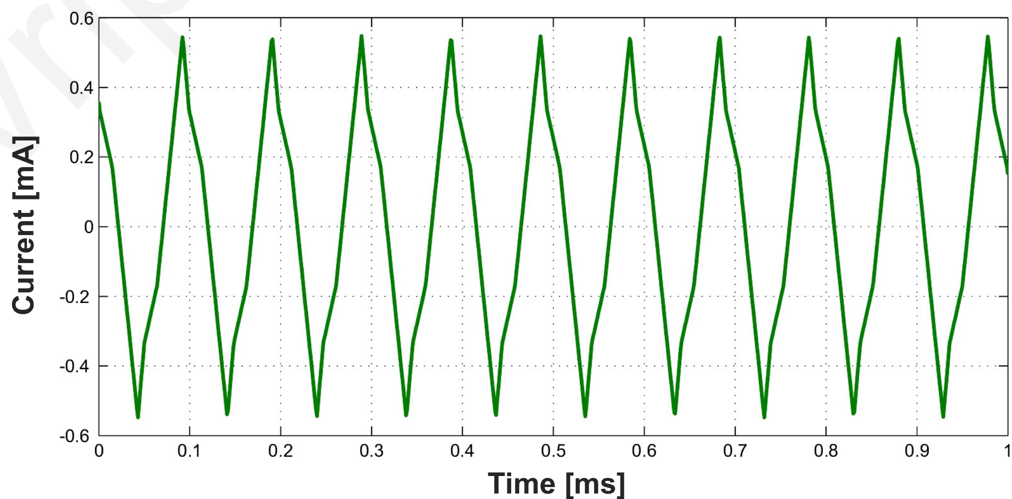

Figure 5.4: Current through memristor during oscillation.

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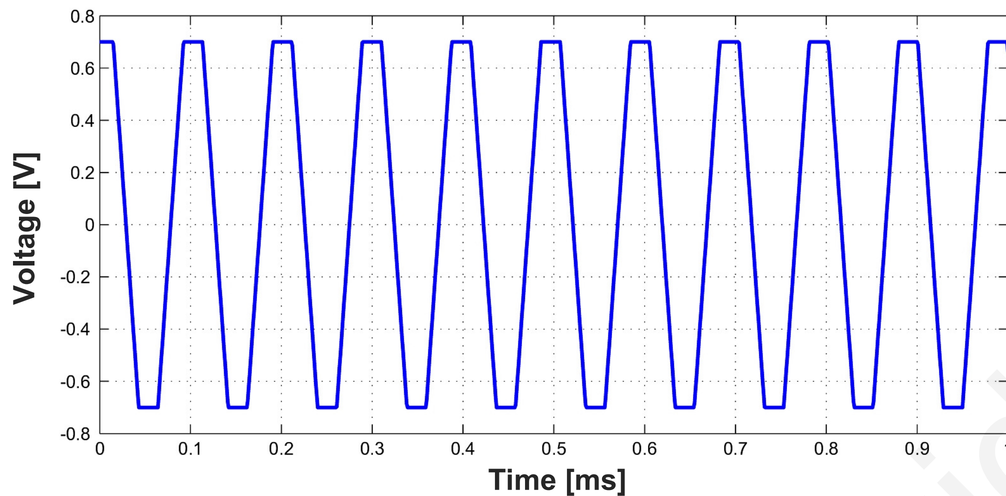

Figure 5.5: Circuit output voltage during oscillation.

The initial conditions necessary for oscillation are: (a) that the memristor starts at an initial state of low resistance (e.g. $R_M = R_{on}$), and (b) that it can reach a resistance value given by $R_M = (R_1\, R_3)/R_2$. To this end, the memristor initially acts as a resistance sweep function, varying its resistance until it reaches the crossing point with the inverting input.

Various parameters had to be taken into consideration during the design of the circuit. Most importantly, the ratio between resistances R_1 and R_2 affects the frequency of oscillation. However, this ratio can provide circuit designers the added benefit of post-fabrication tunability. Through the use of resistive trimming blocks, such as those used in [144], designers can define a range of frequencies to be chosen after fabrication by choosing the ratio R_2/R_1. Given the limits of the memristor resistance, fundamental limits are set on the value chosen for R_3. Design trade-offs balance higher resistance values, which give lower currents and hence lower power consumption, with lower resistance values that would give a smaller footprint at the expense of power consumption. Finally, the amplifier gain must be high enough so as to avoid a stuck-at-zero state and must be able to provide the currents required to bias Paths 1 and 2 (Fig. 5.2) accordingly. The aforementioned constraints result in resistance values of 5 kΩ, 20 kΩ and 3.205 kΩ for R_1, R_2 and R_3, respectively. The resulting oscillation frequency is 10.14 kHz.

In this particular implementation the peak current requirement of the circuit is calculated through simulations as 696.7 μA. However, since the output of the op-amp varies with time and the memristance is dynamic, the average is calculated as an integral of

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the current and voltage waveforms over time. Given the parameters above, and with rail voltages of ±0.7 V, optimization of the memristor-based oscillator resulted in power consumption of 199.8 μW. A further reduction in power could be achieved by increasing the overall resistances. In the case of the memristor, multiple memristors could be connected in series to achieve this.

5.2.3 Discussion

Without the use of memristors, various approaches could be used to build on-chip low frequency oscillators, such as using an ultra-low voltage local regulated supply [145], gm-C based oscillators or by using pseudo resistors to get a high resistance, without utilizing a prohibitively high area. In all these cases a high R is achieved by using an active device to limit the current that will charge a capacitance up, which will still take a relatively large area, given that on-chip capacitors are typically in the order 3 $fF \cdot \mu m^{-2}$. Given that the oscillation frequency depends on the RC constant, any benefit derived from reducing the size of R will also benefit the proposed capacitorless design, since the size of R here will also be reduced. Given that the HP memristor used in this implementation has a cross-point structure measuring 50 nm × 50 nm [69], it is quite clear that the proposed capacitorless design promises to provide extremely compact low frequency oscillator implementations on chip, just on the basis of being able to eliminate the capacitor. Of course it will depend on whether memristors become mainstream devices that are included as options on conventional processes.

Though ring oscillators can have small chip area compared to the RC oscillator, they typically exhibit higher oscillation frequencies [146]. This frequency then needs to be divided multiple times to reach the frequency of the proposed circuit (10.14 kHz). Moreover, they are extremely sensitive to supply voltage. RC-based oscillators are less sensitive to supply, nevertheless, in order to match the oscillation frequency of the proposed circuit, whilst keeping the other three resistance values constant, a capacitance of 7.02 nF would be required. Such capacitance dictates an unfeasibly large on-chip area of 2.828 mm × 2.828 mm with a typical current technology. Conversely, the memristor used in this implementation has a cross-point structure measuring 50 nm × 50 nm. This yields a

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total circuit area for the proposed oscillator of 348 μm^2. Additionally, the proposed oscillator offers the benefit of simple post-fabrication tunability.

The oscillator described above also provides a toolbox with which to build a neuromorphic circuit emulating the Hodgkin-Huxley dynamics. Modifying the circuit resistances and adding a pulse voltage source in Path 1 between R_3 and ground, results in a system that stays inactive in the absence of stimuli and produces spiking behavior when stimulated with a 100 mV input, as shown in Figs. 5.6 - 5.7. This is in accordance with the Hodgkin-Huxley model for the nerve axon membrane, where an above-threshold depolarization potential produces a train of pulses for as long as it is applied.

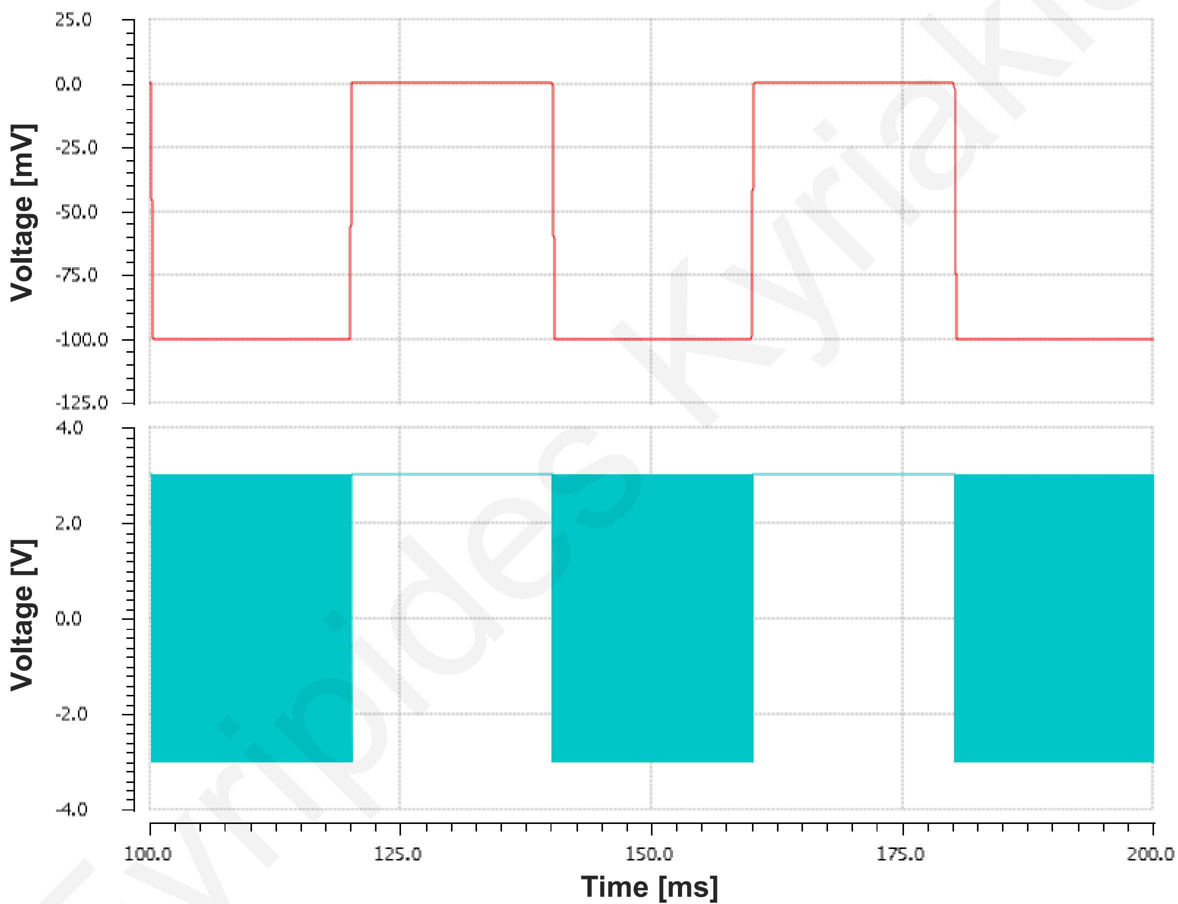

Figure 5.6: Oscillator behavior with respect to input pulses. Top: Input pulses. Bottom: Output oscillations.

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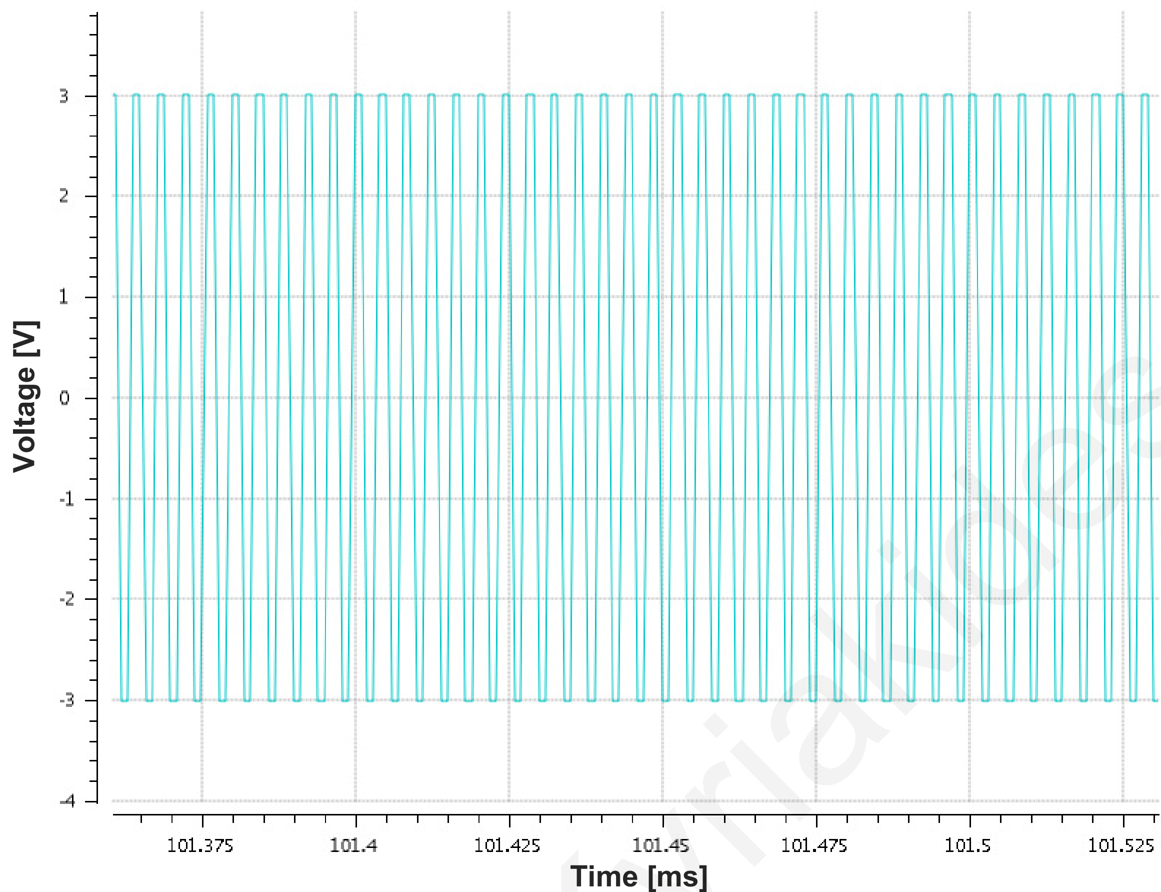

Figure 5.7: Oscillator output oscillations with pulse input, visible in higher time resolution.

5.3 Learning network

CMOS technology and by extension the classical von Neumann computer architecture have so far failed to mimic the capabilities of biological organisms. Nature's paradigm involves information storage and processing happening at the same place, the synapse. Compared to CMOS technology, this has proven faster and more energy efficient, as well as adaptable [134]. Using memristors it becomes possible to design biomimetic spiking neural networks emulating nature's paradigm. The use of memristor devices, along with biomimetic neurons, and their exploitation in a neuromorphic circuit, is hereby presented. This is intended as a working example of how these devices can be used in a bioinspired circuit to accomplish cognitive tasks.

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For the purpose of the following work, Cu/Ta_2O_5 memristors have been fabricated as reported in Chapter 4. The characterization and modeling of these devices is reported in the same chapter. The fabrication and characterization of Leaky Integrate-and-Fire (LIF) neurons is hereby reported. The neurons draw analogies from biological neurons and, in a spiking network of such neurons connected via synapses, the memristor devices are used to emulate the plasticity exhibited by biological synapses. The outcome is the modification of the system's output depending on past input.

Using the results obtained from the electrical characterization, the behavioral models of the fabricated Cu/Ta_2O_5 structures were represented in Verilog-A. The coded modules were introduced in Cadence analog environment. After obtaining the results of the separate modules and complete circuit simulations - with the introduction of the memristor model - using Cadence Spectre, Cadence Virtuoso was used to design the circuit physical layout. The resulting mask layout (tape-out) of the complete neural circuit was sent for fabrication. This was effectively the neural circuit minus the memristor devices. In a later stage the two circuits were wire-bonded in a complete package. The resulting implementation of the neural circuit was tested for its desired traits. Evaluation of the implementation and a comparison with transistor-based implementations of comparable functions are presented at the end of the chapter.

5.3.1 Design

The circuit aims to showcase the functionality of a memristor as an electronic equivalent of the biological synapse. With the completion of the phases concerning device fabrication, characterization and modeling, the neural circuit could then be designed. The neural circuit was built around the fabricated memristors and was designed using the aforementioned models.

The aim is to demonstrate synaptic plasticity in a network consisting of neurons and synapses. The neuron functionality is accomplished through the use of LIF neurons and the synaptic functionality through memristor devices. This is showcased by the connection of source and target neurons through memristors, as in Fig. 5.8 shown below. The source neurons are activated by a current source to send spikes through a memristor while the target neuron's spiking is observed. Multiple source neurons are connected to a single

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target neuron. It is expected that the source neuron activated more frequently will cause the memristor's resistance to diminish, thereby causing a change in the output neuron spiking. Consequently, by detecting the target neuron's spiking pattern, it becomes possible to identify which of the source neurons is activated at a given time.

The electronic synapse's function is revealed in a circuit designed to exhibit synaptic plasticity. The fabricated circuit includes three LIF neurons. A memristor is placed between two neurons in two paths. The first (input) neuron integrates an externally supplied current to produce output spikes. Because of the memristor devices' sensitivity to high currents, these spikes are modulated through a current limiter in order to restrict the maximum input current. The current limiter output is then supplied to the memristor and the memristors' output is supplied to the second (output) neuron.

The memristor resistance is dependent on its prior inputs. Therefore, the more current is channeled through the memristor (with the correct polarity) the more conductive it becomes. Based on this principle, two cells with a combined output neuron have been tested to emulate synaptic plasticity (Fig. 5.8).

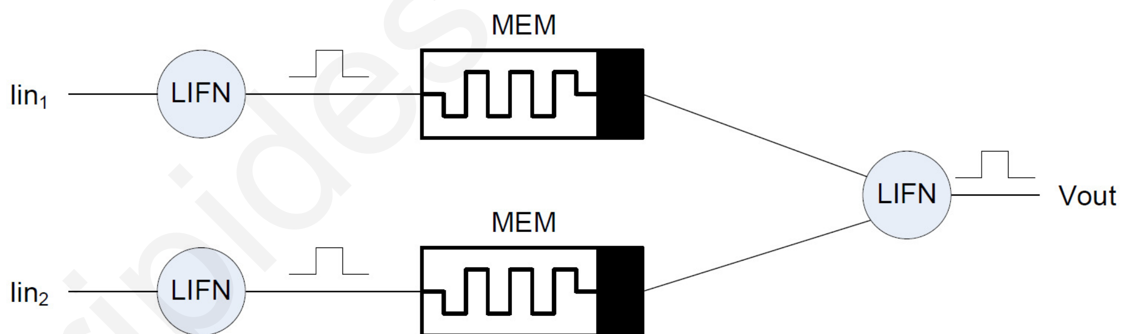

Figure 5.8: Block diagram of synaptic plasticity network with two input and one output LIF neurons, connected with two memristors.

Initially, each input neuron is fed with current and the output neuron's output voltage is measured. This sets the benchmark for the depressed synaptic state. This is followed by the training period, where one of the two input neurons is supplied with positive current, resulting in memristor potentiation. The result of the training is that, with identical current

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fed to each of the two input neurons (in sequence), the potentiated connection causes the output neuron to generate greater pulses in both amplitude and duration than the depressed one. This exhibits learning in one of the synapses, similar to the manner with which biological nervous systems encode information.

5.3.2 LIF neuron

The fundamental component of the neural circuit, besides the memristor, is the LIF neuron. The LIF neuron circuit's diagram is shown in Fig. 5.9. The LIF neuron circuit's schematic and layout are included in Appendix D. The implementation is an adaption of the one presented by Chicca et al. [147]. It integrates the incoming current and produces a voltage spike at the output whenever an internal threshold voltage is reached.

The neuron accepts externally generated currents as inputs that are integrated on two capacitors. The incoming current is defined as I_{exc} - I_{inh}, mimicking excitatory and inhibitory inputs to a biological cell. This charges capacitors C_1 and C_2, building up the "soma" voltage V_{sm}, which has the analogous function to a cell's membrane potential. Once V_{sm} reaches a defined threshold (akin to the axon hillock's threshold), a spike is generated. The threshold is defined as a value of internal voltage V_{sm}. Two inverters are then responsible for the generation of the output spike once V_{sm} reaches a predefined threshold, as shown in Fig. 5.10. During the spike the two capacitors are discharged through V_{dis}. Furthermore, a leakage line controlled through V_{leak} ensures the volatility of the neuron.

The voltage output is then fed to a current limiting stage, necessary due to sensitivity of the memristor devices to high currents. The current limiter is adjustable, with regards to its output, in the nanoamp range.

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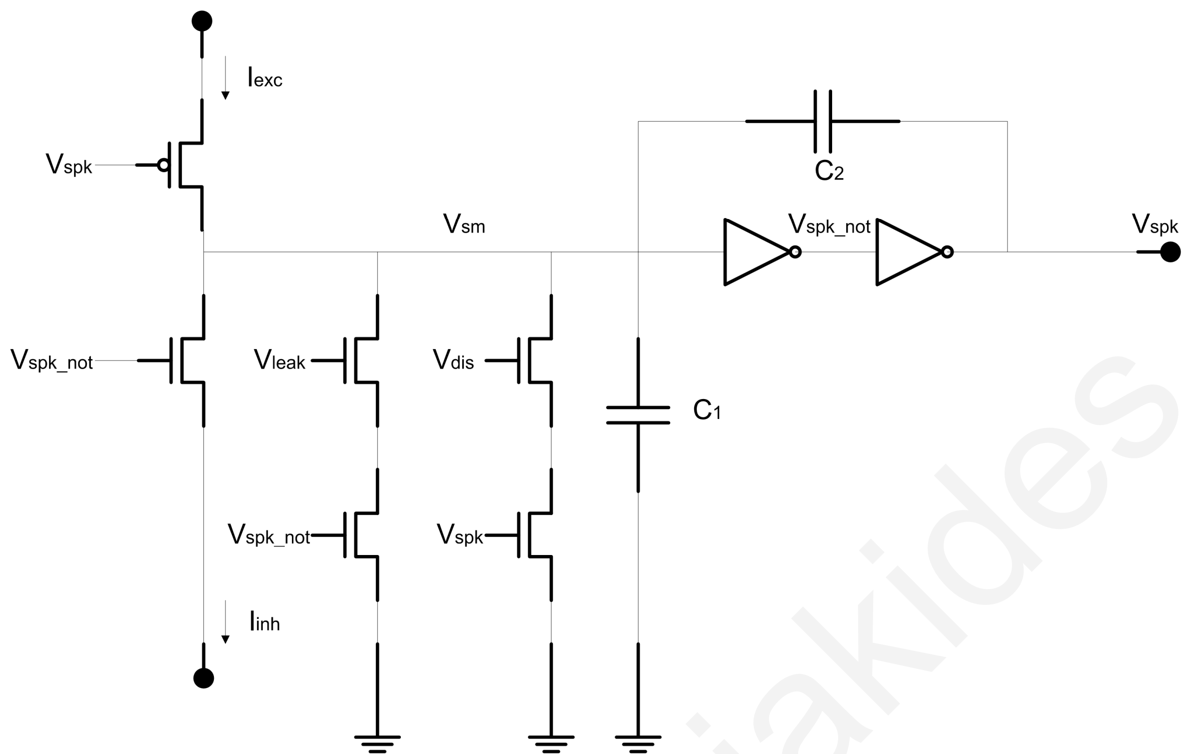

Figure 5.9: Schematic of the LIF neuron module.

Optimization of the circuit sought to define the capacitors' sizes in conjunction with the leakage and discharge currents to produce the required output from low-level input. The leakage and discharge currents are controlled by the voltage on transistors V_{leak} and V_{dis} (acting as high-level pseudo resistors) of Fig. 5.9. This resulted in capacitor values of 500 fF for capacitor C_1 and 1 pF for capacitor C_2. The voltage levels were determined as 320 mV for V_{leak} and 600 mV for V_{dis}.

The circuit of Fig. 5.9 was realized in Cadence Virtuoso (Fig. D.2), where simulations resulted in defining the spiking characteristics of the LIF neuron. The determined values were used to design the circuit layout shown in Appendix D. A verification procedure, matching layout and schematic views, is essential before the circuit proceeds to fabrication.

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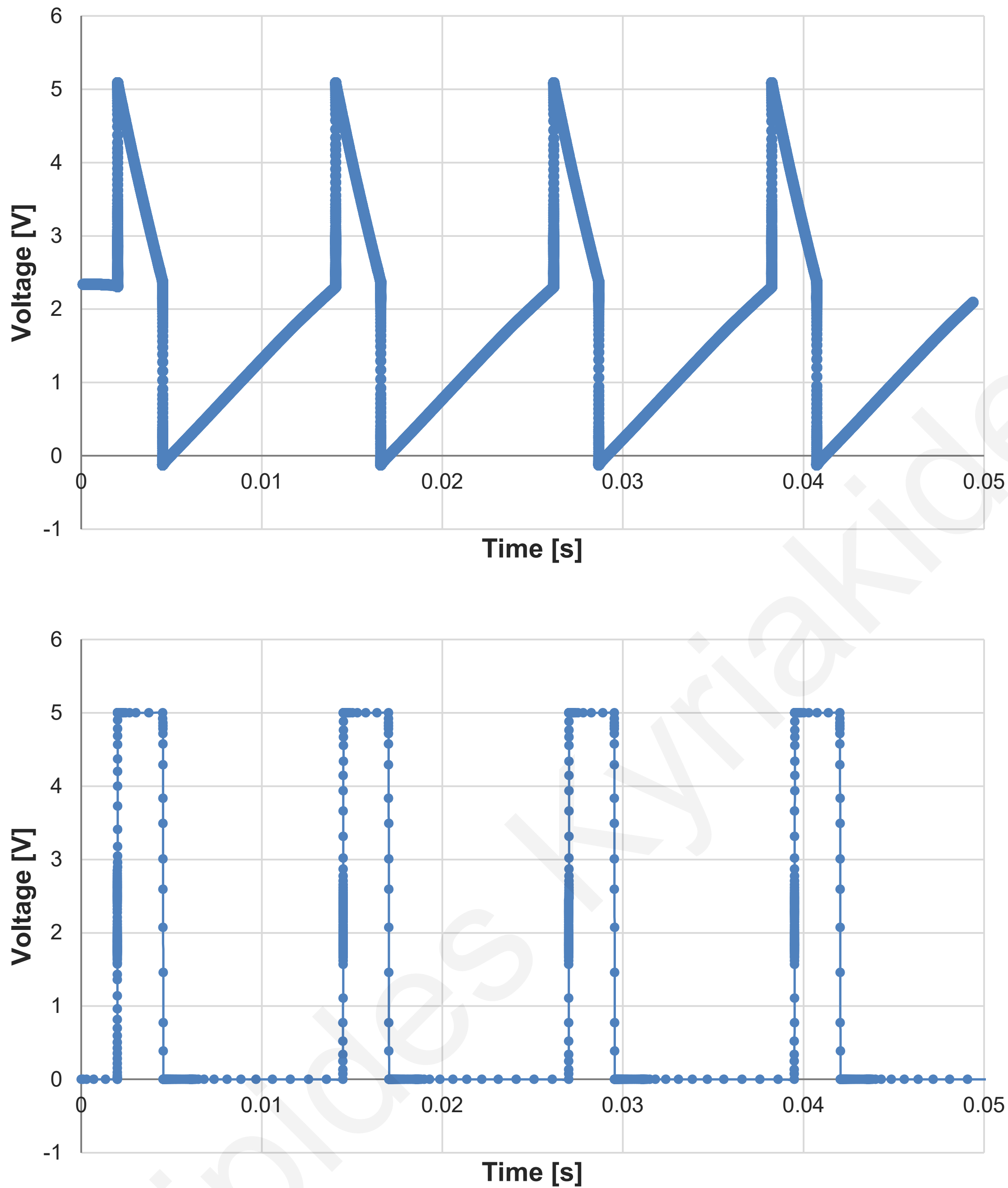

Figure 5.10: Simulated traces of internal voltage V_{sm} (top) and output voltage V_{spk} (bottom) showing integrate-and-fire functionality of LIF neuron.

5.3.3 Modules

As previously noted, the neuron integrates incoming currents and outputs a voltage spike. Since the fabricated memristors showed intolerance to high currents, the current created by

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the neuron output needed special consideration. The LIF neuron input was adjusted to work with the low currents required by the memristors' compliance. However, the output had to be limited before it reached the next memristor in the circuit. A current limiter was thus deemed necessary. The current limiter, shown in Fig. 5.11, takes V_{in} from the neuron output and generates a current output that is limited to the desired level. Therefore, the spike generated by the neuron reaches the next stage (e.g. a memristor) but is limited to I_{in}, the current limiter's other input.

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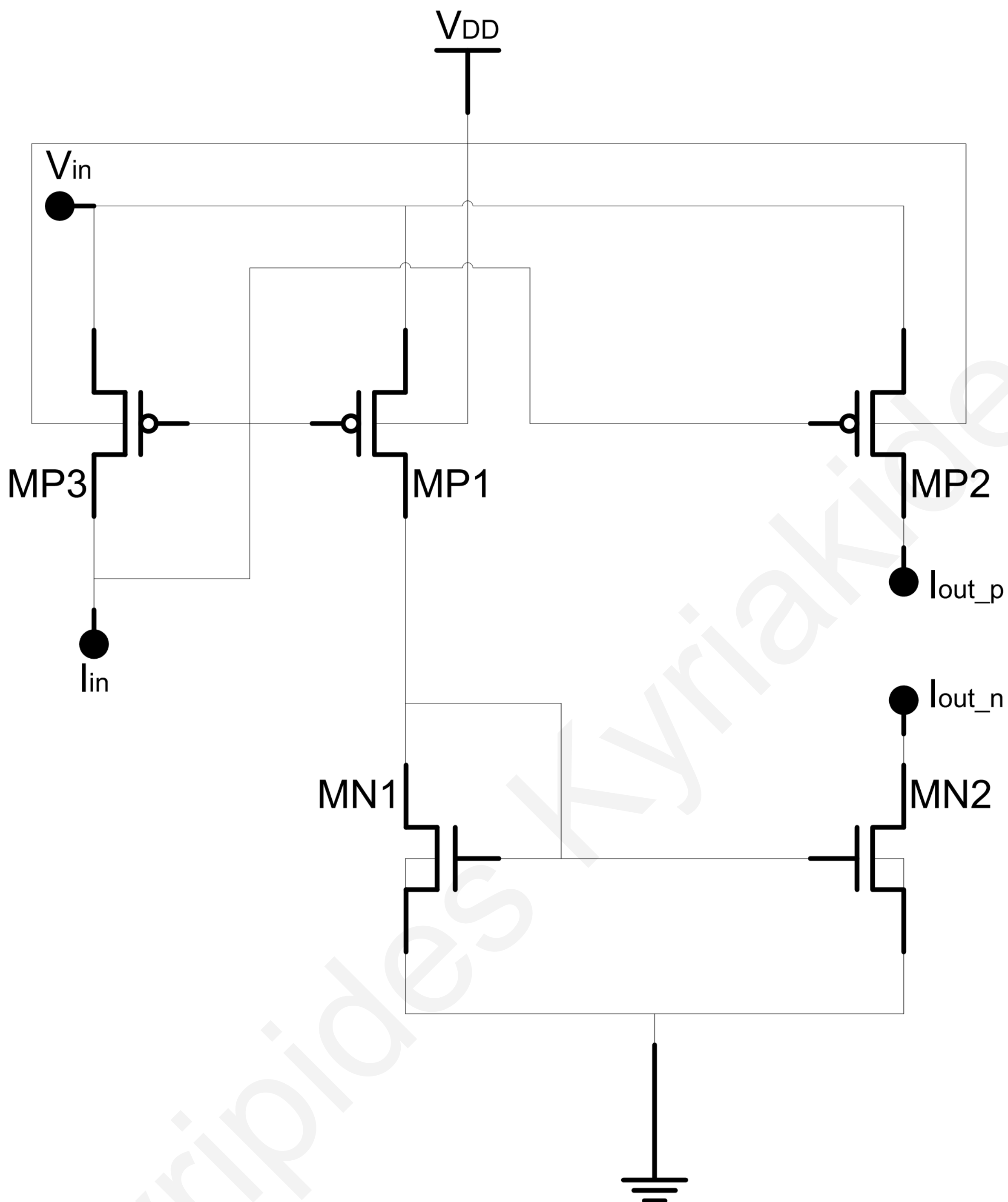

Figure 5.11:Schematic of the current limiter module. V_{in} represents the of the previous stage and I_{in} the threshold current applied to it.

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The current limiter's input current, I_{in}, was defined by the characterization of the Cu/Ta_2O_5 devices of Chapter 4. The characterization defined an upper limit on the memristor current in the range of nanoamps. Such low current levels are not easily obtainable using standard foundry elements. Therefore, a current source had to be designed that precisely and reliably gave such low currents. The resulting current reference module

is shown in Fig. 5.12. It supplies constant nanoamp-range currents independent of temperature. This is attained by summing two currents, one proportional and one complimentary proportional to the temperature and supply voltage, using feedback.

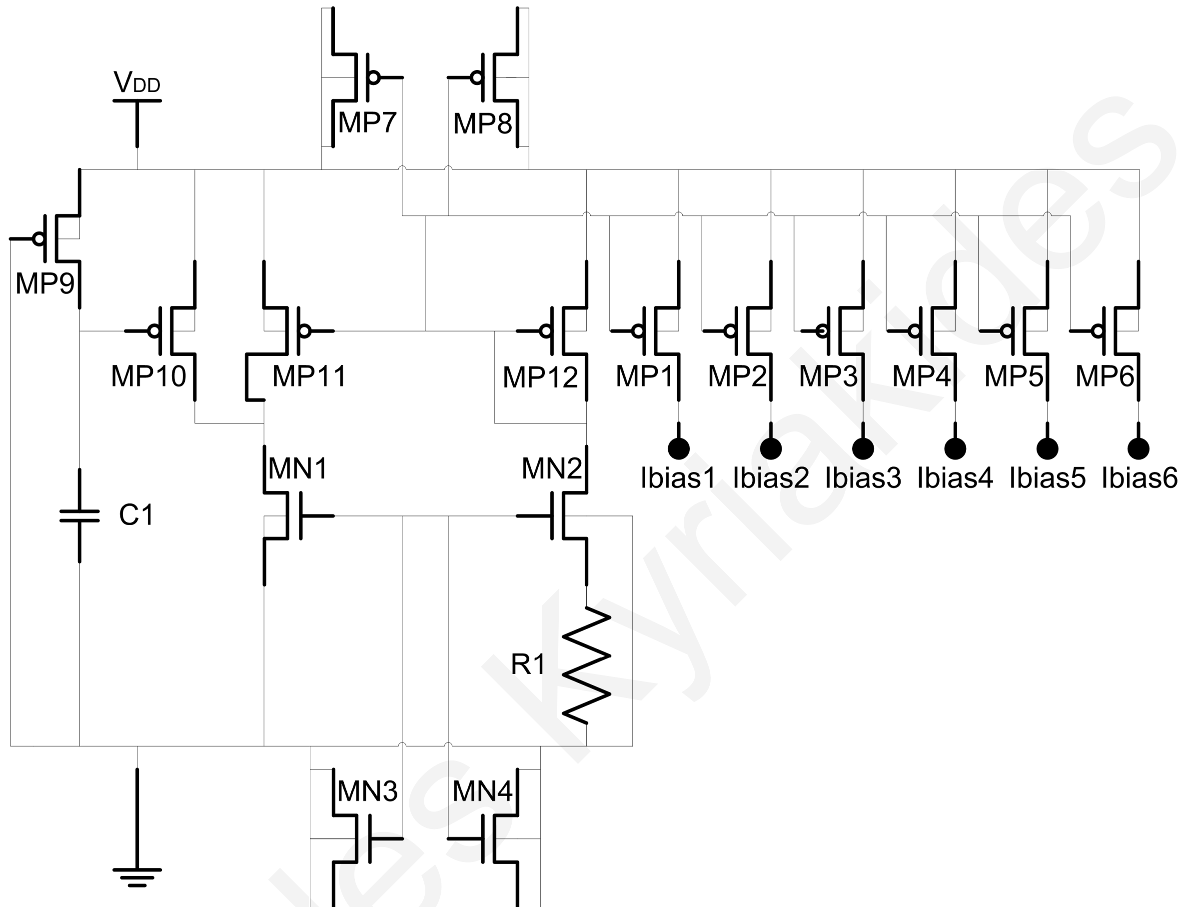

Figure 5.12: Schematic of the current reference module.

Various components of the circuit require the low-level currents generated by the current reference module. To accommodate multiple neurons on each die without the need for multiple current reference modules, a current mirror module was designed. The current mirror module mirrors its input to a total of six outputs with the accuracy required for such low-level currents. The bias current defines V_{GS} on the reference transistor, which is then forced on the mirroring transistors. Provided: (a) V_{DG} is zero, and (b) all transistors are matched, such being the case, then outputs $I_{mirror1}$ - $I_{mirror6}$ are equal to I_{bias}. The schematic of the current mirror module is shown in Fig. 5.13.

As a result of foundry space constraints, six LIF neurons and peripheral components were included in a top cell. Two current references and two current mirrors were required

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for each cell. A current limiter is necessary for each LIF neuron. The top cell schematic and matching layout are included in Appendix D.

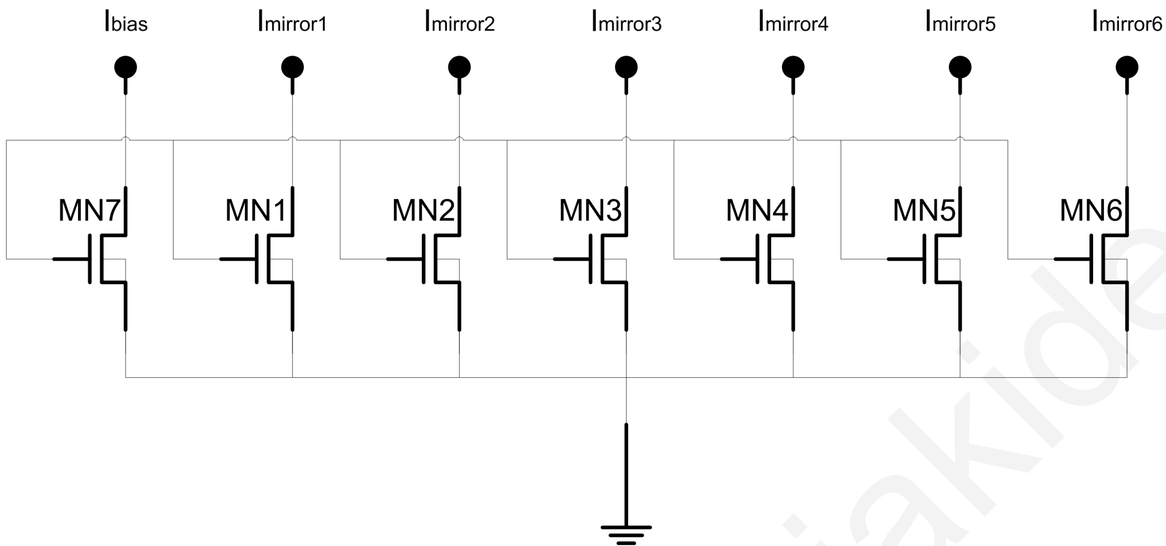

Figure 5.13: Schematic of the current mirror module.

5.3.4 Characterization

Due to process variation and low-level currents, the neuromorphic chip must be tested for its compliance to specifications. Starting hierarchically, the individual components of the circuit are tested and their functionality explained. The necessary connections and instruments are listed below. This leads to the final network test, where the neuromorphic network shown in Fig. 5.8 is tested. Schematics included in Appendix D illustrate each procedure.

The instruments used for the measurements comprise a Keithley 4200-SCS Parameter Analyzer, a National Instruments PCI-4462 Dynamic Signal Acquisition Module, and a custom made current-to-voltage converter. These instruments are presented in Chapter 4. Additionally, a Keithley 236 SMU, shown in Appendix B, is utilized as a power supply and ground. The connection configuration is either coaxial (coax) or triaxial (triax) wiring.

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Current reference module

The current reference module is a current source that accurately produces the low currents required in the circuit. The module supplies six distinct picoamp- to nanoamp-range currents independent of temperature.

To test the current reference module (Fig. 5.14), each output current is measured and compared to the nominal one. The smallest discrepancy between the two values is desired. The necessary connections are VDD, GND, and PADs 1 through 6. VDD is set at 5 V and the currents from PADs 1 through 6 are measured. The nominal currents range from 0.212 pA to 10.3 nA, as shown in Tab. 5.1. The picoamp and nanoamp current levels necessitate the use of triax connections to instruments for accuracy. The detailed connection diagram is included in Appendix D.

Signal	Instrument	Configuration	Source Value	Expected Value
VDD	Keithley 236	Triax	5 V	
GND	Keithley 236	Triax	Ground	
PAD 1	Keithley 4200	Triax		212 pA
PAD 2	Keithley 4200	Triax		463 pA
PAD 3	Keithley 4200	Triax		1.09 nA
PAD 4	Keithley 4200	Triax		2.23 nA
PAD 5	Keithley 4200	Triax		5.90 nA
PAD 6	Keithley 4200	Triax		10.3 nA

Table 5.1: Current reference module test particulars.

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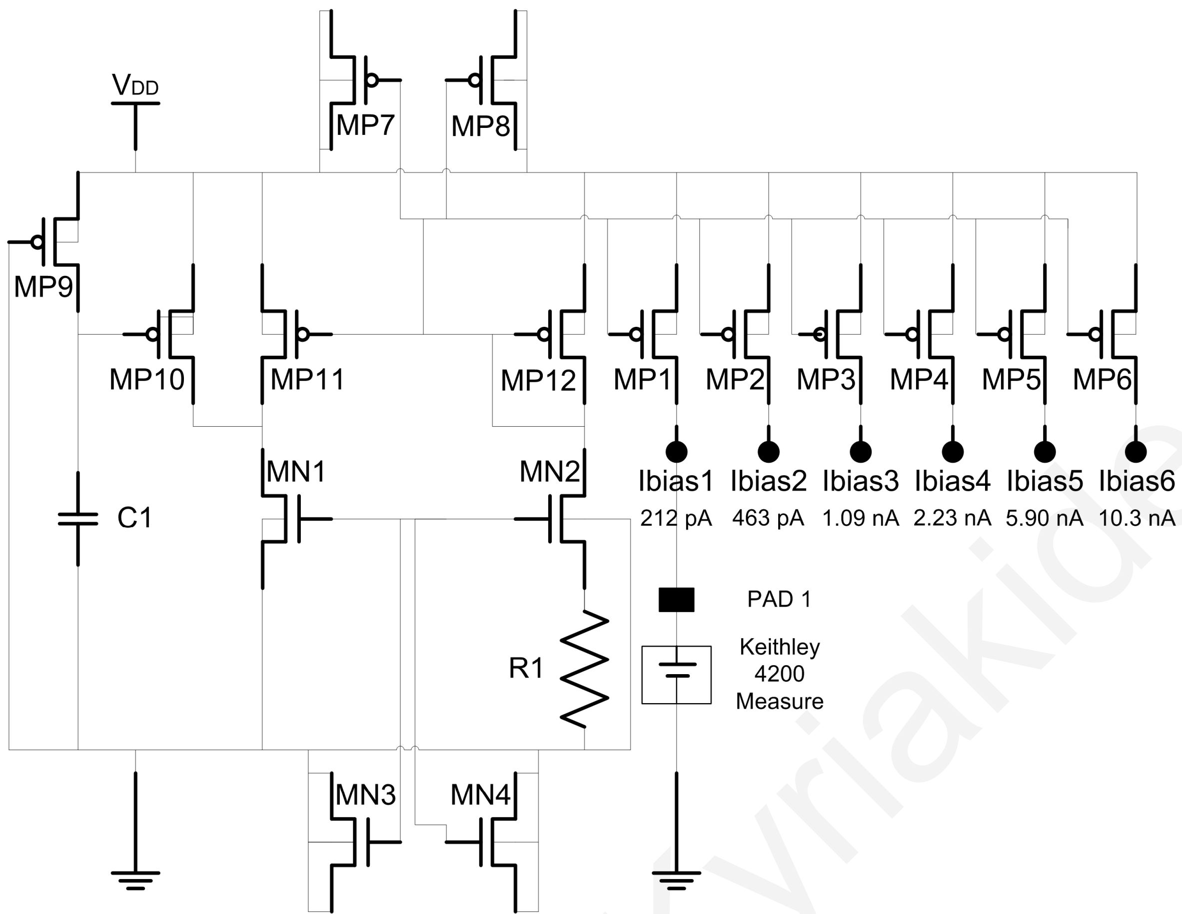

Figure 5.14: Current reference module test setup.

Current mirror module

The current mirror module is designed to accurately mirror the input current to its six outputs. It is designed to function in the nanoamp range, so currents between 1 - 10 nA should be reliably reproduced.

To test the current mirror module (Fig. 5.15), a DC current sweep is sourced to I_{biasL} and the output current of I_{mir}-V_{sm1} is measured. The necessary connections are VDD, GND, I_{biasL} and I_{mir}-V_{sm1}. VDD is set at 5 V and maximum voltage compliance of I_{biasL} is set at 3 V. The test parameters are listed in Tab. 5.2 and the expected result, as calculated through Cadence Virtuoso simulations, is shown in Fig. 5.16. Triax connections are used for sourced and measured currents due to their low level. The detailed connection diagram is included in Appendix D.

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Signal	Instrument	Configuration	Source Value	Expected Value
VDD	Keithley 236	Triax	5 V	
GND	Keithley 236	Triax	Ground	
I_{biasL}	Keithley 4200	Triax	1 - 10 nA	
I_{mir}-V_{sm1}	Keithley 4200	Triax		1 - 10 nA

Table 5.2: Current mirror module test particulars.

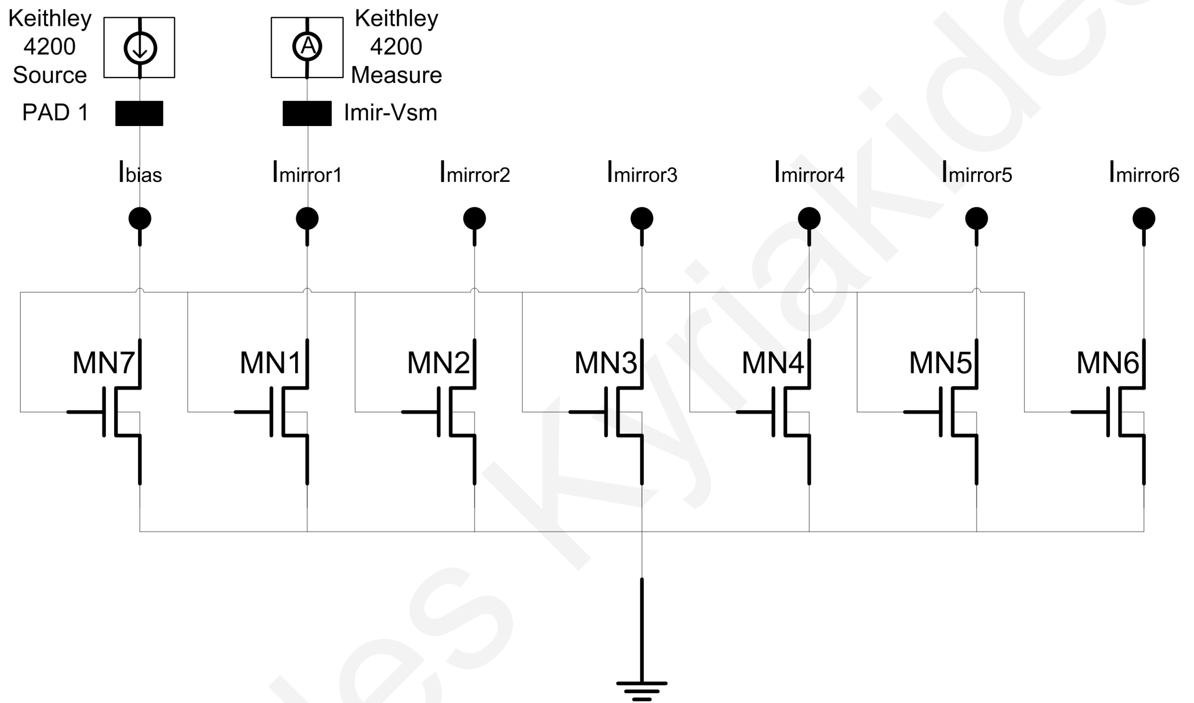

Figure 5.15: Current mirror module test setup.

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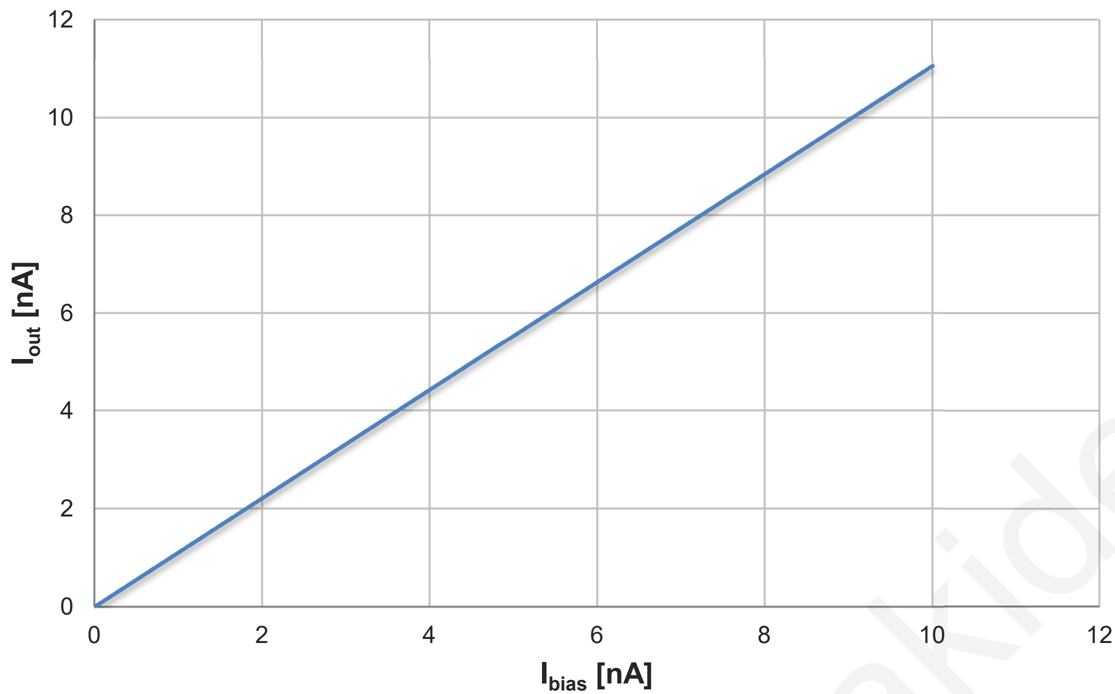

Figure 5.16: Current mirror module expected result through simulations.

LIF neuron

The LIF neuron is designed to integrate the current input (excitatory minus inhibitory) by charging two internal capacitors. Once an internal voltage level has been reached (equal to its predefined threshold), a spike should be produced at its output, discharging the internal capacitors. Continued current input should produce a series of spikes.

To test the LIF neuron circuit (Fig. 5.17), a DC sweep is performed on input I_{exc1} while V_{spk6} is measured. The necessary connections are VDD, GND, V_{pw}, V_b, I_{exc1}, and V_{spk6}. A triax connection is required for the input current. VDD is set at 5 V, V_{pw} at 600 mV, V_b at 320 mV, I_{exc1} is swept in the nanoamp range, while V_{spk6} is measured with expected range 0 - 5 V. The test parameters are listed in Tab. 5.3. The result should reproduce the pulsed waveform shown in Fig. 5.18. The LIF neuron is designed to produce 2.5 ms, 3.5 V spikes at 1 nA input current. I_{exc1} maximum voltage compliance is set at 3 V. The input impedance of the NI PCI-4462 is 1 MΩ. The detailed connection diagram is included in Appendix D.

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Signal	Instrument	Configuration	Source Value	Expected Value
VDD	Keithley 236	Triax	5 V	
GND	Keithley 236	Triax	Ground	
V_{pw}	Keithley 4200	Coax	600 mV	
V_b	Keithley 4200	Coax	320 mV	
I_{exc1}	Keithley 4200	Triax	0.1 – 10 nA	
V_{spk6}	NI PCI-4462	Coax		0 - 5 V

Table 5.3: LIF neuron circuit test particulars.

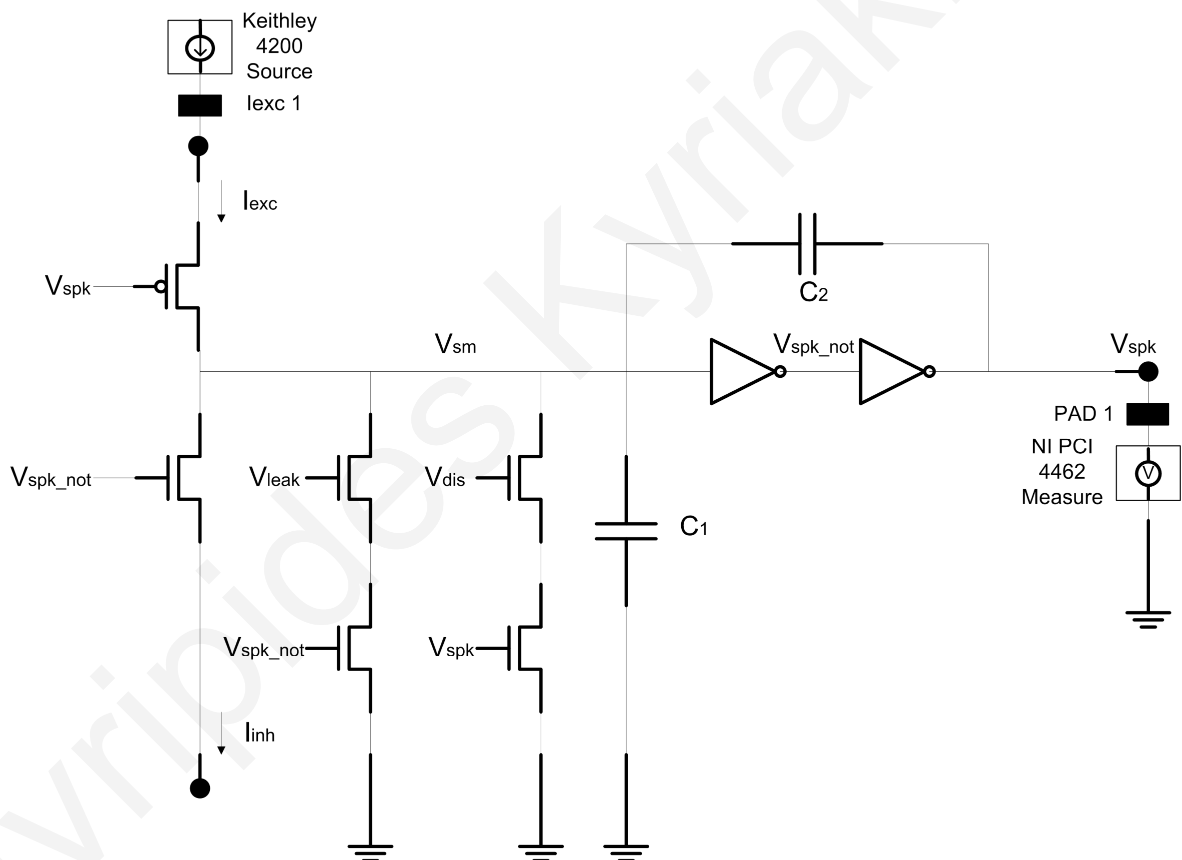

Figure 5.17: LIF neuron test setup.

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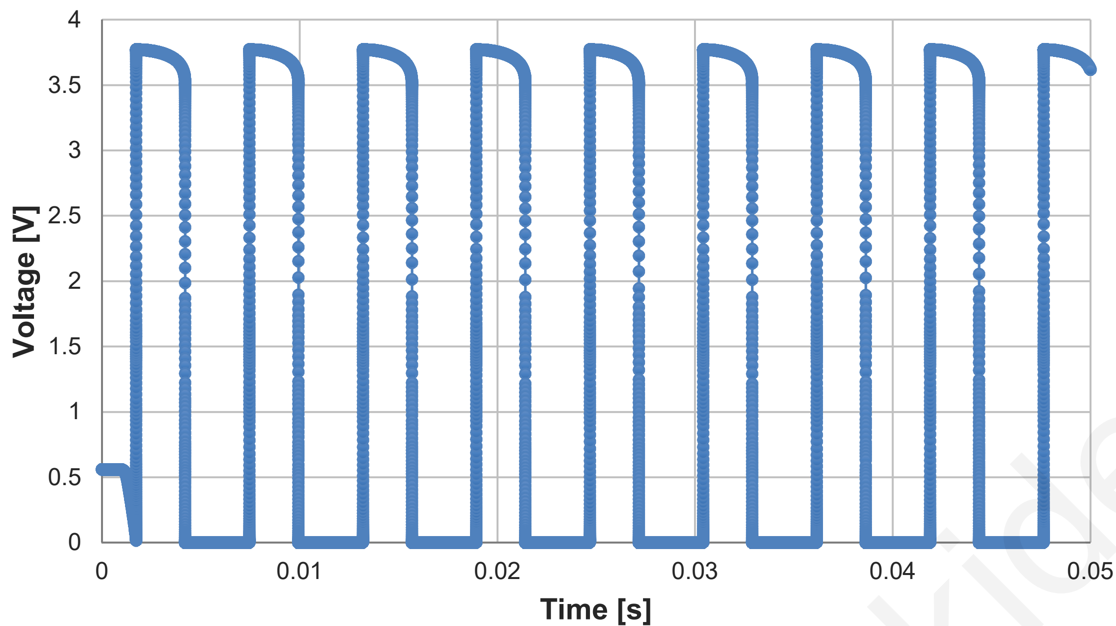

Figure 5.18: Simulated LIF neuron output waveform at 1 nA input current.

LIF neuron with current limiter module

The current limiter is designed to limit the maximum current going into the memristor. The maximum current is defined by a second input to the current limiter (I_{bias}). This current compliance affects the peak of the output spikes in the current domain.

To test this function, namely, the LIF neuron with the current limiter circuit (Fig. 5.19), the current-limited output spikes of the neuron must be measured. The appropriate (as determined from above) I_{biasR} is connected to I_{exc1} to drive the neuron. Afterwards, a DC current sweep is performed on I_{biasR} input and measure Iout_exc 1 to test for maximum current out of the chip. I_{out_exc1} will be converted to voltage through the OPA128 module and measured using the NI PCI-4462. The necessary connections are VDD, GND, V_{pw}, V_b, I_{biasR}, and I_{out_exc1}. VDD is set at 5 V, V_{pw} at 600 mV, V_b at 320 mV, I_{biasR} is swept, and I_{out_exc1} is measured. I_{biasR} maximum voltage compliance is set at 3 V. The input impedance of the NI PCI-4462 is 1 MΩ. The expected result, as illustrated in Fig. 5.20, is a cap on the current output, set by the input current (set here at 1.5 nA). The artifact shown in Fig. 5.20 in the form of an initial overshoot in current could not be avoided, however it was deemed neither high enough in amplitude nor long enough in duration to modify the fundamental operation of the current limiter. As shown in Tab 5.4, the sourced and measured currents

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are in the picoamp to nanoamp range, therefore triax connections are used. The detailed connection diagram is included in Appendix D.

Signal	Instrument	Configuration	Source Value	Expected Value
VDD	Keithley 236	Triax	5 V	
GND	Keithley 236	Triax	Ground	
V_{pw}	Keithley 4200	Coax	600 mV	
V_b	Keithley 4200	Coax	320 mV	
I_{biasR}	Keithley 4200	Triax	0.1 – 10 nA	
I_{out_exc1}	NI PCI-4462	Triax		0.1 – 10 nA

Table 5.4: LIF neuron with current limiter module test particulars.

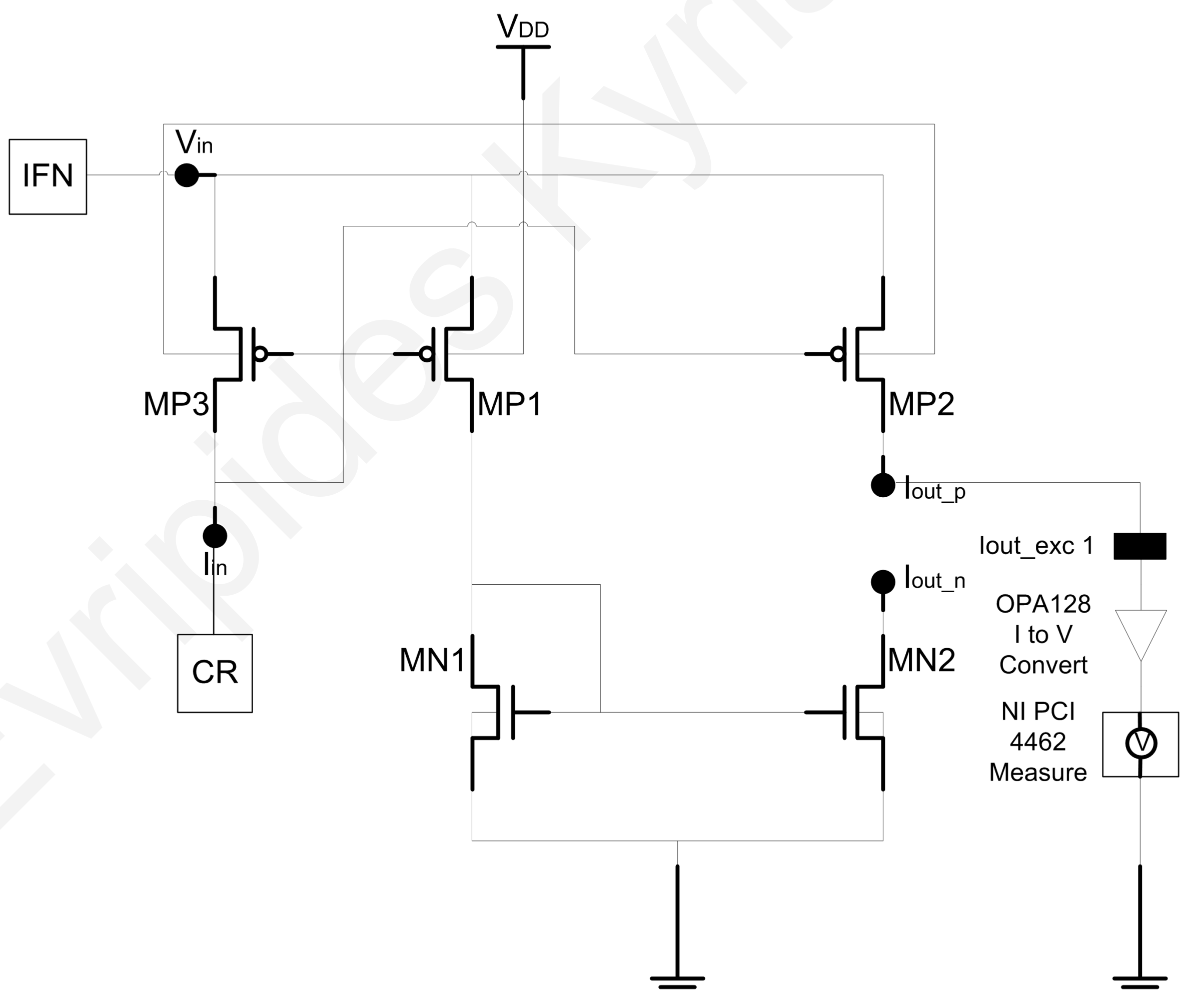

Figure 5.19: LIF neuron with current limiter module test setup.

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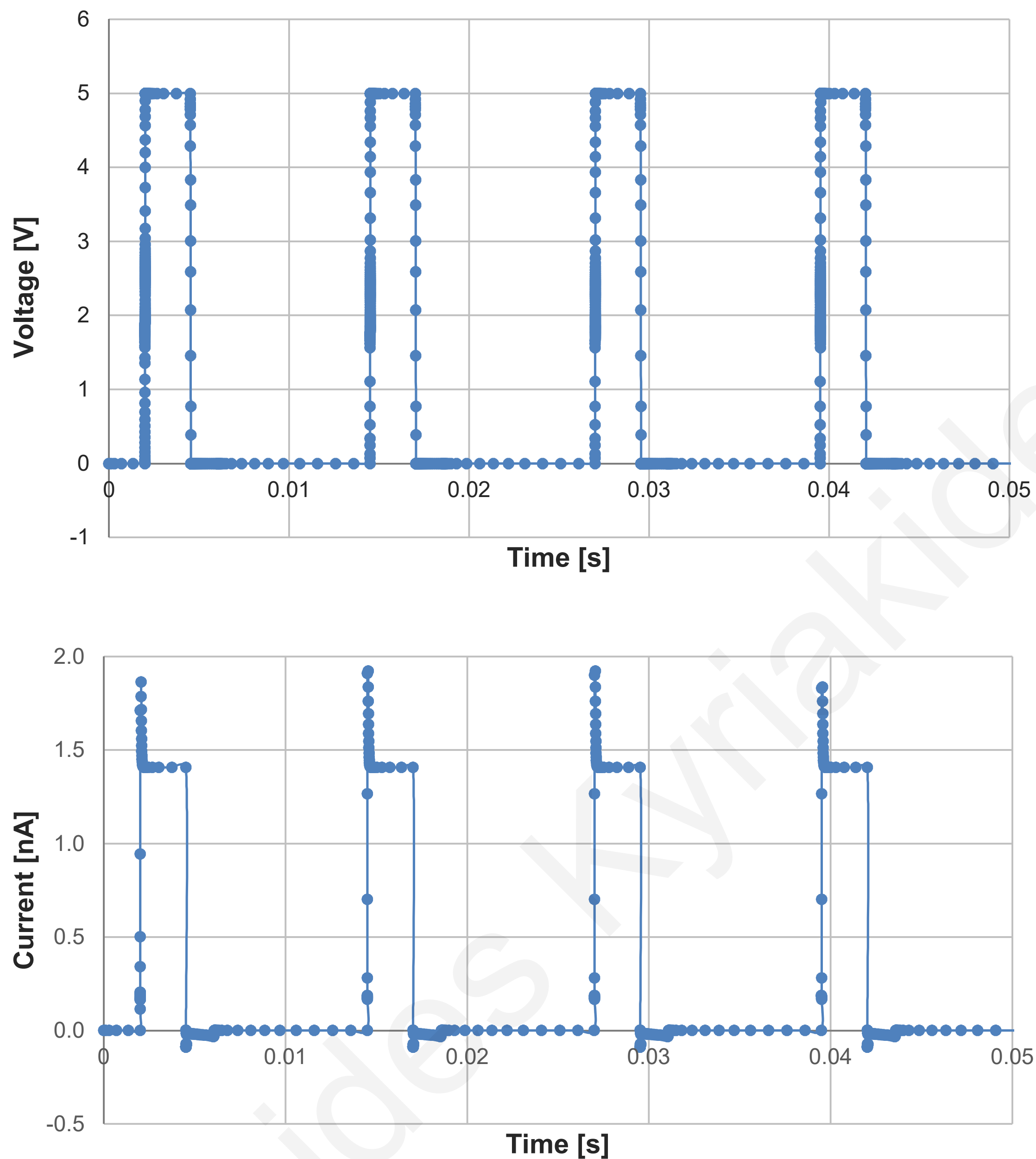

Figure 5.20: Simulated LIF neuron output voltage (top waveform) and associated current limiter module output current (bottom waveform) showing current limiter operation.

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Network

The network connects "input" LIF neurons to "output" LIF neurons through memristors. The "input" neurons are meant to train the intervening memristors by continuous spiking. The effect of training is seen in the "output" neurons. An untrained synaptic connection (i.e. memristor) will produce the measured depressed spiking. A trained synaptic connection will produce the measured potentiated spiking.

Thus, the aim is to demonstrate synaptic plasticity by connecting input and output LIF neurons through memristors, as in Fig. 5.21 below. To test the network function, i.e. two LIF neurons connected through a memristor, the connections are configured as in Fig. 5.22 below. The intervening memristor, which is not shown in the schematic, is connected between I_{out_exc1} and I_{exc1}. The procedure is summarized within the test schematic. The "input" LIF neuron is activated to send spikes through the memristor while the "output" LIF neuron's spiking is observed (Fig. 5.23). The memristor's plasticity is expressed by its diminishing resistance, as seen in Fig. 5.24 below.

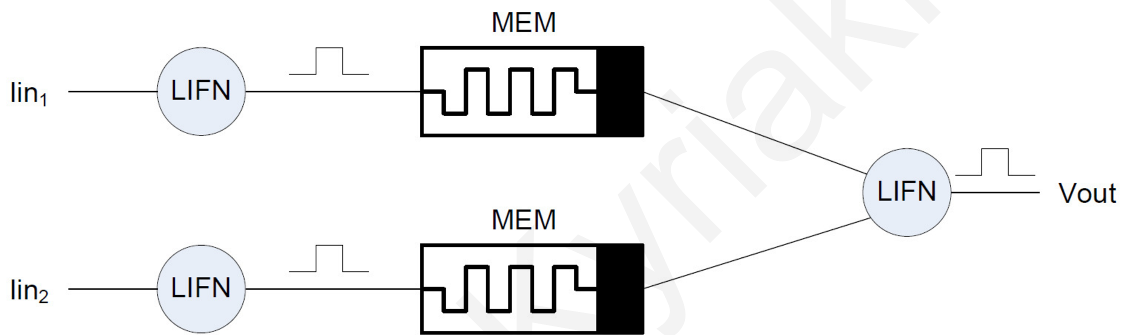

Figure 5.21: Synaptic plasticity connection diagram.

For the input LIF neurons, I_{exc1} and current limiter are connected to the appropriate (as determined from above) I_{bias} chip pads to drive the neuron and limit the current limiter output, respectively. Each I_{out_exc1} is fed to a memristor. All memristor outputs are connected to a single output LIF neuron through I_{exc1}. The output LIF neuron's V_{spk} output, constituting the output signal of the network, is then measured. The necessary connections, shown in Fig. 5.22 below, are VDD, GND, V_{pw}, and V_b for both LIF neurons. The input LIF neurons will also connect to a memristor through I_{out_exc1}. The output LIF neuron will be connected to the memristors through I_{exc1} and to the NI PCI-4462 through V_{spk}. As shown in Tab 5.5, VDD is set at 5 V, V_{pw} at 600 mV, V_b at 320 mV, and V_{spk} is measured. The input impedance of the NI PCI-4462 is 1 MΩ.

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Signal	Instrument	Configuration	Source Value	Expected Value
VDD	Keithley 236	Triax	5 V	
GND	Keithley 236	Triax	Ground	
V_{pw}	Keithley 4200	Coax	600 mV	
V_b	Keithley 4200	Coax	320 mV	
V_{spk6}	NI PCI-4462	Coax		0 - 5 V

Table 5.5: Network function test particulars.

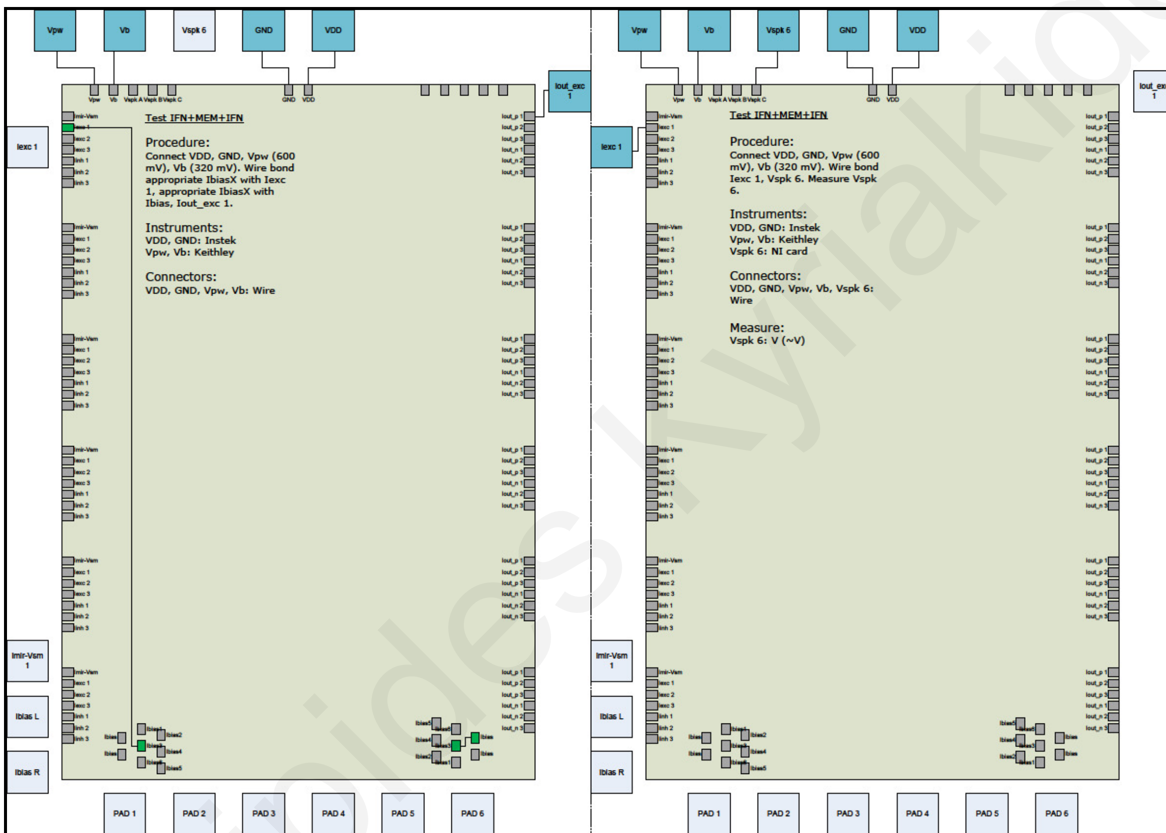

Figure 5.22: Network test diagram and description showing connection between input and output neurons. Used pads are shown as green, whereas unused ones are shown as grey.

Simulating the LIF neuron's spiking with different excitation currents (Fig. 5.23) predicts the change expected in the output waveform. Increasing current causes elongation of the pulse duration and period.

The memristor's resistance is deduced through output current and comparison of the first output pulse after 100 ms, 200 ms, and 300 ms of continuous excitation (Fig. 5.24). The gradual increase in the pulse shape delineates the memristor's diminishing resistance.

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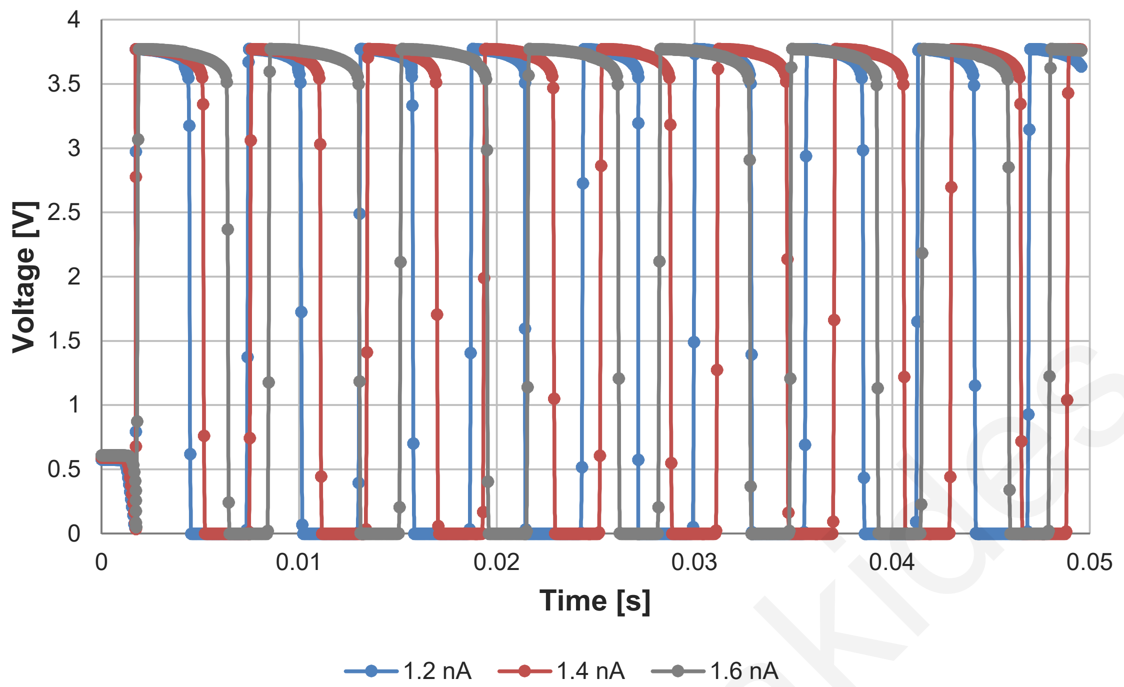

Figure 5.23: LIF spiking evolution simulation with increasing excitation current at 1.2 nA, 1.4 nA, and 1.6 nA.

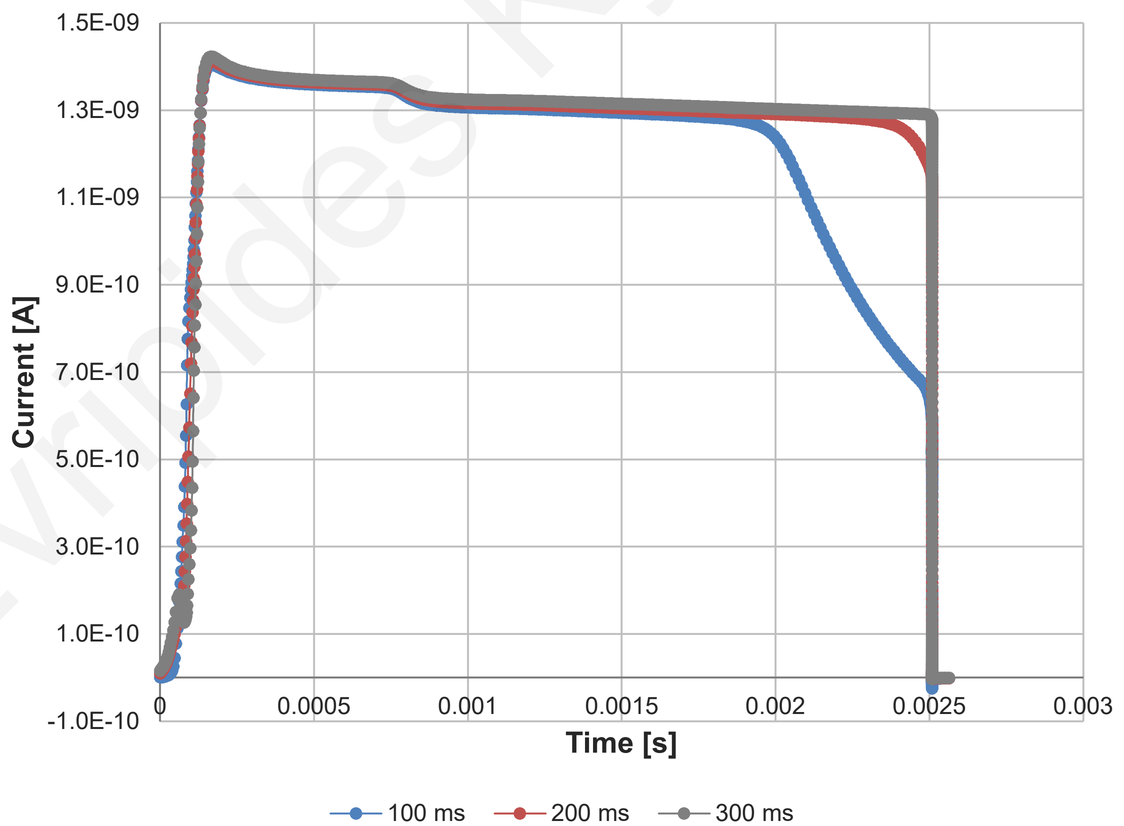

Figure 5.24: Gradual potentiation of memristor element. The memristor output is simulated and the spikes after 100 ms, 200 ms, and 300 ms are compared.

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Assembly

The designed circuit was completed in Cadence Virtuoso and sent to ams AG, Styria, Austria, a semiconductor foundry, for fabrication. The chips produced were placed on a package for testing. A package/socket combination can be connected to instrumentation using a PCB. Initial testing involved the chip with regards to its designed functionality. In a subsequent stage, the memristor dies were placed adjacent to the chips to complete the network.

The component dimensions are: (a) memristor die: 4.5 mm × 3.5 mm, and (b) ams chips: 4 mm × 2.5 mm. The package used was chosen to measure 10.5 mm × 10.5 mm in order to accommodate the aforementioned components yet not require long bonded wires. Placement of the chips on the package is done using epoxy adhesive. Wires are then placed using the F & K Delvotec 53XX wire bonder. The wire bonding procedure involves gold wires drawn between the chip and memristor pads on one side, and the package pads on the other. The wire bonded package containing the circuit chips and memristor dies is shown in Fig. 5.25. The package's bonding diagram is included in Appendix D.

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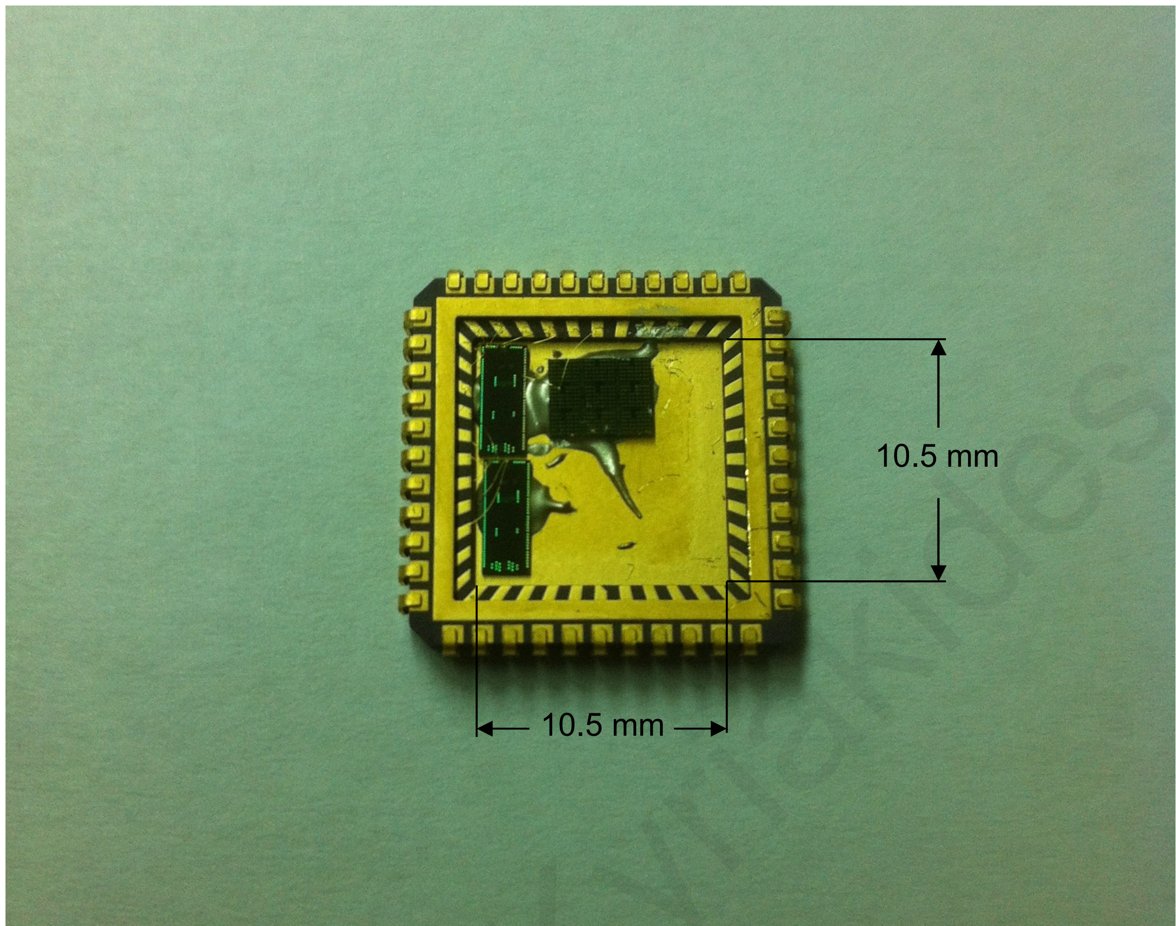

Figure 5.25: The 10.5 × 10.5 mm^2 package wire bonded with circuit chip and memristor dies.

The package was fitted into a 44-pin PLCC socket for linking with external instruments. The socket's connection diagram between internal pads and external pins can be seen in Appendix D. The socket is subsequently fitted to a Printed Circuit Board (PCB), milled specifically for this setup.

A PCB is necessary to complete the test setup. Thus, a PCB was designed using Altium Designer. The PCB provides connections between the 44 pins available on the socket to external instrumentation. The design files generated by Altium Designer were transferred to the LPKF ProtoMat H100 PCB milling system. The milling procedure, shown in Appendix B, produced the PCB out of blank layered metal sheets.

To complete the setup, the socket was soldered onto the PCB with through-hole connectors mounted along the PCB edges. They are used to provide connection to external instruments, where the power and measurement cables can be attached. The PCB layout can be seen in Fig. 5.26. The end result is illustrated in Fig. 5.27.

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It is essential that compliance currents are calculated, based on their target chip wires, their width and foundry-provided specifications. A connection diagram is included in Appendix D that illustrates the necessary connections, their respective type, and compliance requirements.

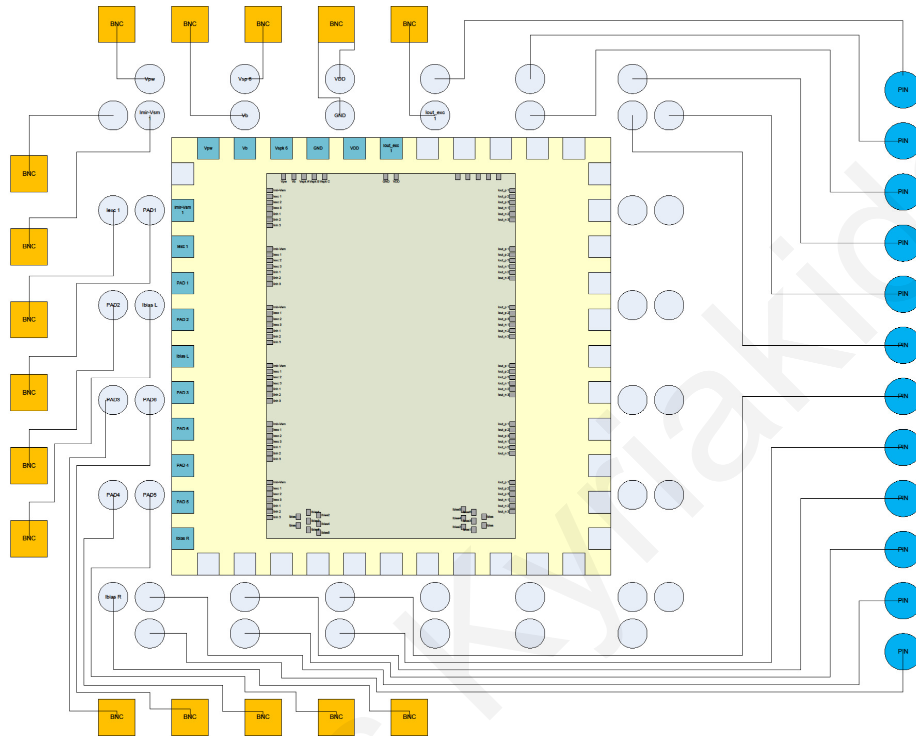

Figure 5.26: PCB layout showing connections between the socket and connectors.

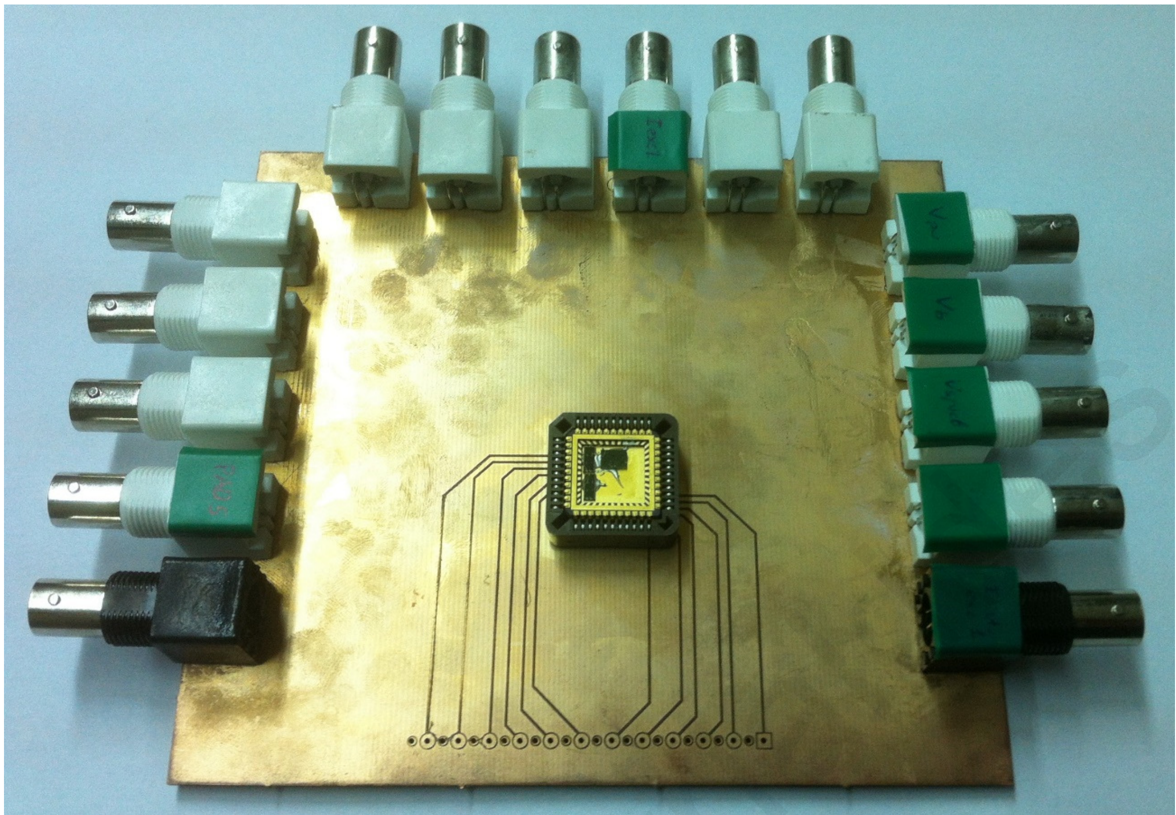

Figure 5.27: Complete test setup assembled on the PCB, illustrating the dies wire bonded to the package, the socket attached to the PCB, and the through-hole connectors.

5.3.5 Results

An evaluation of the various modules and circuits making up the network aims to verify the biomimetic network function. The characterization process described in the previous sections is therefore implemented and the results compared with designed specifications.

The current reference module presents good agreement with current outputs specified in design. After measurements were taken, a sixth-order bandstop filter was designed in Matlab® and applied to the signal to filter noise around 50 Hz. The resultant values are compared to the nominal ones in Tab. 5.6. As expected due to sizing, the two columns are not an exact match, however, a reasonable agreement is observed, with the 1 nA source showing excellent converge.

Nominal Value	Measured Value
463 pA	0.698 nA ±7 pA
1.09 nA	1.085 nA ±5 pA
2.23 nA	1.972 nA ±30 pA
5.90 nA	6.425 nA ±80 pA
10.3 nA	9.997 nA ±1 pA

Table 5.6: Characterization results of the current reference module, showing nominal and measured values.

A set of measurements attempts to compare input to output values for the current mirror module. As before, a sixth-order bandstop filter was designed in Matlab and applied to the signal to filter noise around 50 Hz. As shown in Fig. 5.28, the module functions adequately in producing mirrored currents from a reference current.

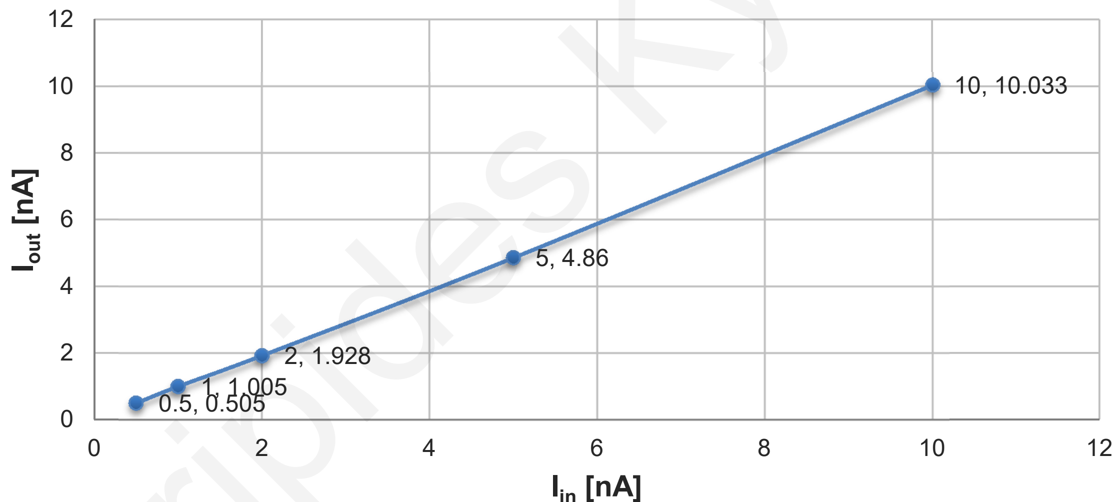

Figure 5.28: Current mirror test results. Labels represent I_{in} and I_{out} values for each data point.

With the current supply set at 1 nA, the LIF neuron's voltage output is measured. The result is the expected firing, shown in Fig. 5.29. The output gives on average 30 ms pulses with peak value 3.22 V and period of 155 ms.

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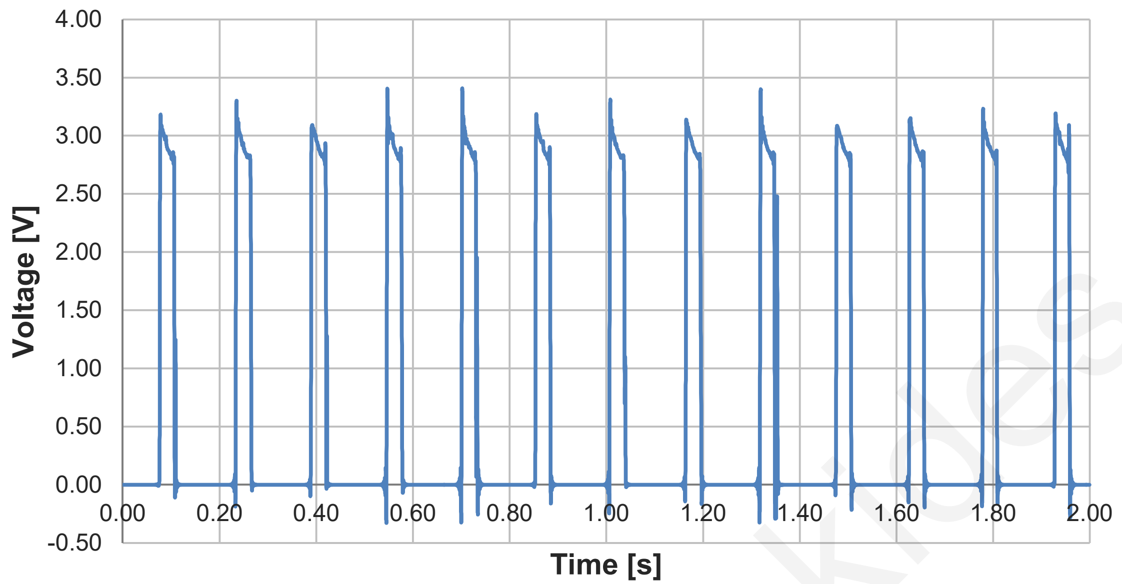

Figure 5.29: Measured LIF neuron output.

The deviation in temporal response (i.e. pulse width and period) is possibly due to parasitic capacitances, something which subsequent simulations corroborate. Fig. 5.30 illustrates the effect of capacitance at circuit junctions on the output waveform. Another possible factor is the high sensitivity of leakage and discharge currents to the bias and sizing of transistors MN1 and MN3 shown in Fig. D.2. These highly resistive pseudo-resistors are susceptible to process variations. The unavoidable discrepancy from designed specifications changes the current to ground during both firing and spiking periods, thereby affecting firing frequency and pulse width. With the spiking behavior qualitatively unaffected, this discrepancy is not expected to interfere with designed network functionality.

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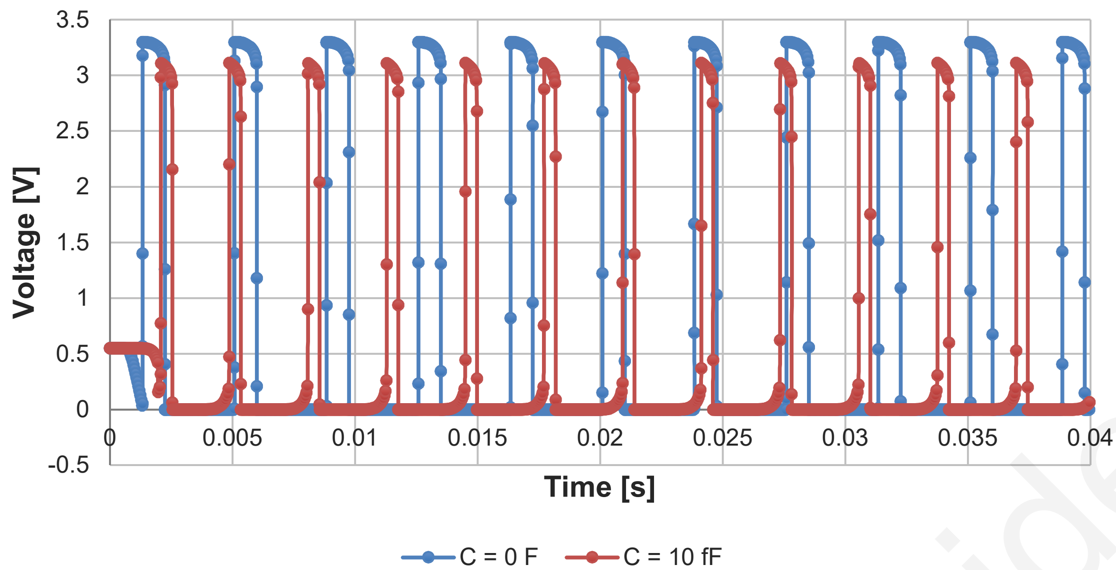

Figure 5.30: Simulated comparison output of LIF neuron with added junction capacitance.

The current limiter achieves the required compliance in current output from the LIF neuron. Connecting the current limiter module to the LIF output, the current limiter output is measured. The voltage pulses produced by the LIF neuron are then observed as current pulses. For a 4 nA limiting current the result can be seen in Fig. 5.31. The pulses are restricted below 4 nA, although some do exceed the enforced limit, reaching a maximum of 4.54 nA. Therefore, a 2 nA current limiter is preferred in the network implementation to keep memristor currents within acceptable bounds.

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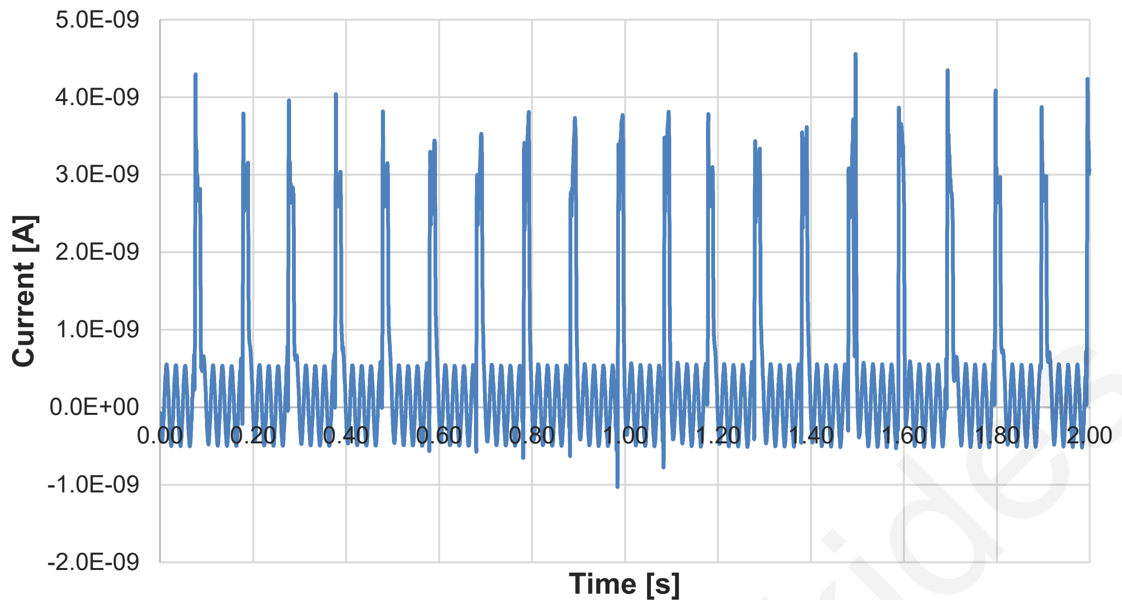

Figure 5.31: Measured LIF neuron output with current limiter module.

With the individual components confirmed to qualitatively comply with specifications in providing spiking output and current compliance, the network can be tested for biomimetic functionality. Initially, a fabricated memristor device is electroformed, as described in Chapter 4, and connected between two LIF neurons (source and target) in series. Current is supplied to the source neuron while the target neuron is observed. Fig. 5.32 shows the initial (untrained) response, consisting of narrow pulses. Their approximate width is 4 ms, height 1.35 V, and period 120 ms. Continuous activation of the source neuron causes a drop in resistance of the memristor, or potentiation of the synapse through training. The target neuron's output then settles into the final (trained) response, represented by the waveform of Fig. 5.33. This consists of wide pulses with approximate width 85 ms, height 2.7 V, and period 240 ms.

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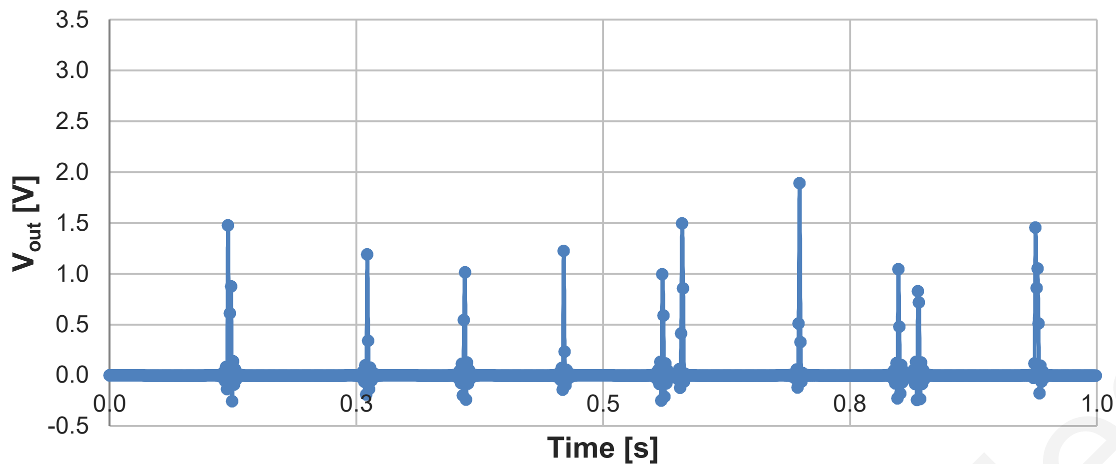

Figure 5.32: Spiking pattern measurement of LIF neuron initial output.

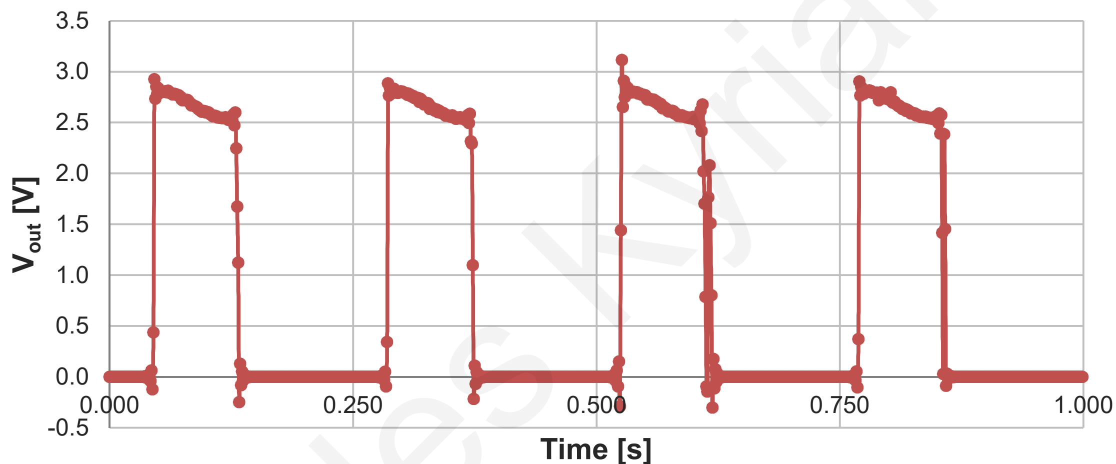

Figure 5.33: Spiking pattern measurement of LIF neuron final output.

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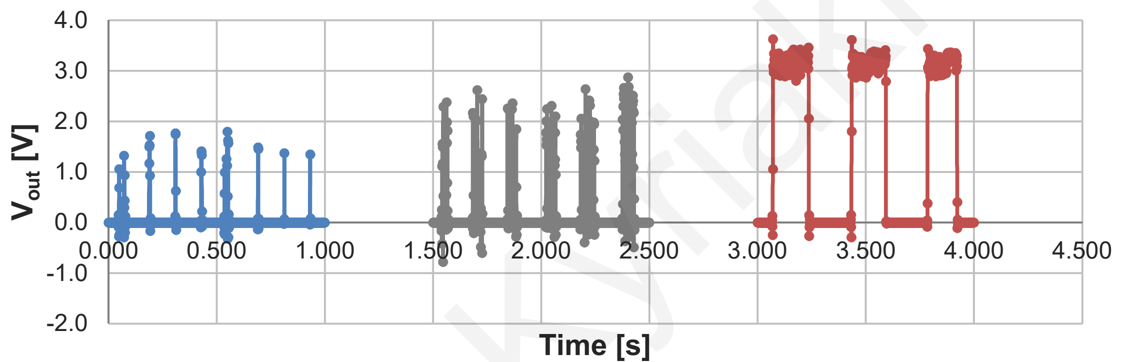
In order to complete the network shown in Fig. 5.21, two source neurons are connected to a target neuron through two memristors. The target neuron's output is recorded for each input neuron activation and shown in Fig. 5.34. The output is separated into two graphs representing each input neuron. Three periods can be defined:

Untrained period: Initial activation of either source neuron produces the untrained phase output predicted by Fig. 5.32, with approximate pulse width 4 ms, height 1.55 V, and period 125 ms. The response is that shown in the left section of Fig. 5.34.

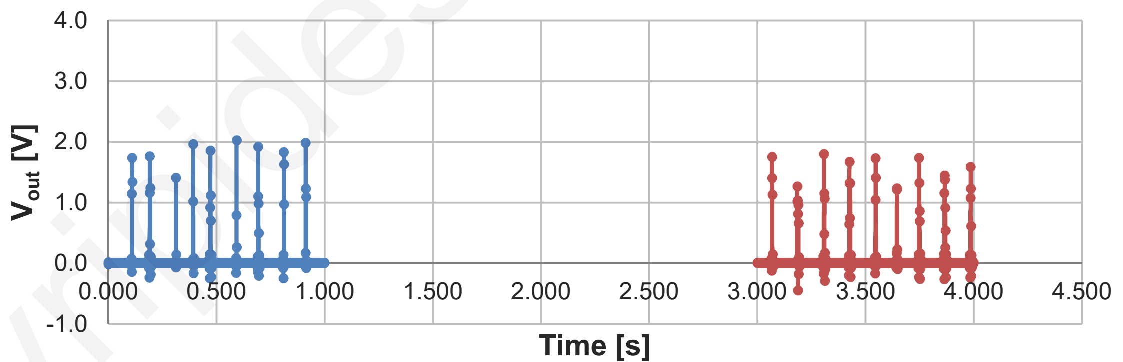
Training period: Subsequently, one of the source neurons is stimulated, whereas the other stays inactive. Continuous activation of the top source neuron shows a transitional

phase during the training of the intervening synapse, i.e. memristor potentiation. The response is that shown in the middle section of Fig. 5.34.

Trained period: With continuous activation of the top source neuron, the output settles into its final trained phase, where the observed response is that predicted by Fig. 5.33, with approximate pulse width 155 ms, height 3.2 V, and period 345 ms. The response is that shown in the right section of Fig. 5.34. In this state, activating the trained synapse will cause the system output to conform to the potentiated state, shown on the top right section of Fig. 5.34, whereas activating the untrained synapse causes the system to conform to the depressed state, shown on the bottom right section of Fig. 5.34.



(a)



(b)

Figure 5.34: Evolution of system output. Graphs (a) and (b) represent the output from each input neuron activation. Each output is separated in three sections corresponding from left to right to untrained, training, and trained periods.

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5.3.6 Discussion

The purpose of the biomimetic circuit designed is to show how a memristor can function as an electronic synapse equivalent. This entails "strengthening" the connection between two adjacent neurons when they communicate more often. In electronic terms, this can mean lowering the resistance of the connection. To test that, initially each input LIF neuron is fed with current and the output LIF neuron's output voltage is measured. The frequency of output spikes should be the same for all LIF neurons and this sets the benchmark for the "depressed" synaptic state.

The probing phase is followed by the "training" phase, where one of the two input LIF neurons is supplied with current, i.e. potentiated, whereas the rest are not. The result of the "training" is that the memristor attached to the particular LIF neuron consistently lowers its resistance due to the application of consecutive positive pulses.

In the second probing phase all input neurons are again supplied with constant current. Testing each one individually one should notice a dissimilarity between the potentiated connection and the rest; the output from the potentiated memristor should give scaled output spikes. This is due to the increased current reaching the output neuron and exhibits the result of the "learning" that took place at that "synapse".

The common output of the memristors at the target neuron input ensures a stability to the system against random spikes. Spikes arriving at the source neurons will create a high voltage state at the common point (before the target neuron) from the potentiated memristor. Therefore, the potential difference across the depressed memristor will be reduced and no potentiation will occur.

The analog circuit is asynchronous in its operation, abiding to its neuromorphic design, and thereby eliminating clock circuitry. Though implemented with two inputs, the principle is applicable to any number of inputs. It features electronic neurons emulating biological neurons in integrating incoming signals and firing when an internal threshold is crossed. Similar to biological neurons, they feature a refractory period, while leakage ensures volatility in their operation. Synapses are emulated through memristor devices. The biological function paramount to the successful emulation of many bioinspired applications, such as pattern recognition, is plasticity. This is accomplished by the potentiation of memristors through the neuron's spiking output. The overall circuit output can then be supplied to another layer of neurons, where the difference between spike

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amplitude and duration can be utilized. Alternatively, computations at the next stage can be performed based on the difference in charge per time delivered from the circuit.

The results presented above should be compared to a transistor-based implementation of a synapse. One such highly cited memristor emulator has been presented by Pershin and Di Ventra [124]. The memristor emulator consists of the following units: a digital potentiometer, an ADC, and a microcontroller. The terminals of the digital potentiometer serve as the external connections of the memristor emulator. The microcontroller executes a code according to a set of predefined equations and determines a resistance that is written into the digital potentiometer. Two significant disadvantages can be noticed compared to the aforementioned single device: (a) the memristor emulator contains active components that consume power, as opposed to the passive device that consumes none; and (b) the memristor emulator requires a very large topology, with thousands of micron-scale transistors, whereas this single device measures a few microns in width and can be scaled down to nanometers.

5.4 Conclusion

This chapter firstly demonstrates that it is possible to build an extremely compact, low-frequency, capacitorless oscillator using memristors. The oscillator takes advantage of the change in resistance of a memristor, and the associated voltage across the device to replace the space consuming capacitor of an RC oscillator. It has been shown that the advantage of this approach in comparison to traditional approaches is that it yields a very low footprint. Furthermore, any active method of reducing the footprint of the resistive component benefits this approach equally to other approaches.

Secondly, a neuromorphic circuit is presented. Memristor devices based on a Cu/Ta_2O_5 active layer have been fabricated. The devices were characterized and modeled. They were subsequently used in the design of a neuromorphic circuit exhibiting plasticity. The system consists of LIF neurons connected through memristors, emulating the architecture of neurons and synapses found in biological organisms. The results confirm the simulation data in exhibiting plasticity and thereby enabling identification of input through the output spiking characteristics.

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Chapter 6

Conclusion

6.1 Summary

Leon Chua's postulation of the existence of the memristor in 1971 was followed by a long period of idleness in the subject matter. In 2008 memristors were discovered in HP Labs, bringing that period to an end. It has since been established that memristors have existed for much longer, without being identified as such. Moreover, memristors have been classified within a broader group of devices called memristive devices. The 2008 discovery sparked substantial activity in the newly-established field. During this time, a variety of memristive devices have been proposed and fabricated by numerous research groups. Through this continuous process, the physical mechanisms leading to memristance effects are being investigated. As the characteristics of these devices are being deciphered, novel memristive applications are being proposed. These applications include both improvements of existing approaches as well as novel architectures based on new paradigms. This thesis has aimed to add to the body of knowledge in the respective fields of memristive devices and their applications.

Within the scope of this thesis, two different device types were fabricated. The devices are different in both structure and physical process involved. The first type of devices, based on NiTi, have the unique advantage of multi-time-scale volatility. This marked the first time their hysteresis in the I-V domain has been explored. A method with which they can be incorporated in CMOS processes has also been proposed. The second type of devices, based on Cu/Ta_2O_5, feature high integration with CMOS fabrication processes. In the process of this thesis, Cu/Ta_2O_5 devices have been shown to conform to the definition of memristor devices.

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The NiTi device fabrication involved encapsulation in borosilicate glass through heat treatment. The Cu/Ta_2O_5 device was fabricated in a cleanroom facility. A series of fabrication steps, involving wet oxidation, evaporation, lift-off, sputtering, and dry etching, were used to construct the device. Optical microscopy and SEM/FIB imaging were used to verify the successful creation of the structure.

Extensive characterization of the memristive devices has been performed. These characterization results were used to produce models of the fabricated NiTi and Cu/Ta_2O_5 devices.

The NiTi devices were characterized for their change in resistance with respect to temperature, while heat loss was mapped using a multi-physics platform. The characterization revealed that hysteresis curves are evident in various forms, most importantly the I-V domain. Combining simulations and ab-initio calculations rendered a Verilog-A behavioral model for NiTi devices that can be used in IC design. Simulations with the model have been shown to match the device measurements.

For Cu/Ta_2O_5 devices, the forming procedure has been delineated and the two regions of operation, namely pre- and post-forming, have been introduced for the first time. Through extensive electrical measurements the forming parameters required, as well as functionality in the pre-forming and post-forming regions, have been explored. Characterization regimes included DC, AC and pulse measurements. After recognizing that diffusion is the mechanism driving memristance, and building upon existing diffusion models, an accurate device model was proposed. The model has been derived for the post-forming behavior of the devices and coded in Verilog-A. Simulations with the model have been shown to agree with respective measurements.

Using the aforementioned models, neural circuits have been designed. Firstly, it was demonstrated that it is possible to build an extremely compact, low-frequency, capacitorless oscillator using memristors. The oscillator takes advantage of the change in resistance of a memristor, and the associated voltage across the device to replace the space consuming capacitor of an RC oscillator. It has been shown that the advantage of this approach in comparison to traditional approaches is that it yields a very low footprint.

Furthermore, a CMOS-process-compatible circuit-level application has been proposed and a prototype has been fabricated. After the Cu/Ta_2O_5 devices were characterized and modeled, they were used in the design of a neuromorphic circuit exhibiting plasticity. The system consists of LIF neurons connected through memristors, emulating the architecture

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of neurons and synapses found in biological organisms. The results confirm the simulation data in exhibiting plasticity and thereby enabling pattern recognition or input identification through the output spiking characteristics.

6.2 Contributions

With the completion of this project, novel memristive devices have been proposed, fabricated, and characterized. The class of devices presented are CMOS compliant and can be used as electronic synapses in bioinspired circuits.

Novel fabrication techniques have been proposed and implemented, such as the encapsulation of NiTi alloy in PTFE. Furthermore, the fabrication details reported for Cu/Ta_2O_5 structures add to the growing literature.

The characterization confirms some of the findings on different meristive devices, but at the same time new concepts, such as pre-forming behavior, have been introduced. Memristance mechanisms can vary between implementations, as shown with NiTi and Cu/Ta_2O_5 devices. NiTi devices rely on lattice transformation, while Cu/Ta_2O_5 devices rely on filament formation. The characterization results have been formalized in an effort to gain further understanding into these novel devices.

With regards to the first device, a novel memristive device implementation has been proposed that exploits the properties of NiTi smart alloy. This is the first time the hysteresis of NiTi devices in the I-V domain has been explored. It has been shown that a NiTi device exhibits memristive behavior, i.e. resistance drops with flux through heating, thus enabling the emulation of synaptic dynamics. The device can be scaled down for CMOS fabrication and integrated into ICs. It can be adapted under certain constraints or optimized for specific attributes through its geometry. The potential for multi-time-scale volatility is a significant advantage for future development of the NiTi device. Their mechanism of operation has been explored in depth so as to enable their physics-based modeling. Circuit designers will be afforded a customizable tool in developing circuits, bioinspired or otherwise.

With regards to the second device, Cu/Ta_2O_5 devices have been explored as memristors and proven to conform to the definition of memristor devices. Their behavior has been

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thoroughly analyzed resulting in the proposal of two regions of operation: pre-forming and post-forming. The two regions of operation for Cu/Ta_2O_5 devices allow great control over device behavior, while also deciphering complex behavior. The capability for low voltage/current operation of the Cu/Ta_2O_5 device in the pre-forming region also eliminates the overhead of an electroforming step, meaning they can be used without the extra circuitry and costs relating to forming solid electrolyte memristors. Low voltage/current operation also lends itself nicely to low-power biomimetic circuits.

Through extensive characterization, the physical mechanism of the Cu/Ta_2O_5 devices has been explored in depth. This enabled the use of diffusion models to be applied to them, resulting in a physics-based model implementation. A first principles model has been deduced and shown to match exhibited behavior. The ability to use the aforementioned model ahead of any potential application design is a significant advantage.

The circuit fabrication phase of the thesis corroborates the capability to integrate memristors into ICs. By targeting only CMOS process compatible structures for the fabricated memristors, several significant objectives are served. System complexity and manufacturing costs are reduced due to a single process. Chip footprint and power consumption are reduced by eliminating peripheral circuitry and interconnect losses. Post-fabrication processing is reduced or entirely eliminated. Resulting technologies that are potentially commercialized may benefit from a short time to market.

On the circuit level, novel memristor applications have been introduced. Biomimetic functions have been implemented to showcase the advantage memristors hold over existing approaches.

A proposed memristor-based oscillator exhibits the advantage of occupying significantly less area than equivalent circuits. This becomes important when trying to incorporate oscillators in portable or medical applications. Additionally, the oscillator is designed to produce oscillations within biological frequencies, thereby enabling its use in bioinspired neural networks. The oscillator described above also provides a toolbox with which to build a neuromorphic circuit emulating the Hodgkin-Huxley dynamics.

Within this thesis it has shown that, using memristors, cognitive tasks such as plasticity, learning, and recognition can be accomplished in compact and energy efficient architectures. Synaptic plasticity is demonstrated in a bioinspired network consisting of neurons and synapses. The neuron functionality is accomplished through the use of LIF neurons and the synaptic functionality through memristor devices. The measured results

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confirm the simulation data in exhibiting plasticity and thereby enabling identification of input through the output spiking characteristics. Furthermore, the presented prototype is asynchronous and highly scalable. Using single memristor devices boasts several advantages compared to the use of memristor emulators, since a memristor is passive, with no power consumption, simpler, and significantly smaller.

6.3 Future work

As previously noted, further investigation and exploitation of these devices' properties can be pursued. NiTi thin films can be deposited on wafers in CMOS-compatible processes. Therefore, NiTi thin films can be added to an underlying layer of CMOS components to implement neuromorphic circuits. Their prospect of multi-time-scale volatility can be explored through varying geometries.

Cu/Ta_2O_5 devices merit further investigation. With the ability for multiple runs in a fabrication facility, varying layer thicknesses can be explored. Especially considering the Ta_2O_5 layer, the effects of the layer's thickness on forming voltage, current tolerance, and voltage thresholds can be examined. Additionally, e-beam lithography can be pursued instead of photolithography. This will allow the patterning of the active region to nanometer dimensions, enabling the investigation of the filament creation and its effect on device behavior.

Operation of the memristor devices in neuromorphic circuits in higher time resolution can yield more complicated applications. Additionally, the circuits can be scaled up to emulate more intricate tasks.

Such endeavors could lead to systems with intelligent behavior or provide a platform for testing neuroscience's hypotheses concerning cognition. The true challenge for neuromorphic engineering is to understand the neurobiological mechanisms that support cognitive abilities [148]. With the available hardware in place, large-scale simulations can be used to reverse-engineer the biological brain.

Through bioinspired architecture, memristive devices may be the key element to achieving the superior performance obtained by biological systems.

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Appendix A

Cleanroom Fabrication Equipment

The range of equipment used for the fabrication process of the Cu/Ta_2O_5 devices is hereby presented. The equipment is part of the Center of MicroNanoTechnology [105] of the École Polytechnique Fédérale de Lausanne.

Heidelberg DWL200 optical pattern generator

The Heidelberg DWL200 is an optical pattern generator based on a fast laser scanner. Using the DWL200, the GDS files generated at the design stage are written onto chromium masks. It accepts chromium blank mask plates (5 × 5 " for 100 mm wafers, or 7 × 7 " for 150 mm wafers). Two exposure resolutions are offered: (a) standard exposure mode with 2.5 μm spot size, and (b) high resolution exposure mode with spot size down to 0.8 μm.

Figure A.1: Heidelberg DWL200 optical pattern generator.

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Centrotherm furnace

The wet oxidation of the silicon wafer was performed in a Centrotherm furnace. The Centrotherm furnace has a dedicated air tube for wet oxidation of silicon wafers.

Figure A.2: Centrotherm furnace.

EVG 150 automatic resist processing cluster

The spin-coating of photoresist onto the wafer was performed in the EVG 150 Automatic Resist Processing Cluster. The EVG 150 cluster has individual processing stations fed by a central robot arm. It can process standard silicon wafers or transparent substrates from 100 - 150 mm. The machine is available for positive photoresist coating, softbake, post exposure bake (PEB), hardbake, and development.

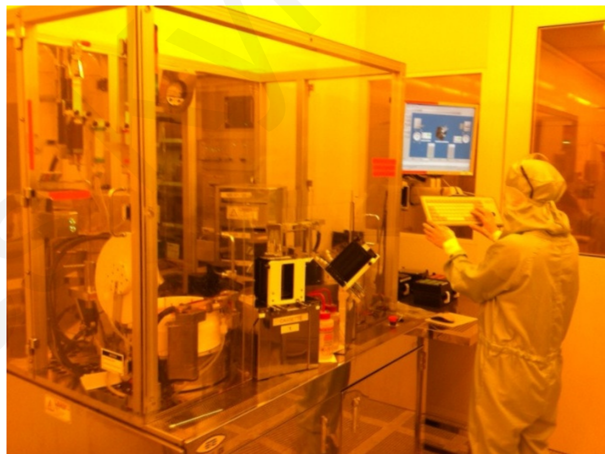

Figure A.3: EVG 150 automatic resist processing cluster.

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SUSS MicroTec MA150 mask aligner

Mask aligner MA150 is used for PR exposure. The whole wafer is exposed in a single flash for a few seconds. Both top side and backside alignment are available. The UV light is generated by a high pressure Hg light source.

The disadvantages of this exposure method are the sensitivity to photoresist thickness homogeneity and damage induced by the presence of dust particles between the mask and the wafer top surface.

Figure A.4: SUSS MicroTec MA150 mask aligner.

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Leybold Optics LAB 600 H evaporator

The LAB 600 H system can deposit metal or insulating layers on plates of 100 mm or 150 mm diameter with the evaporation technique.

LAB 600 H is specially designed for the lift-off process, requiring flux incident close to the normal of the deposition surface of the substrate, for deposits of dense dielectric films requiring the assistance of an ion source.

The low level of vacuum required in the equipment is reached through a cryogenic pump. The LAB 600 H can achieve 1.0×10^{-7} mbar after eight hours of pumping.

The thickness during deposition is measured by the frequency deviation of a quartz oscillator. The equipment also allows cleaning of the plates by ion bombardment before the deposition.

Figure A.5: Leybold Optics LAB 600 H evaporator.

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EVA 600 evaporation system

The EVA 600 equipment is used to deposit metal or insulating layers on plates of 100 mm or 150 mm diameter with the evaporation technique.

The metal deposition layer is obtained by evaporation of a metal in a crucible placed at high temperature. The level of vacuum achieved in the equipment is 5×10^{-7} mbar. The thickness is measured during deposition by the frequency deviation of a quartz oscillator. To improve the uniformity of deposition thickness, the substrate holder is made up of three holders in planetary and self-rotation.

Figure A.6: EVA 600 evaporation system.

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Pfeiffer SPIDER 600 sputtering system

The SPIDER 600 system is used to deposit metal or insulating layers on plates of 100 mm or 150 mm diameter with the sputtering technique. Sputtering is the term describing the mechanism by which atoms are stripped from the surface of a material by a collision with high energy particles.

The choice of material deposition is done simply by the replacement of a rectangular plate, called target, said material being a pure metal (e.g. aluminum, titanium, platinum, etc.), an alloy (e.g. Al + 1% Si, etc.) or a dielectric material (e.g. SiO_2, Si, etc.).

The equipment consists of four independent chambers and a load lock chamber, connected to a central chamber with a robot for transferring plates. It allows the placement of up to three metallic and one dielectric material without changing targets. Reactive sputtering is achieved with a metal target in the presence of oxygen or nitrogen.

The substrate holder can be heated. The maximum temperature is 500 °C at the surface of the plates. Pre-cleaning of the surface of the plates is done just prior to the deposition, whereas the first deposition is used for cleaning the target.

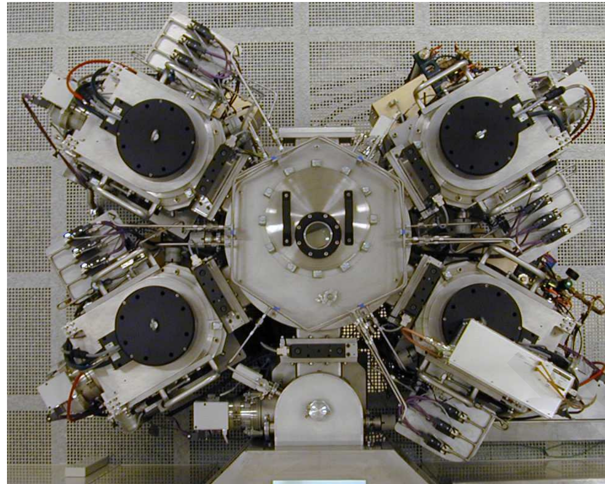

Figure A.7: Pfeiffer SPIDER 600 sputtering system.

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Plade Solvent wet bench

The Plade Solvent wet bench is where processing is carried out for 100 mm wafers. The wafers are placed in cassettes and special chemistry solvents are used for each process. Typical processes include the lift-off dissolution step with ultrasonic activation. The solvent is Remover 1165, a NMP-based mixture at room temperature. The wafers are rinsed with DI water as the final step, followed by a spin-rinse-dry cycle to remove contamination and residual particles of metal remaining from the lift-off processing.

Figure A.8: Plade Solvent wet bench.

Alcatel AMS 200 etcher

The Alcatel AMS 200 etcher is an optimized DRIE system for Silicon and Silicon on Insulator (SOI) wafers. Special hardware arrangements make it possible to use one of these three families of processes: (a) Silicon etching with pulsed process (Bosch process) and pulsed Low Frequency (LF) wafer biasing, (b) Silicon etching with no pulsed process (continuous process), and (c) Dielectric etch with Radio Frequency (RF) wafer biasing.

Figure A.9: Alcatel AMS 200 etcher.

FEI Nova 600 Nanolab dual beam SEM/FIB

The Nova 600 NanoLab is a Dual Beam SEM/FIB for nanoscale prototyping, machining, characterization, and analysis of structures below 100 nm. It combines ultra-high resolution field emission Scanning Electron Microscopy (SEM) and precise Focused Ion Beam (FIB) etch and deposition. The Nova 600 NanoLab uses a differential pumping vacuum system on the electron column, ensuring tip operation at the ultra-high vacuum levels (10^{-10} mbar), even with a controlled gas flow in the specimen chamber. The electron and ion column are mounted at 52° to each other.

Once the two columns are adjusted, the process starts with a Pt deposition of 0.5 - 1.0 μm to protect the area. This is followed by a tapered etching procedure with the FIB, as shown in Fig. A.11. Once the etching and cleaning of the area is complete, the cross-section of interest is revealed and the SEM can be guided in for imaging.

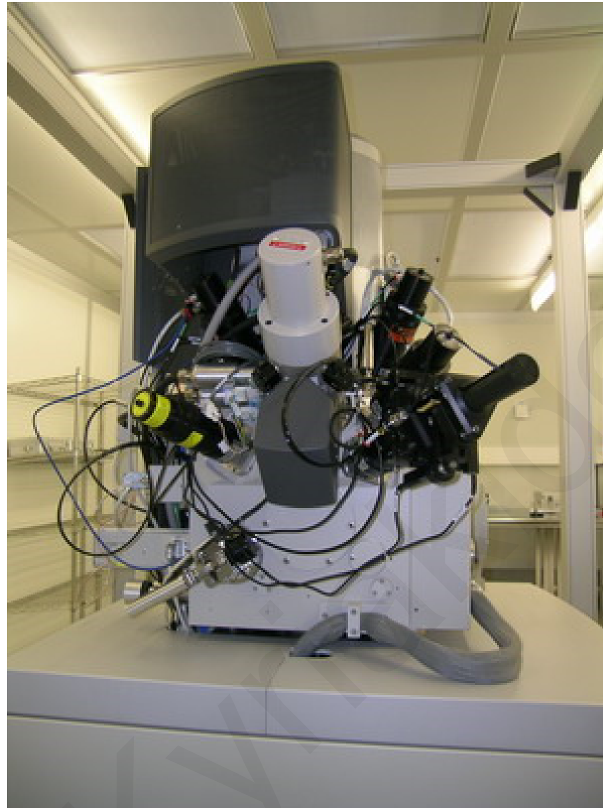

Figure A.10: FEI Nova 600 Nanolab Dual Beam SEM/FIB.

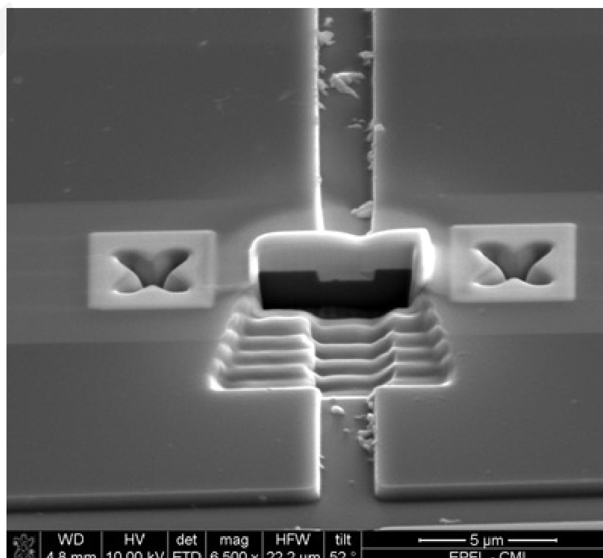

Figure A.11: Typical FIB etching by Nova 600.

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Appendix B

Electrical Characterization Equipment

This appendix lists the electrical characterization equipment described in this thesis.

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Figure B.1: The ESPEC SU-261 temperature chamber, shown with a sample loaded for testing, used for controlled heating of the NiTi devices.

Figure B.2: Keithley 4200-SCS Parameter Analyzer for low-level measurements.

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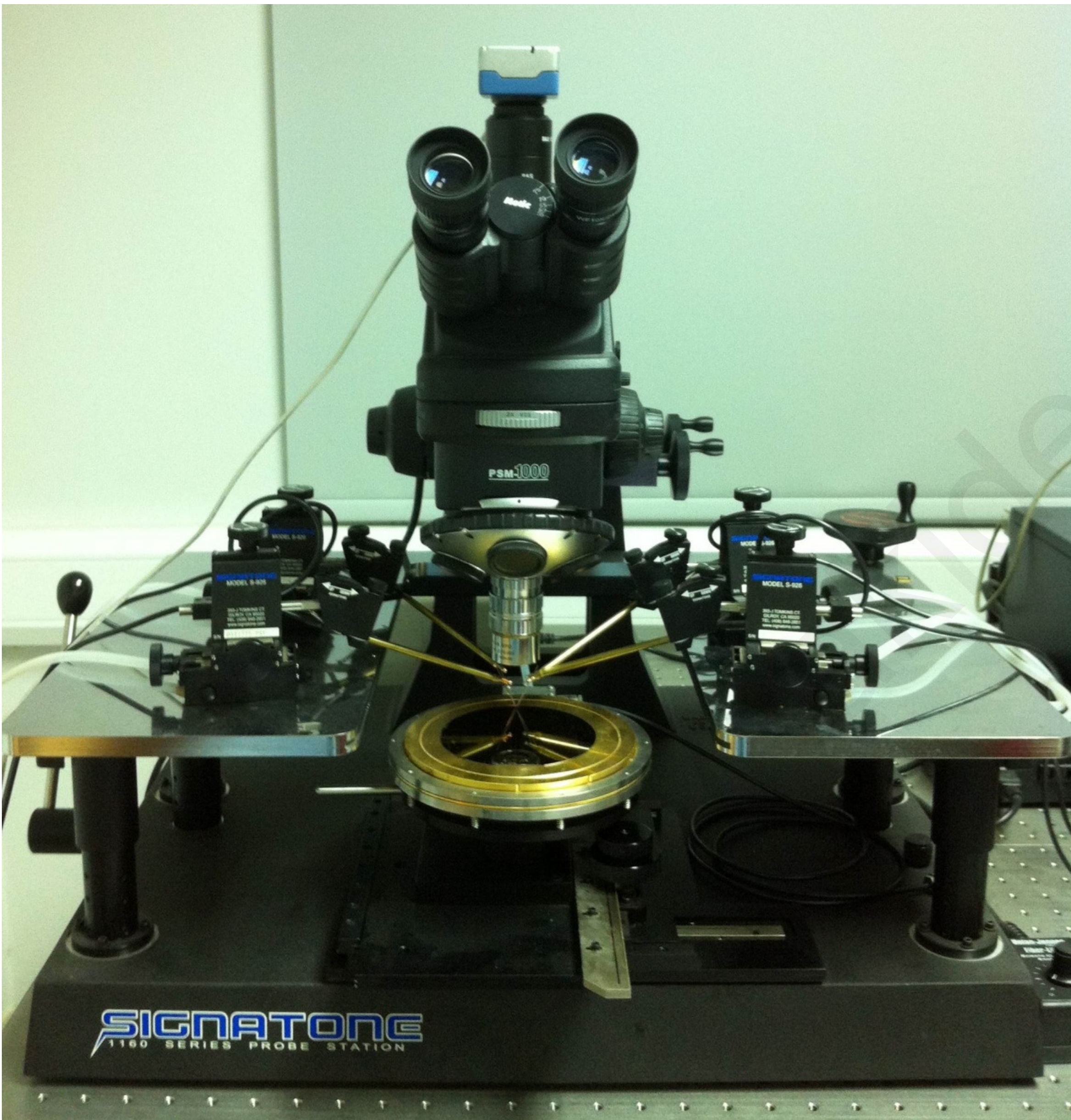

Figure B.3: Signatone 1160 Probe Station. Used for characterization of Cu/Ta_2O_5 devices.

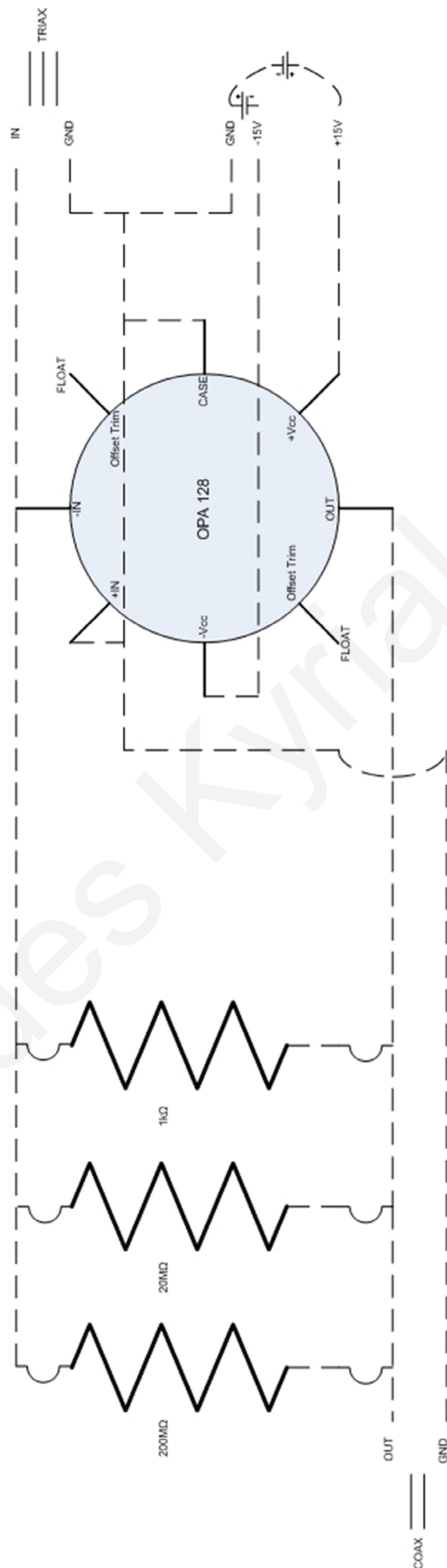

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Figure B.4: Board layout of custom-made measurement module.

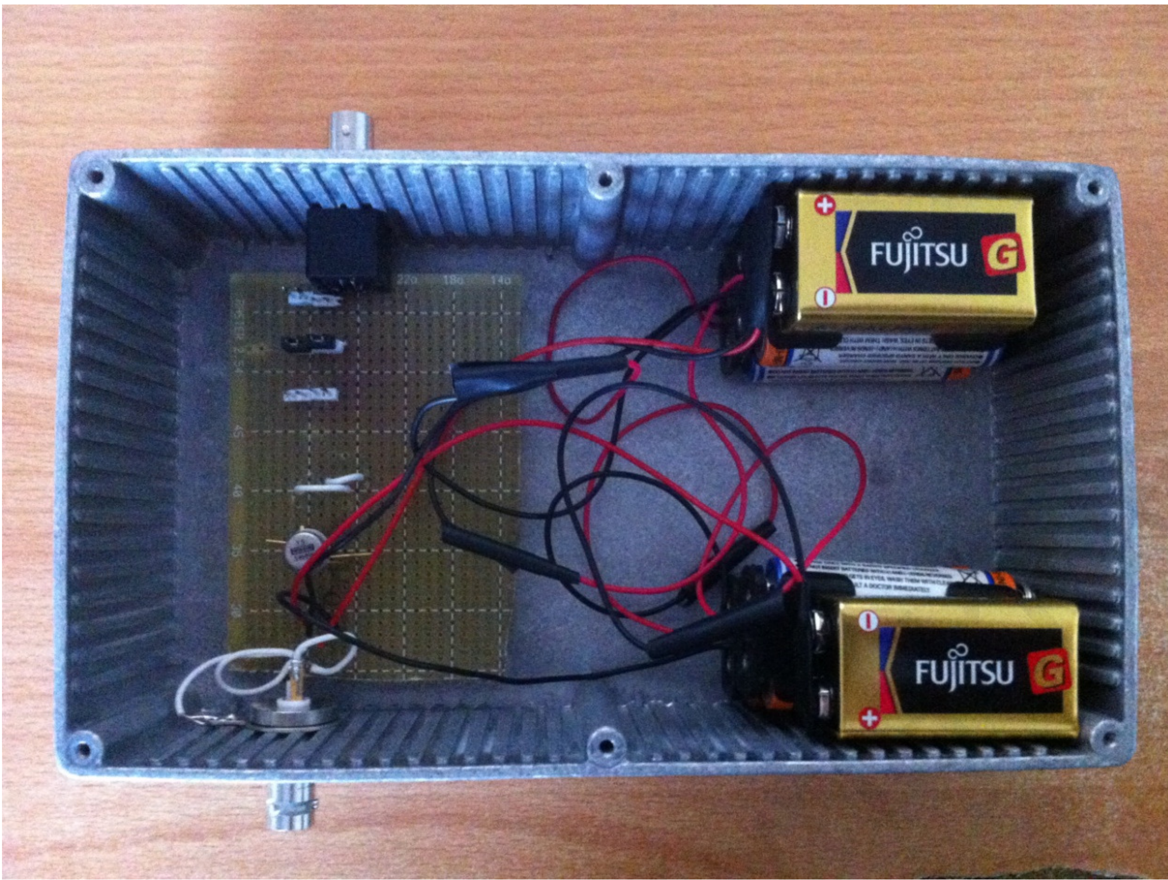

Figure B.5: Casing of custom-made measurement module.

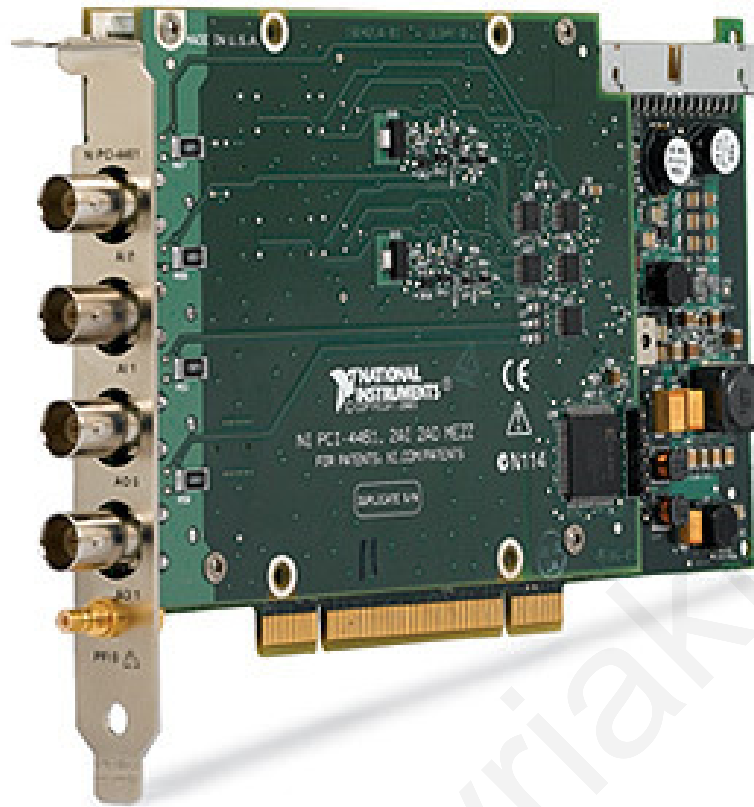

Figure B.6: The NI PCI-4462 acquisition board used for voltage measurements.

Figure B.7: The Keithley 236 SMU used for testing the neuromorphic chip.

Figure B.8: The F & K Delvotec 53XX wirebonder used to connect the fabricated chips to a package.

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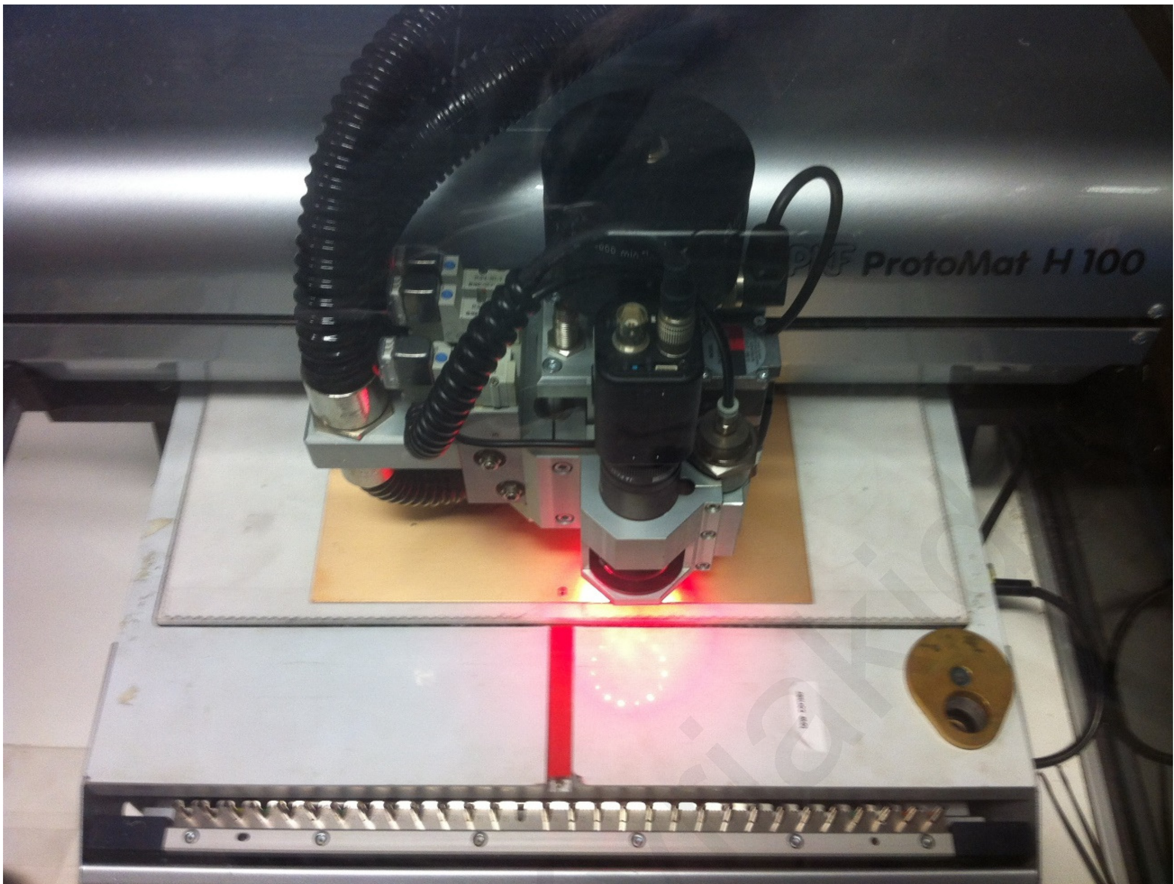

Figure B.9: The LPKF ProtoMat H100 PCB system during the PCB milling process.

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Appendix C

Verilog-A Scripts

This appendix contains the Verilog-A scripts for the NiTi and Cu/Ta_2O_5 device models presented in Chapters 3 - 4.

NiTi Device

```
// VerilogA for Memristors, NiTi, veriloga

`include "constants.vams"
`include "disciplines.vams"

module NiTi (A, B);

        inout A, B;
        electrical A, B;
        branch (A, B) res;              //contact port

// Constants
parameter real Pi=3.14159265358979323846;

// Parameters
parameter real period=0.001;            //period
parameter real L_i=0.036;               //length initial
parameter real d_i=25e-6;               //diameter initial
parameter real T_i=$temperature;        //temperature initial
parameter real T_th=343.15;             //temperature threshold
```


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```
parameter real p_v=6400;            //density
parameter real c=550;               //specific heat capacity
parameter real p_i=6.6e-7;          //resistivity initial

// Variables
real y;                             //temperature position
real t_i;                           //time initial
real t_c;                           //time current
real t_p;                           //time position
real V_i;                           //voltage initial
real V_f;                           //voltage final
real a_L;                           //linear expansion coefficient
real A_i;                           //area initial
real m;                             //mass
real R_i;                           //resistance initial
real I_i;                           //current initial
real I_f;                           //current final
real d_q;                           //heat created
real d_T;                           //temperature change
real d_L;                           //change in length
real d_d;                           //change in diameter
real d_A;                           //change in area
real d_R;                           //change in resistance
real L_f;                           //length final
real A_f;                           //area final
real R_f;                           //resistance final
real T_f;                           //temperature final
real p_f;                           //resistivity final
real d_p_d_T;                       //resistivity gradient

//Analog
analog begin

@(initial_step) begin
        A_i = Pi*((d_i/2)*(d_i/2));             //area initial
```


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```
        m = L_i*A_i*p_v;                  //mass
        T_f = T_i;                        //temperature final
end

@(timer(0, period)) begin

        t_c=$abstime;
        if (T_f > T_th) begin             //linear expansion coefficient
                a_L = 11e-6;              //austenite
        end
        else begin
                a_L = 6.6e-6;             //martensite
        end

        V_i=V(A);                         //voltage initial
        V_f=V(A);                         //voltage initial
        R_i=p_i*L_i/A_i;                  //resistance initial
        I_i=V_i/R_i;                      //current initial
        d_q=I_i*I_i*R_i*(period);         //heat created
        d_T=d_q/(c*m);                    //temperature change
        d_L=L_i*a_L*d_T;                  //change in length
        L_f=L_i-d_L;                      //length final
        d_d=d_i*0.33*d_L/L_i;             //change in diameter
        d_A=(Pi/4)*((d_i+d_d)*(d_i+d_d)-d_i*d_i);   //change in area
        A_f=A_i+d_A;                      //area final

        y=T_f;                            //temperature position initial
        t_p=pow((98.00*sqrt(7.070e+33*y*y-
4.264e+36*y+6.430e38)/(2.815e11*pow(5.848e05,(3/2)))-((4.890e26*y-
1.475e29)/7.470e27)),(1/3))-4.850e16/(3.383e17*pow((98.00*sqrt(7.070e33*y*y-
4.264e36*y+6.430e38)/(2.815e11*pow(5.848e5,(3/2)))-(4.890e26*y-
1.475e29)/7.470e27),(1/3)))+ 6.248e7/2.972e7;       //time position initial
        t_p=t_p+period;                   //time position final
        y=379.5-104.6*t_p+48.17*t_p*t_p-7.639*t_p*t_p*t_p;//temperature position final

        T_f=y+d_T;                        //temperature final
```


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```
        if (T_f > T_th)  begin                  //resistivity gradient
                d_p_d_T = -5e-10;               //austenite
        end
        else begin
                d_p_d_T = -2.3e-9;              //martensite
        end

        p_f=7.75e-7-(d_p_d_T*(T_th-T_f));  //resistivity final
        R_f=p_f*L_f/A_f;                   //resistance final
        I_f=V_f/R_f;                       //current final
end

        I(A, B) <+ I_f;                    //contact output
end

endmodule
```

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Cu/Ta_2O_5 Device

```
// VerilogA for Memristors, Ta2O5, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Ta2O5 (A, B);

        inout A, B;
        electrical A, B;
        branch (A, B) res;              //contact port

        parameter real Pi=3.14159265358979323846;
        parameter real a1=0.00008;              //a1 current amplitude
        parameter real a2=0.000015;             //a2 current amplitude
        parameter real b1=4;                    //b1 threshold strength
        parameter real b2=4.5;                  //b2 threshold strength
        parameter real c1=0.00002;              //Ap exponential magnitude
        parameter real c2=0.00002;              //An exponential magnitude
        parameter real d1=1;                    //d1 state variable amplitude
        parameter real d2=1;                    //d2 state variable amplitude
        parameter real Vp=1.55;                 //Vp threshold voltage
        parameter real Vn=0.9;                  //Vn threshold voltage

        real V_current;
        real I_current;
        real x_dot;
        real x;

analog begin

        V_current = V(A, B);
```

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```
        if (V_current > Vp) begin
            x_dot = c1 * (limexp(V_current/d1-Vp));
        end
        else if (V_current < -Vn) begin
            x_dot = -c2 * (limexp(-V_current/d2-Vn));
        end
        else begin
            x_dot = 0;
        end

        x = idt(x_dot, 0, 0, 1e-7);

        if (V_current >= 0) begin
            I_current = a1 * x * (limexp(b1*V_current) - limexp(-b1*V_current)) / 2;
        end
        else begin
            I_current = a2 * x * (limexp(b2*V_current) - limexp(-b2*V_current)) / 2;
    end

        I(A, B) <+ I_current;          //contact output
    end

    endmodule
```

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Appendix D

Chip Fabrication and Testing

This appendix lists schematics and layouts describing the chip fabrication. Diagrams are then used to illustrate each testing procedure. In the listed diagrams, used pads are shown as green, whereas unused ones are shown as grey. The testing procedure, instruments, and connectors are summarized within the diagram.

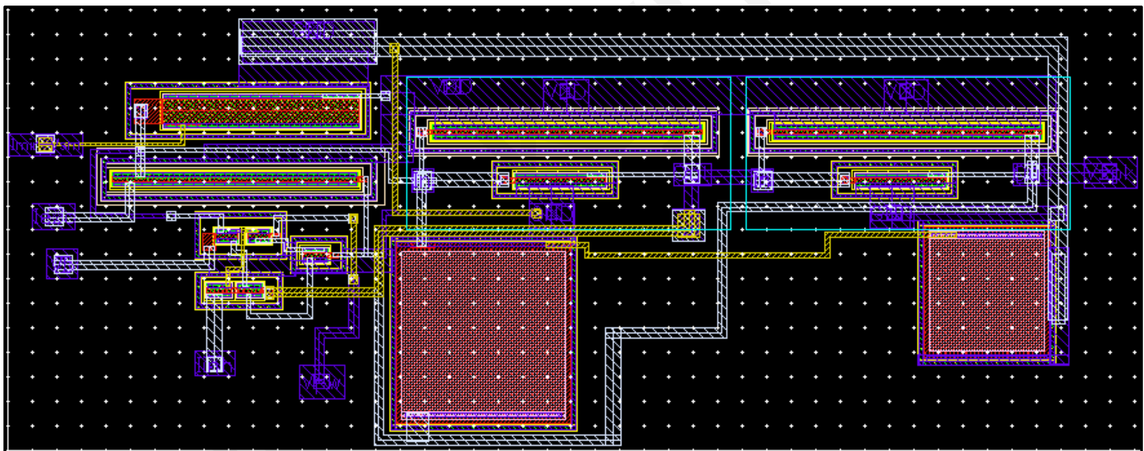

Figure D.1: Cadence Virtuoso layout of the fabricated LIF neuron circuit.

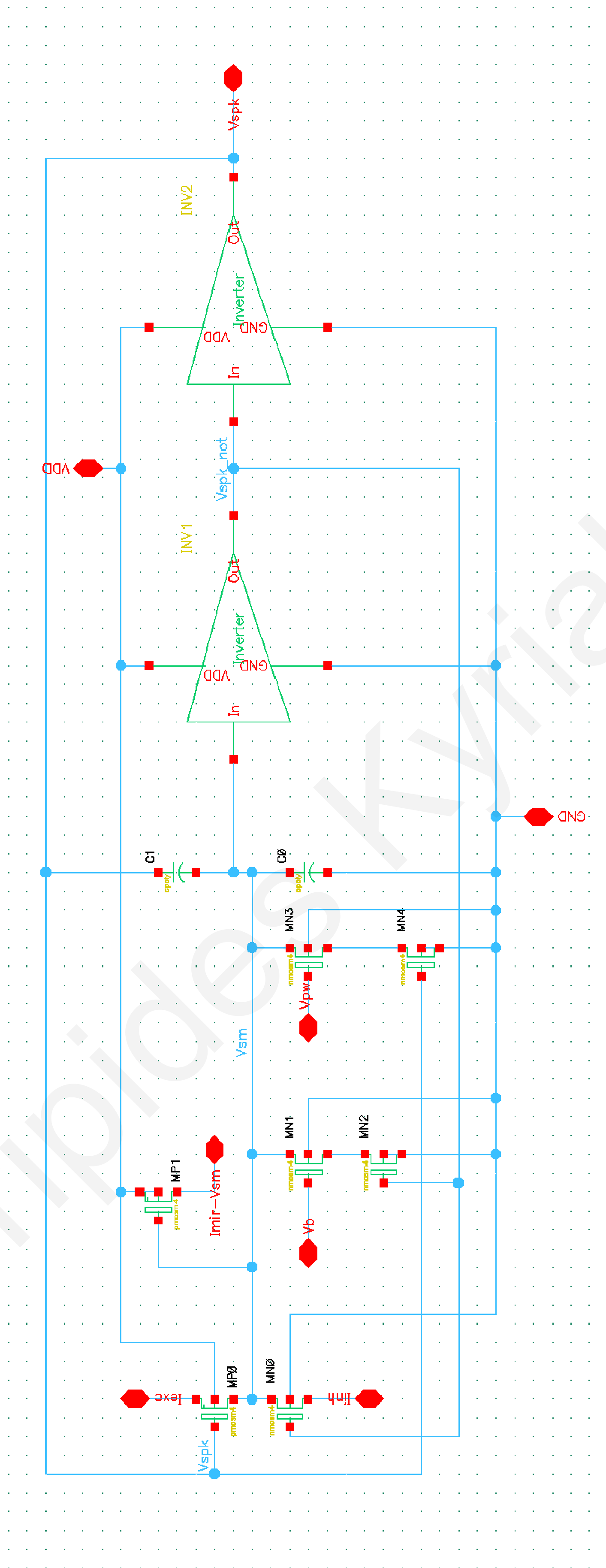

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Figure D.2: Cadence Virtuoso schematic of the fabricated LIF neuron circuit.

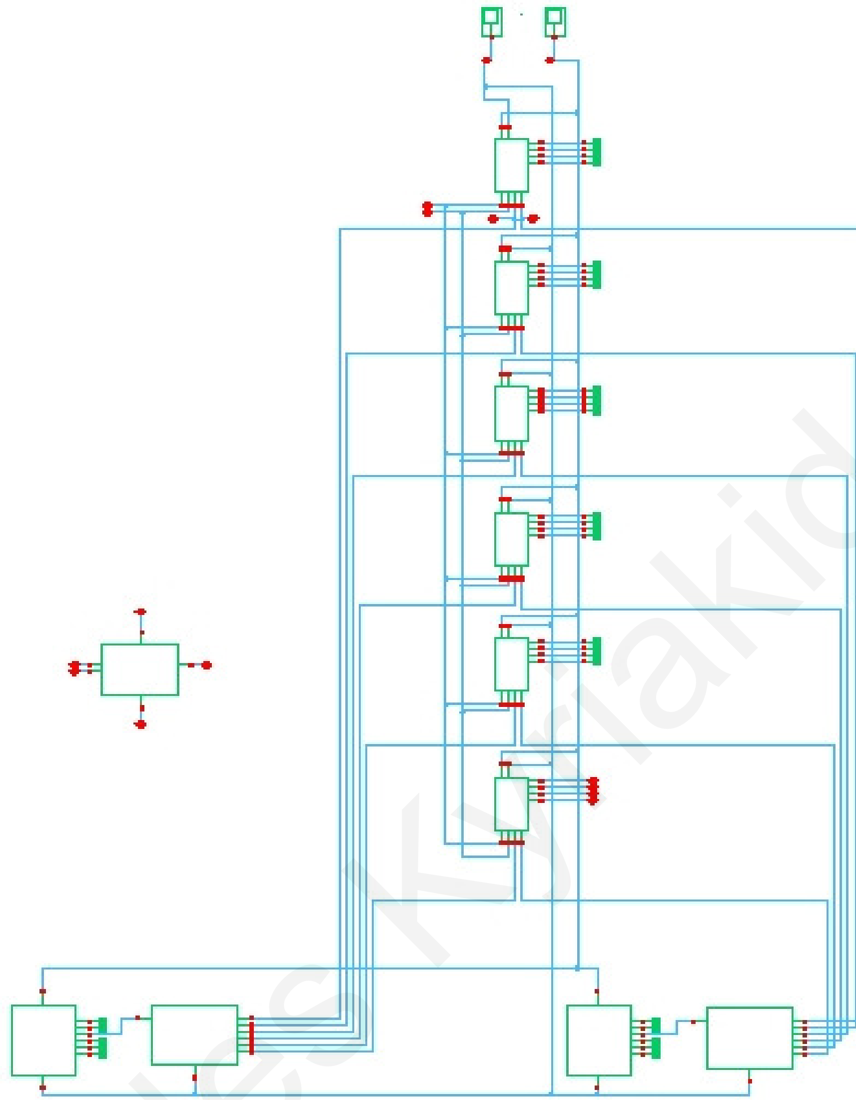

Figure D.3: Cadence Virtuoso schematic of top cell of complete neural circuit. All other cells are referenced from within this cell.

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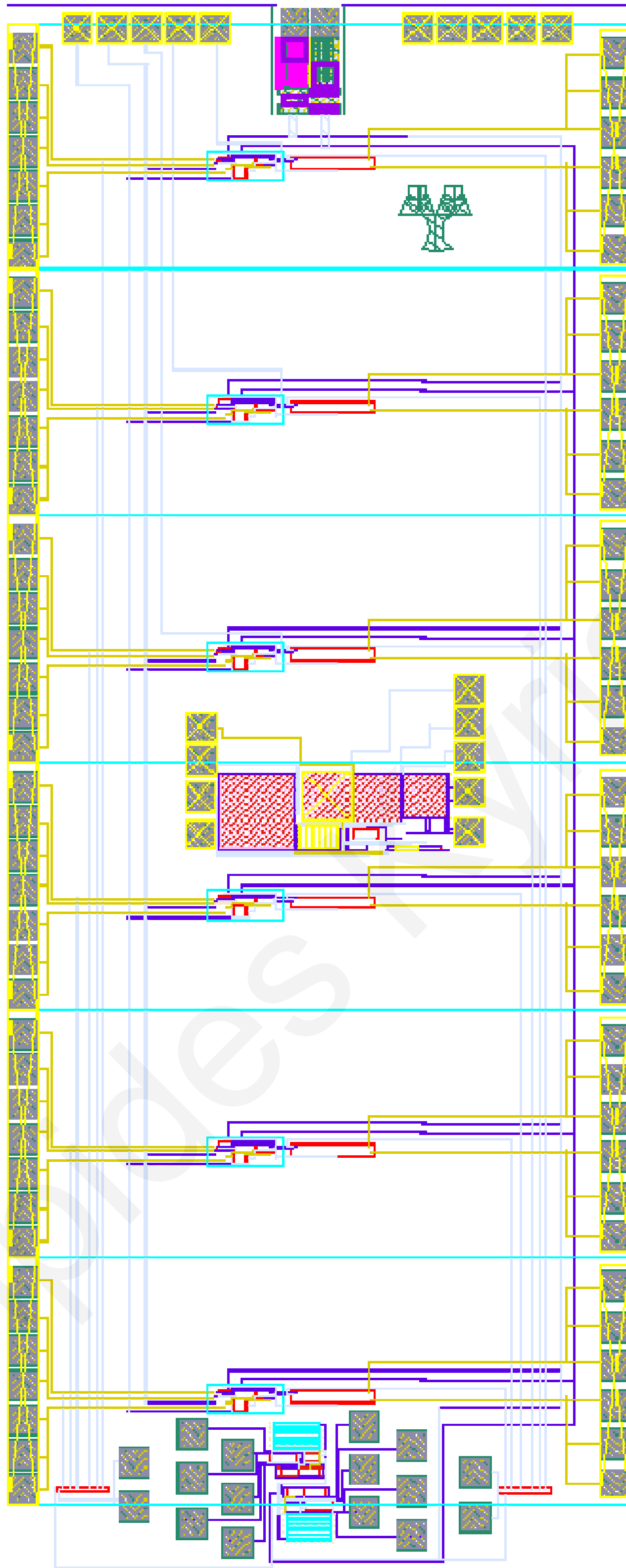

Figure D.4: Cadence Virtuoso layout of complete chip. Six LIF neurons are available on each chip. The components are connected to external instrumentation through the contact pads, shown as grey squares on the margins.

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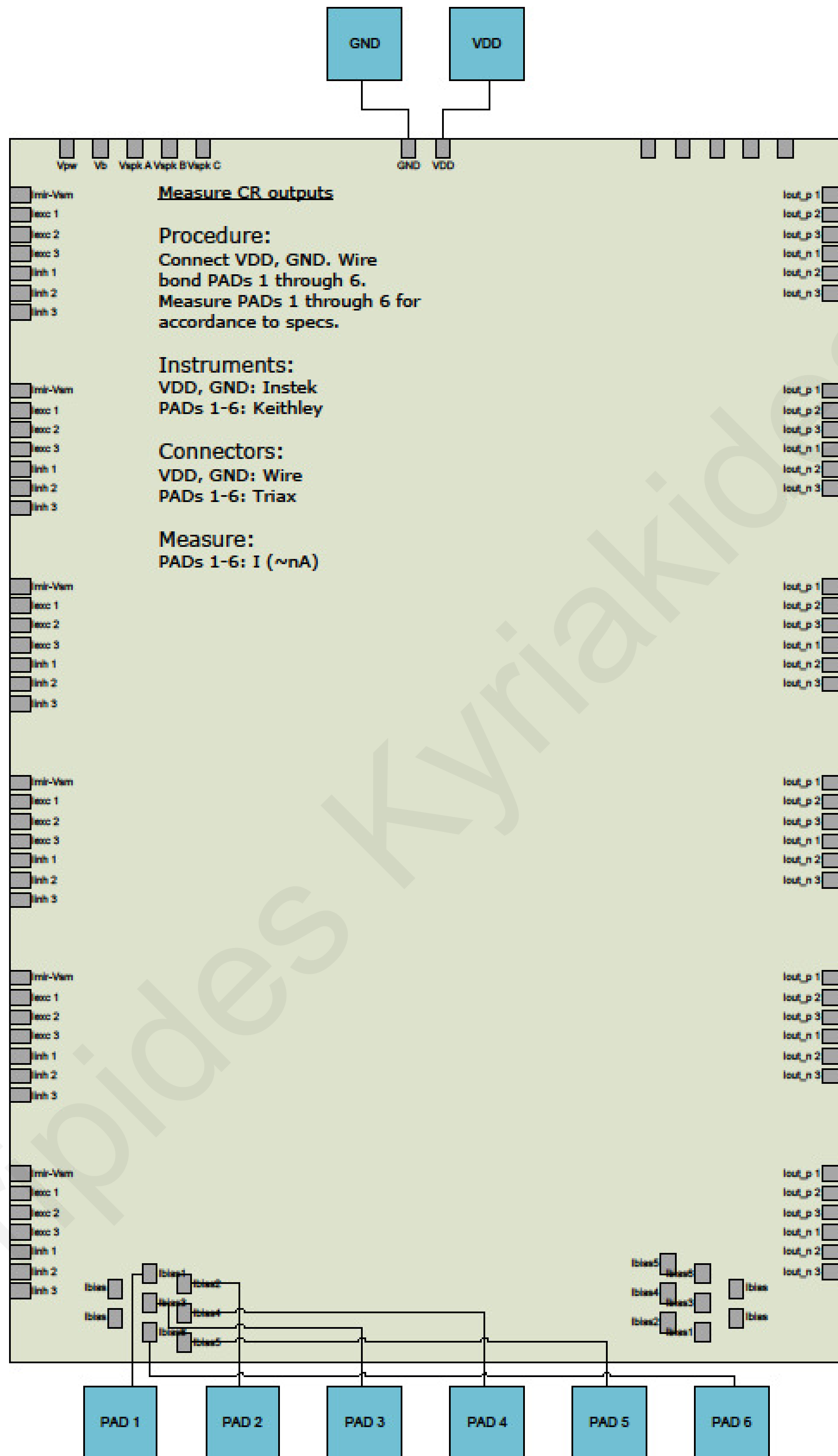

Figure D.5: Current reference module test diagram and description.

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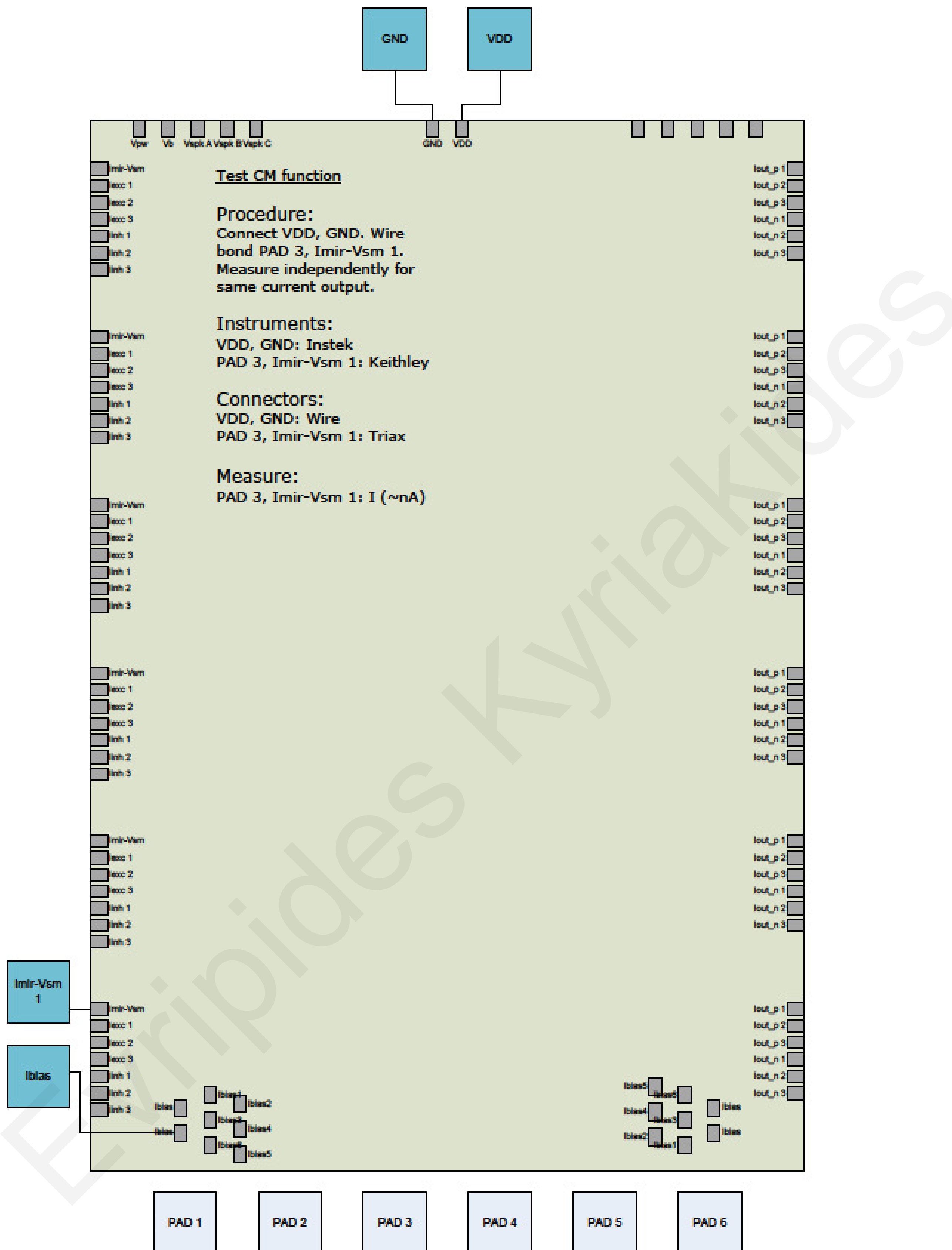

Figure D.6: Current mirror module test diagram and description.

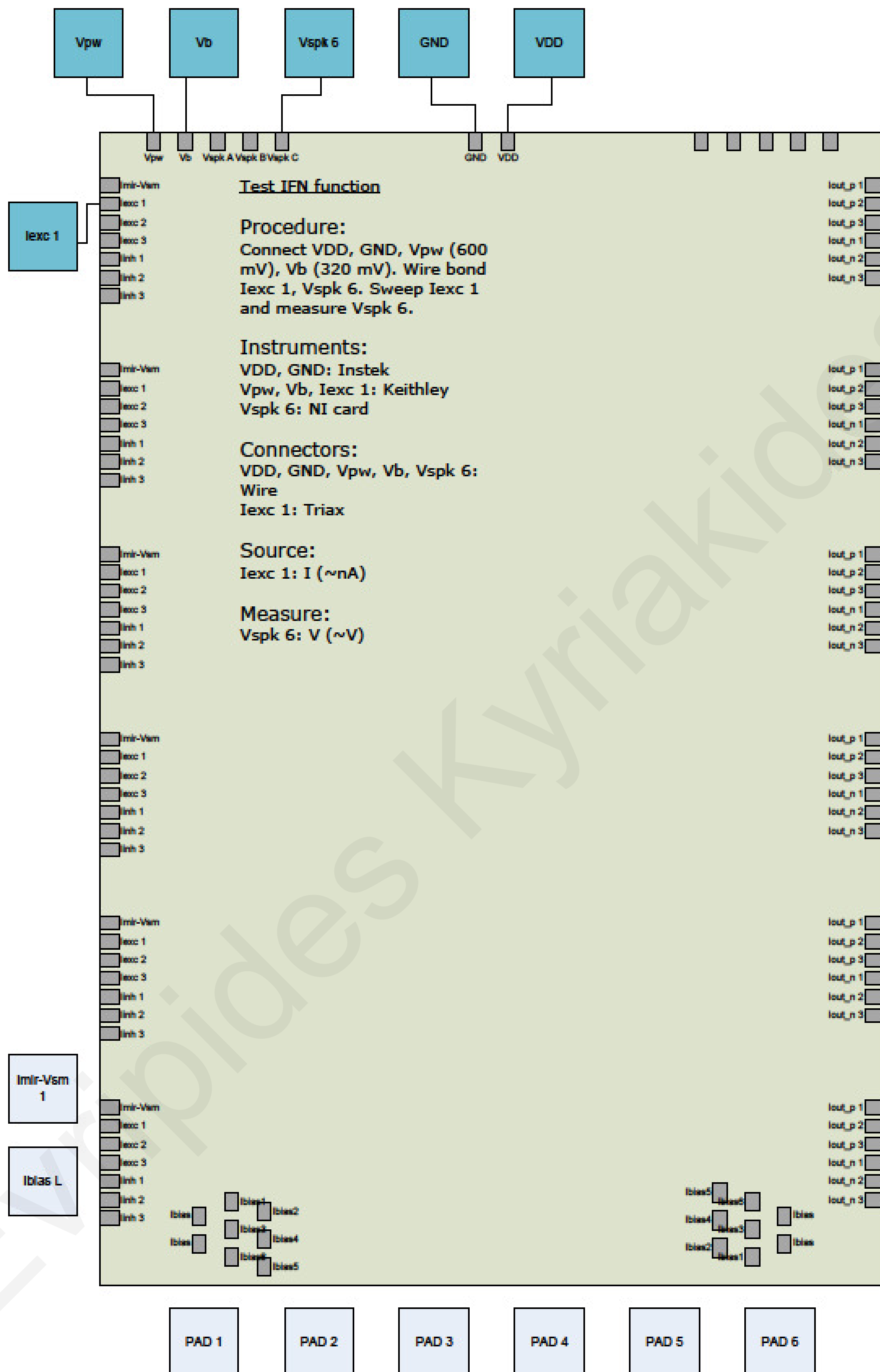

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Figure D.7: LIF neuron test diagram and description.

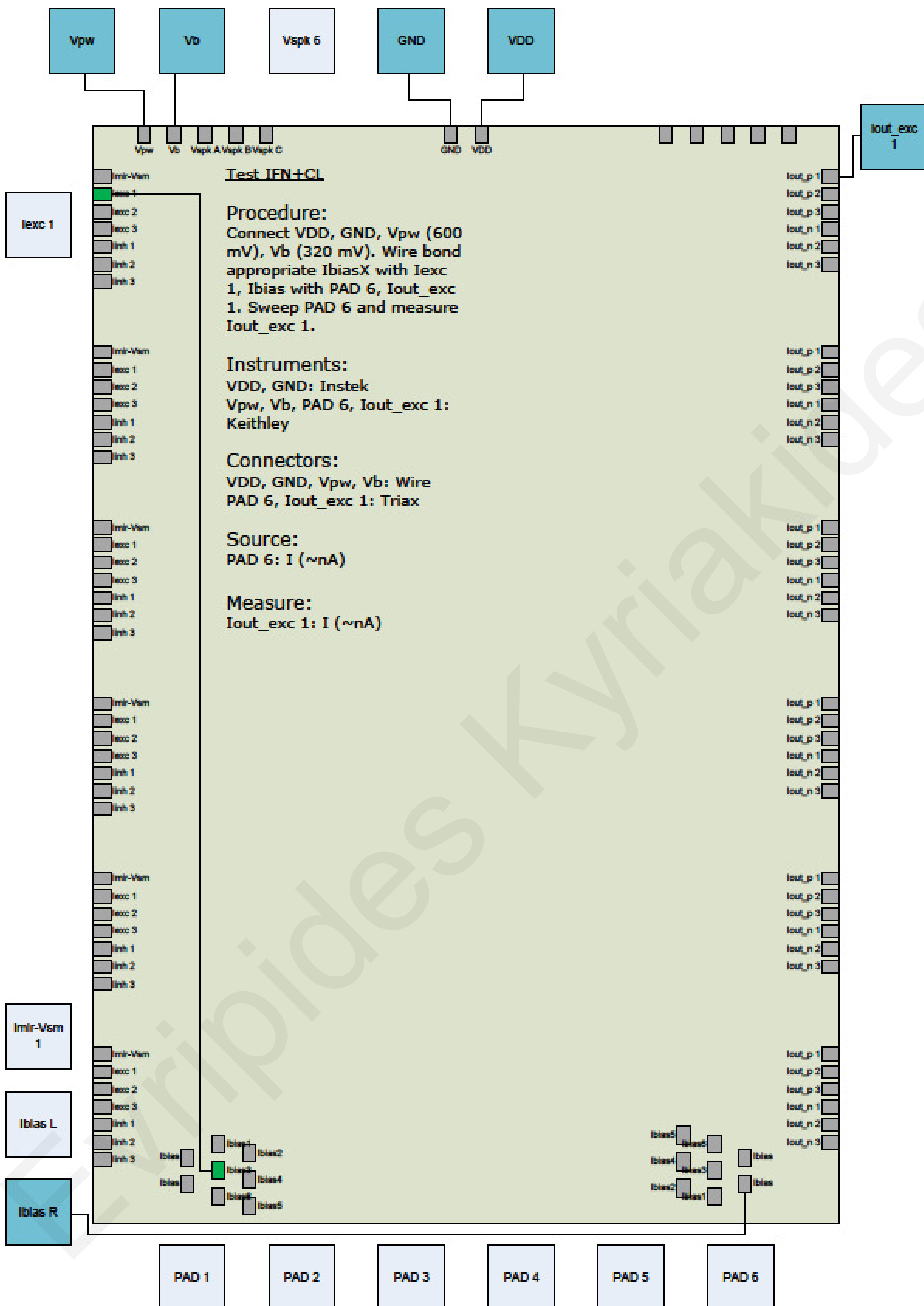

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Figure D.8: LIF neuron with current limiter module test diagram and description.

Figure D.9: Bonding diagram for ams chip and package.

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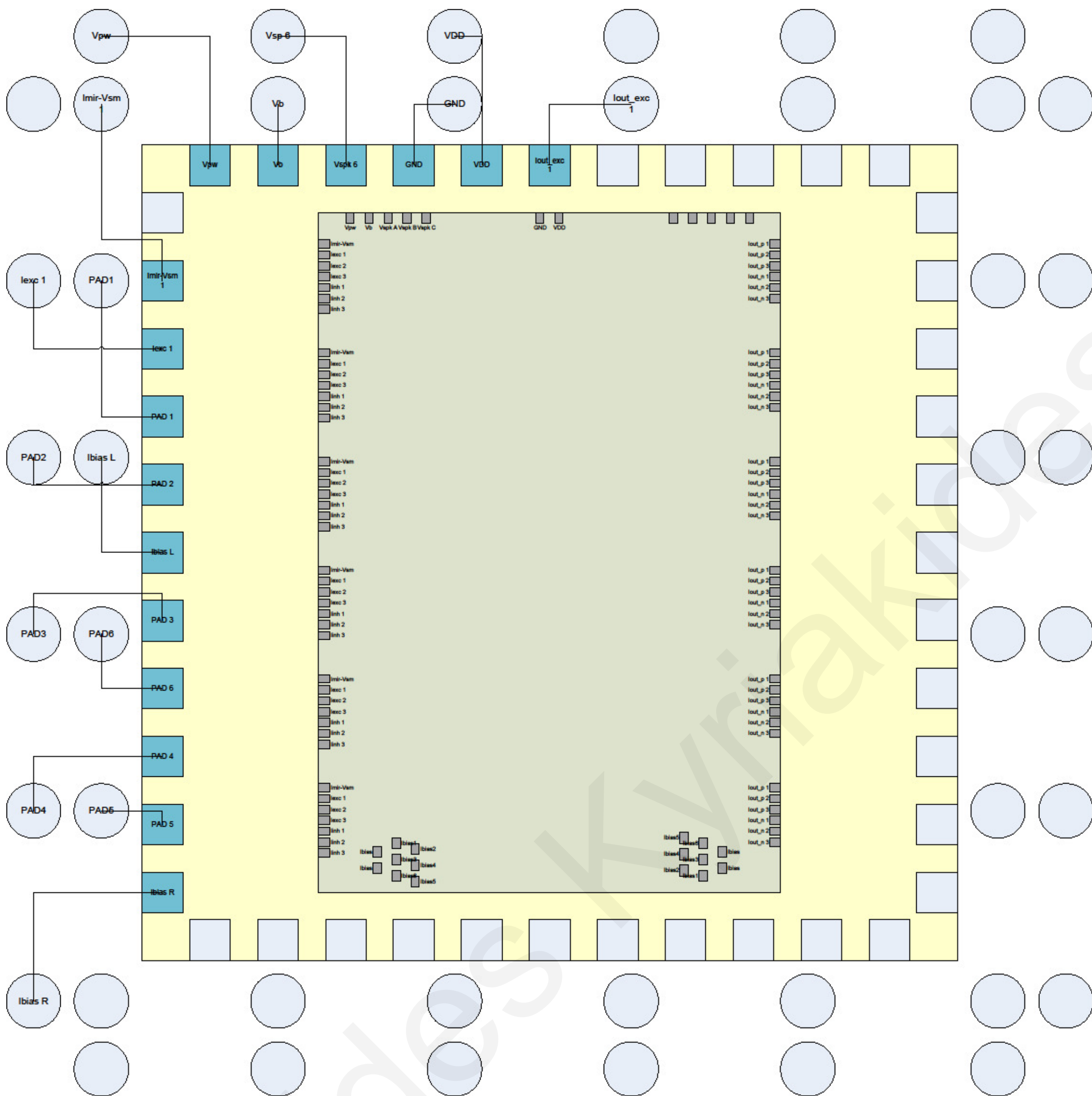

Figure D.10: The socket's connection diagram showing connections between internal pads and external pins.

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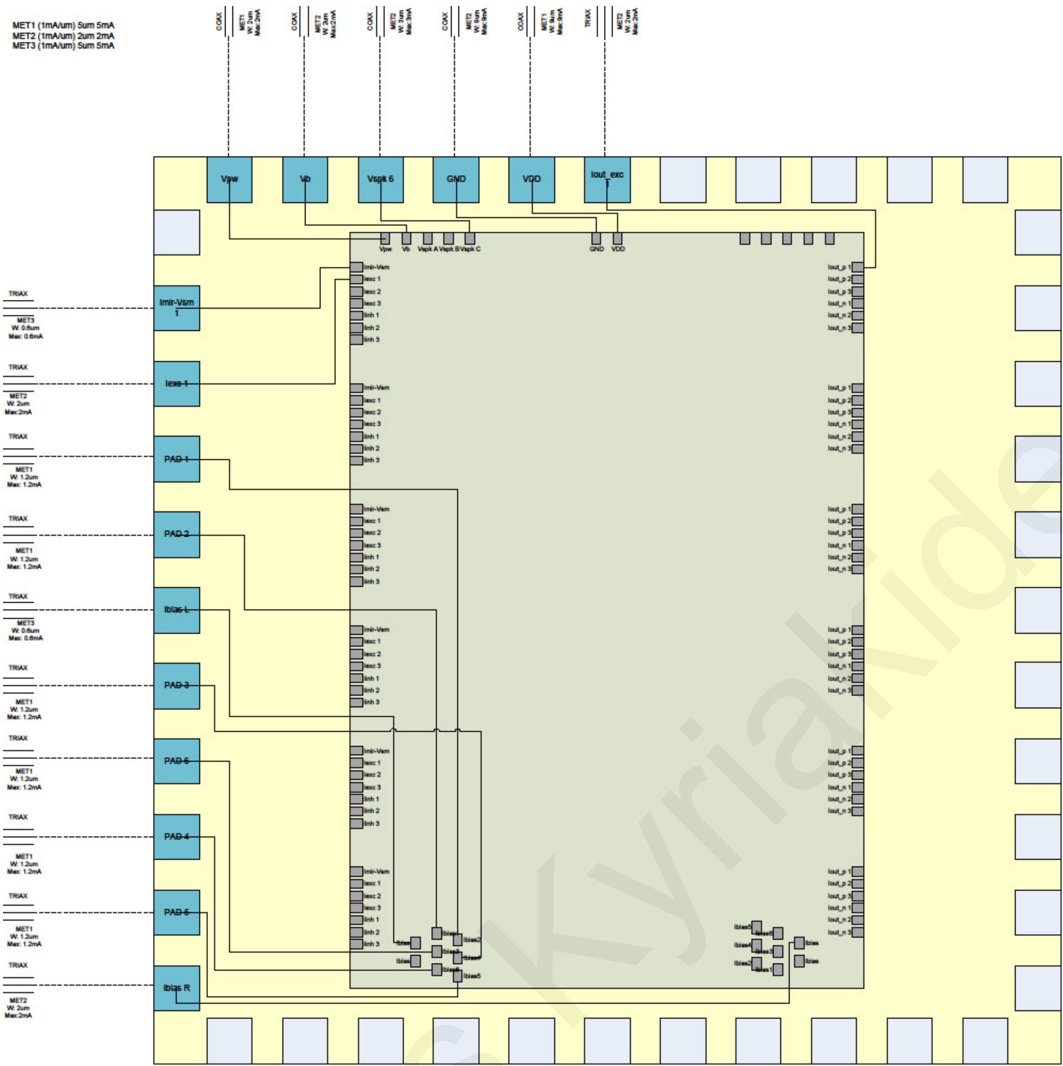

Figure D.11: The packet's connection diagram showing connection type and necessary compliance.

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