University of Cyprus
Department of Mechanical and Manufacturing Engineering

COMPLEX FUNCTIONAL OXIDES FOR THERMAL MANAGEMENT AND RESISTIVE SWITCHING APPLICATIONS

DOCTOR OF PHILOSOPHY DISSERTATION

CHARIS ORFANIDOU

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COMPLEX FUNCTIONAL OXIDES FOR THERMAL MANAGEMENT AND RESISTIVE SWITCHING APPLICATIONS

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VALIDATION PAGE

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COMPLEX FUNCTIONAL OXIDES FOR THERMAL MANAGEMENT AND RESISTIVE SWITCHING APPLICATIONS

The present Doctoral Dissertation was submitted in partial fulfillment of the requirements for the Degree of Doctor of Philosophy at the ***Department of Mechanical and Manufacturing Engineering*** *and was approved on the* ***December 12, 2018*** *by the members of the Examination Committee.*

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DECLARATION OF DOCTORAL CANDIDATE

The present doctoral dissertation was submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy of the University of Cyprus. It is a product of original work of my own, unless otherwise mentioned through references, notes, or any other statements.

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ABSTRACT

Ever-increasing miniaturization and high-demanding computer memory and processor industry require fast, miniaturized, reproducible and "cool" electronic devices. Novel materials that are able to lower processor temperature, and new device structures for faster and miniaturized computer memories are currently investigated.

In this thesis technological application related features of $La_5Ca_9Cu_{24}O_{41}$ and Li_xCoO_2 materials have been studied. In particular, a feasibility simulation study using $La_5Ca_9Cu_{24}O_{41}$ material for heat channeling in Extremely-Thin-Silicon-on-Insulator devices was accomplished, and an experimental study of Resistive Switching phenomena in Li_xCoO_2–based memory cells was carried out in order to identify the mechanism governing these phenomena.

$La_5Ca_9Cu_{24}O_{41}$ was selected for this study, as a material with highly anisotropic thermal conductivity, while at the same time is an electrical insulator. For that reason the possible use of it in electronic devices can be of high research interest.

Li_xCoO_2 is an extensively studied material and widely known for its use as a cathode material in Li-ion rechargeable batteries. Nevertheless, it has recently been shown to also exhibit resistive switching characteristics. The fundamental mechanism underlying the resistive switching behavior could be of high research and industrial interest.

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Περιληψη

Η υψηλά απαιτητική βιομηχανία υπολογιστών για γρήγορη σμίκρυνση των επεξεργαστών και της μνήμης τους απαιτεί ηλεκτρονικές συσκευές γρήγορες, με το μικρότερο μέγεθος, με σταθερότητα και λειτουργία σε χαμηλές θερμοκρασίες. Νέα υλικά που επιτρέπουν την λειτουργία των επεξεργαστών σε χαμηλή θερμοκρασία, και νέες δομές για ταχύτερες και μικρότερες σε μέγεθος μνήμες ηλεκτρονικών υπολογιστών μελετώνται.

Για την διατριβή αυτή, έχουν μελετηθεί ιδιότητες των υλικών $La_5Ca_9Cu_{24}O_{41}$ και Li_xCoO_2, σχετικές με τη χρήση τους σε τεχνολογικές εφαρμογές. Συγκεκριμένα, μελέτη προσομοίωσης πιθανής χρήσης του υλικού $La_5Ca_9Cu_{24}O_{41}$ για διοχέτευση της υψηλής θερμικής ροής στο εξωτερικό μέρος μίας εξαιρετικά-λεπτής-συσκευής-πυριτίου-πάνω-σε-μονωτή (ETSoI) έχει επιτευχθεί, και επίσης η μελέτη του φαινομένου της μεταγωγής αντίστασης του υλικού Li_xCoO_2 με σκοπό να εντοπιστεί ο μηχανισμός που διέπει αυτό το φαινόμενο πραγματοποιήθηκε.

Το υλικό $La_5Ca_9Cu_{24}O_{41}$ επελέγη για τη μελέτη αυτή ως υλικό με υψηλό βαθμό ανισοτροπίας στη θερμική αγωγιμότητα, ενώ την ίδια στιγμή είναι ένας ηλεκτρικός μονωτής. Για το λόγο αυτό η πιθανή χρήση του $La_5Ca_9Cu_{24}O_{41}$ σε ηλεκτρονικές συσκευές μπορεί να είναι υψηλού ερευνητικού ενδιαφέροντος.

Το Li_xCoO_2 είναι ένα υλικό ευρέως γνωστό για τη χρήση του ως υλικό καθόδου σε επαναφορτιζόμενες μπαταρίες Li-ion και εκτενώς μελετημένο. Παρόλα αυτά, έχει προσελκύσει την προσοχή μας από την πρώτη επίδειξη της μεταγωγής στην αντίστασή του το 2011 από τον A Moradpour *et al.* Η απλότητα του προτεινόμενου μηχανισμού θα μπορούσε να είναι ερευνητικά και από τη σκοπιά της βιομηχανίας πολύ ενδιαφέρουσα.

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List of Publications

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LIST OF CONFERENCES

1. ***C. M. Orfanidou***, C. N. Mihailescu, V. H. Mai, V. S. Nguyen, O. Schneegans, G. Stan and J. Giapintzakis, **oral** presentation: "Resistive switching behavior in Li_xCoO_2-based devices fabricated on Si", E-MRS Fall Meeting 2016, Warsaw, Poland.
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ABBREVIATIONS

AE	Active Electrode
BOX	Buried Oxide layer
CE	Counter Electrode
CMOS	Complementary-Metal-Oxide-Semiconductor
DRAM	Dynamic Random Access Memory
ECM	Electrochemical Metallization Memory
ETSoI	Extremely Thin Silicon-on-Insulator
Fe-RAM	Ferroelectric Random Access Memory
FEA	Finite Elements Analysis
FOX	Field Oxide layer
HRS	High Resistive State
$\mathbf{I_{off}}$	Current, I, at the high resistive state
$\mathbf{I_{on}}$	Current, I, at the low resistive state
LCCO	$La_5Ca_9Cu_{24}O_{41}$
LRS	Low Resistive Stare
M-RAM	Magnetic Random Access Memory
MIM	Metal/Isulator/Metal
MIT	Metal-to-Insulator-Transition
NVM	Non-volatile memory
PC-RAM	Phase Change Random Access Memory
PDE	Partial Differential Equations
RAM	Random Access Memory
ROM	Read-Only Memory
RRAM	Resistive Random Access Memory
RS	Resistive Switching
SoI	Silicon-on-Insulator
SRAM	Static Random Access Memory
TIM	Thermal Interface Material
TCM	Thermochemical Memory
VCM	Valence Change Memory
$\boldsymbol{\kappa}$	Thermal conductivity
$\boldsymbol{\kappa}_{a,\ b,\ or\ c}$	Thermal conductivity along the *a*, *b*, or *c*-axis

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Chapter 1

Introduction

1.1 Motivation on Thermal Management topic

Silicon-on-insulator (SoI) devices are of particular interest for thermal management studies, as they suffer from severe self-heating because of the very low and isotropic thermal conductivity of silicon dioxide that is being used as a buried oxide (BOX) layer. $La_5Ca_9Cu_{24}O_{41}$ (LCCO) exhibits highly anisotropic magnon-mediated thermal conductivity while at the same time is electrically insulating.

The aim of this scientific work is to simulate and find out whether the incorporation of LCCO thin films into extremely thin SoI devices could lead to lower operational temperatures of the transistors build on these devices. In order to study the effect of these phenomena, a series of simulation studies have been carried out that deal with the design of an effective thermal management solution for transistors built on ETSoI wafers with an LCCO BOX layer.

We evaluate the potential of using LCCO BOX layer to resolve thermal management problems in transistors built on ETSoI wafers, and demonstrate a decrease both in the operating temperature of the device and in the temperature of the adjacent-to-a-hot-spot transistor.

This particular part of the thesis was funded by the European Commission via Marie Curie ITN Actions, FP7, LOTHERM (Low-dimensional quantum magnets for thermal management) project.

Moving further, another potential way to minimize the dissipated heat from electronic devices is the upgrade of processor technology to neuromorphic computing processors. Since this type of processors will be designed to emulate human brain

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processing, they should be accompanied with significantly lower operating temperatures. A class of promising devices in this direction is Resistive Switching (RS) devices.

1.2 Motivation on Resistive Switching topic

The potential applications of RS extend from non-volatile resistive random access memory (RRAM) to memristor-based logic devices and neuromorphic computing systems (Snider 2008). Identification of the RS mechanism in the proposed memristive cells - which also behave as nanobatteries (Valov 2013) - is the final obstacle that researchers need to overcome in order to transition from “lab” to “fab” manufacturing (Waser 2009, Ielmini, 2011, Ielmini 2016).

The initial possible application of such devices is Resistive Random Access Memories (RRAM), that is a Non-volatile memory (NVM). These devices are based on the switching of their resistance between two states, ON, and OFF, or else, 1, and 0, respectively. RS devices that show multistate switching, i.e., more than two resistive states, could lead to the design of neuromorphic computing devices.

RS in metal-insulator-metal (MIM) structures was originally reported in the 1960’s (Hickmott 1962) and has attracted the renewed interest of the information materials and devices community during the last decade (Ha 2011, Ielmini 2011, Linn 2010, Muenstermann 2010, Waser 2009, Waser 2007, Rozenberg 2004).

The filamentary mechanism occasionally implies an electroforming step prior to operation. Furthermore, the downscaling potential of filamentary RS devices may be limited by the filament size (Dittmann 2012). Although research efforts are mainly focused on the deeper understanding of the filamentary RS mechanism, identifying materials where a bulk mechanism is responsible for RS, in addition to being compatible with the current integrated circuit technology, can also be of high research interest. Taking advantage of recent advancements in Li integration into current CMOS processes (Kutbee 2016), an emergent structure belonging to this category is the Li_xCoO_2-based RS device (Moradpour 2011, Mai 2015).

Li_xCoO_2, a well-known cathode material used in Li-ion rechargeable batteries for decades, has recently been proposed as a potential candidate for RRAM and neuromorphic system applications (Mai 2015). We have fabricated MIM cells based on Li_xCoO_2 thin films grown on Si substrates covered with a thin layer of SiO_2 and employed two-probe current-voltage measurements to investigate the resistive switching behavior of the devices. The results address the effect of SiO_2- and Li_xCoO_2-layer thickness and of Si type

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and orientation on the RS behavior of these cells. Also, repeatability of the RS phenomena is tested along with the effect of lithium content, x, to the phenomena.

Furthermore, even though it has already been observed that Li ions are involved in the RS (Nguyen 2018), the relation of Li stoichiometry to the RS mechanism remains unanswered. An important question concerns the nature (filamentary/homogeneous) of the RS. Hence in this part of the thesis, Au/Li_xCoO_2/SiO_2/Si cells have been investigated using conventional two-probe current-voltage measurements, with the aim of understanding the origin and nature of the mechanism that governs RS phenomena in these cells.

The aim is to define the mechanism governing the phenomena. Identification of the RS mechanism in memory cells investigated so far is the greatest obstacle that researchers need to overcome in order to step further from "lab" to "fab" manufacturing. A deep understanding of RS mechanism is desirable in confronting key technological issues like reliability, variability and noise of RRAM devices, which exhibit low power consumption, ns-range response times and scalability down to atomic scale (Ielmini 2016, Valov 2013).

1.3 Thesis Structure

This thesis is subdivided in 5 chapters. It is separated regarding the possible application of each material studied.

Chapter 2 discusses the topic of thermal management. What thermal management solutions are being used in the electronics industry and which could be a novel thermal management solution. Initially, the thermal management problem is stated, and some current thermal management solutions are identified. Subsequently, novel thermal management solutions are shown and the $La_5Ca_9Cu_{24}O_{41}$ (LCCO) novel material and its thermal properties are discussed and which is the role of the LCCO material in thermal management solution. To further support the simulation approach realized using the novel LCCO material, the model - that was build using computer-aided engineering (CAE) software - is discussed step by step in this chapter.

Chapter 3 introduces the topic of resistive switching (RS) phenomena. Initially the roadmap of non-volatile memories is discussed as well as the background theory of RS phenomena and the electrochemical processes involved. Li_xCoO_2 material structure and electrical properties are also presented. Research already published on RS phenomena in Li_xCoO_2-based memory cells is discussed subsequently.

In chapter 4, the experimental techniques used in order to realize this thesis are presented. Firstly, the thin film deposition techniques are discussed, and secondly the

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characterization techniques. Subsequently, the obtained results from parametric studies on the Au/Li_xCoO_2/SiO_2/Si memory cell are shown, followed by the interpretation of each experiment. The target of this part of the thesis is to unfold the RS mechanism that governs Au/Li_xCoO_2/SiO_2/Si memory cells. Memory cells based on Li_xCoO_2 thin films have been grown on Si substrates and two-probe current-voltage measurements were employed to investigate the origin and nature of the RS behavior exhibited by these cells.

Chapter 5 summarizes the work done in this thesis. The thermal management and RS topics are reviewed and their key results highlighted.

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Chapter 2

$La_5Ca_9Cu_{24}O_{41}$ for Thermal Management Applications

2.1 Introduction

This chapter discusses the topic of thermal management. What thermal management solutions are being used in the electronics industry and which could be a novel thermal management solution.

Initially, the thermal management problem is stated, and some current thermal management solutions are identified. Subsequently, novel thermal management solutions are shown and $La_5Ca_9Cu_{24}O_{41}$ (LCCO) novel material and its thermal properties are discussed. Which is the role of LCCO material in thermal management solution?

To further support the simulation approach realized using the novel LCCO material, the model - that was build using computer-aided engineering (CAE) software - is discussed step by step in this chapter.

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2.2 Thermal Management Solutions for Electronic devices

Thermal management of electronic devices preoccupies the computer and electronics engineers since the fabrication of the first computer machine (Hartree 1946). Although the evolution of electronic devices (vacuum tubes → solid-state silicon devices (Baker 2002) → bipolar transistor → CMOS devices) offered some respite, the problem is still of major importance due to the ever continuing device miniaturization and increasing transistor density (Wang 2018, Yueh 2016, An 2014, Merkel 2014, Henkel 2013, Ball 2012, Sridhar 2010, Lin 2008, Pedram 2006, Shahidi 2006, Semenov 2006, Schmidt 2005). Figure 2.1 shows the rising heat output of microchips as their transistors switched from bipolar to CMOS technology and the device densities continued to increase (Ball 2012, Cengel 2002).

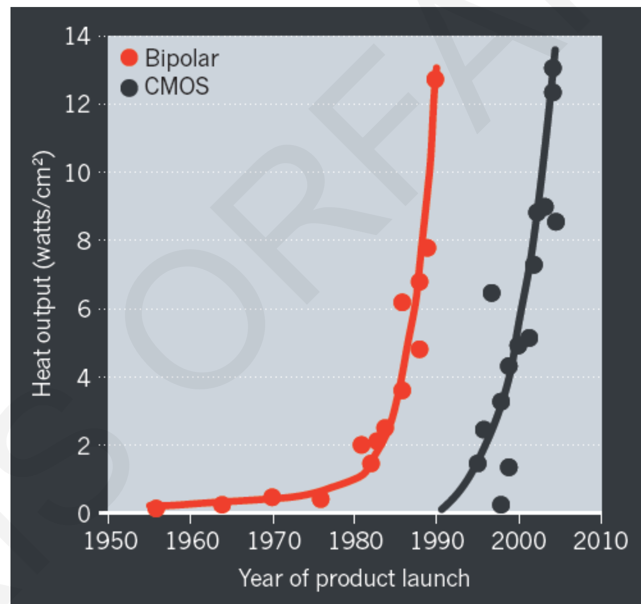

Figure 2.1 *As transistors technology is switching from bipolar to CMOS, microchips' heat output was lowered, but with the increase of device densities have quickly driven up again (Ball 2012).*

Over the years many thermal management methods have arisen and others are still in research. From system-level (Tong 2011, Lin 2008), to board-level and chip-level packaging thermal management, components like fans, blowers, heat sinks, heat pipes (Kang 2006), thermal interface materials (TIMs) (Cho 2016, Pop 2012, Shahil 2012), liquid cooling (Sridhar 2010), Peltier cooling plates and thin film thermoelectric coolers (Barletta 2016, Chowdhury 2009, Anandan 2008), as well as microfluidic redox flow cells

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(Marschewski 2016 & 2015) have an important role in thermal management issues. A lot of research has been done in order to find out the most efficient materials for heat sinks, the best shape and geometry of the same, thermodynamics of the system heat sink-fan etc.

Thermal design of a system is very crucial including hardware components and thermal modeling and monitoring (Intel® 2016, Kursun 2009). Taking further this subject there are only few studies that showed potential solid-state thermal management solutions directly integrated at the CMOS transistor-level (Jeppson 2016, Balandin 2015, Orfanidou 2013, Subrina 2009).

2.2.1 Passive and Active Thermal Management

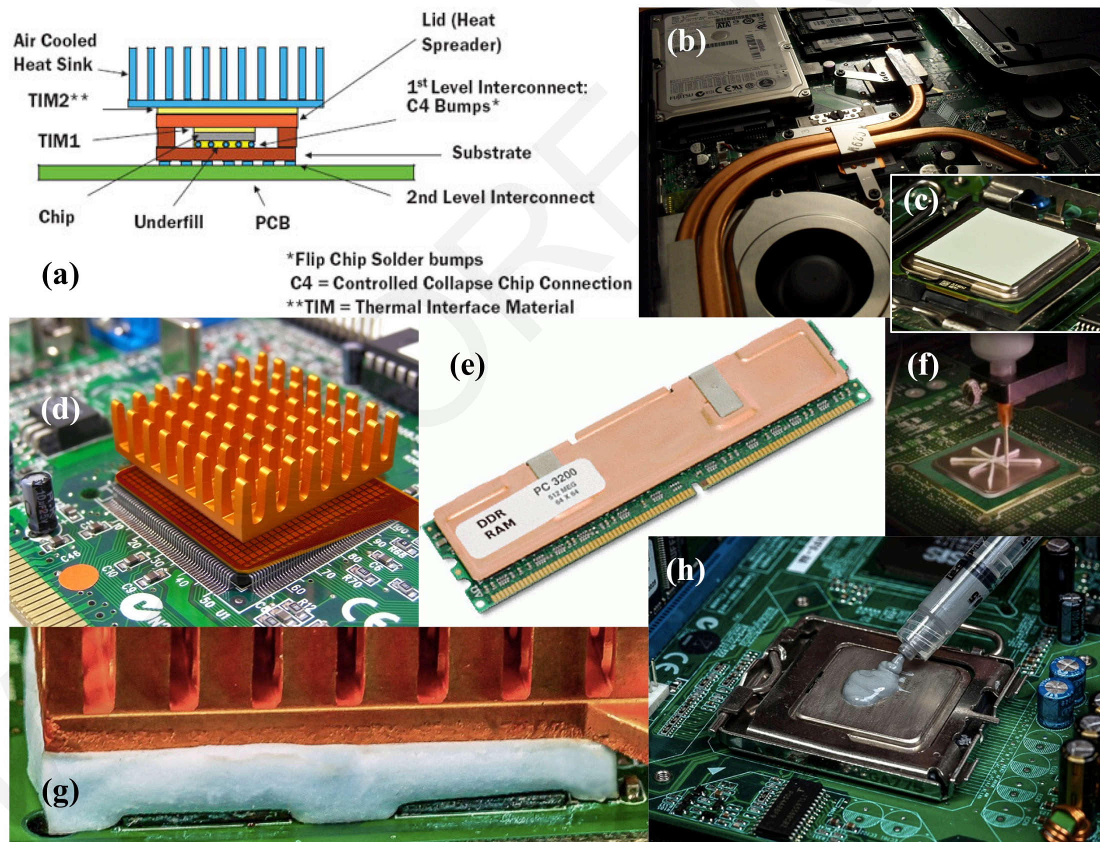

Figure 2.2 *Passive thermal management components. (a) Diagram of a flip-chip IC in a high-performance package with attached heat sink, (b) laptop heat pipe, (c) phase change interface material, (d) heat sink, (e) heat spreader on RAM, (f) thermally conductive grease, (g) heat sink on gap filler thermal pad, (h) thermal conductive paste.*

Passive thermal management (Figure 2.2) is the most common solution that is taking advantage of the thermodynamics of conduction, convection and less radiation. The components that are used to minimize the excessive highly localized temperatures of the electronic devices are not very expensive and are easy to implement. The most frequently used and so far essential thermal management component of an electronic device is the heat sink. In order to have a good heat transfer coefficient, heat sinks are made of high thermal conductivity materials, like aluminum and aluminum alloys or copper, and have a comb- or fin-like structure that increases the surface area.

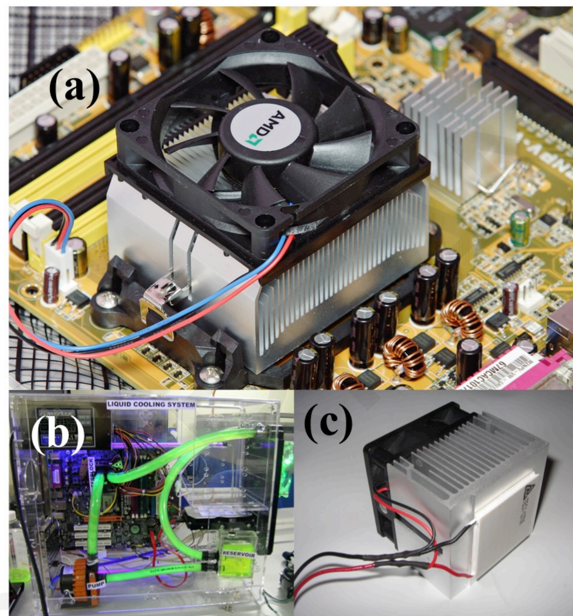

Figure 2.3 *Active thermal management components. (a) Heat sink with fan from AMD Semiconductor Company, (b) liquid cooling system, (c) Peltier cooling plate.*

Active thermal management (Figure 2.3) refers to cooling technologies that must introduce energy to augment the heat transfer process. Active thermal management components increase the rate of fluid flow during convection, which improves dramatically the rate of heat removal. Some of their drawbacks are that they need to use electricity in order to operate consequently most of the times they introduced audible noise to a system. Also they are generally more complex and expensive than passive systems.

2.2.2 Novel Thermal Management Solutions

Planar manufacturing processes in the semiconductor industry have evolved from bulk silicon to silicon-on-insulator (SoI) and lately to extremely thin SoI (ETSoI) (also known as extremely thin fully depleted SoI) (Malviya 2018, Cheng 2016, Morin 2016, Shin 2016, Yang 2015, Yeh 2015, Sampedro 2013, Khakifirooz 2012a, Khakifirooz 2012b, Aulnette 2011, Cheng 2011, Kulkarni 2011, Majumdar 2009a, Majumdar 2009b, Majumdar 2008) technologies because of suppression of short-channel effects implemented by the insulating buried oxide (BOX) layer. However, SoI devices suffer from severe self-heating because the insulating oxide layer (SiO_2) and the thin silicon layer (Shamsa 2008, Pop 2004) have a very low thermal conductivity, which impedes effective heat removal (Pop 2006, Su 1994). Moreover, the increase of the total power generation in combination with occasionally malfunctioning transistors result in hotspots, which increase the temperature locally, and of the adjacent transistors (Shrivastava 2011).

Therefore, it is evident that new thermal management solutions are needed. Many research projects are oriented in this direction seeking solutions at both component and system level (Barletta 2016, Cho 2016, Jeppson 2016, Marschewski 2016, Balandin 2015, Burzo 2012, Shahil 2012, Yan 2012, Cher 2011, Jiménez 2010, Subrina 2009, Bachmann 2008, Shamsa 2008, Mahajan 2006). In particular, (Subrina 2009 & 2011) simulated the incorporation of graphene or a few-layer graphene (FLG) in a SoI device and showed that this approach could be efficient in heat removal. It is noted that graphene or FLG was placed below the BOX layer (SiO_2) because graphene is a good electrical conductor and could cause short-circuiting.

With simulation studies of heat channeling, we propose a novel solution that involves the integration in ETSoI devices of the 1-D Heisenberg quantum antiferromagnet LCCO, in place of the SiO_2 layer. The advantages of LCCO in comparison with SiO_2 and graphene are that LCCO is an electrical insulator with a high anisotropic thermal conductivity (Hess 2001).

2.3 $La_5Ca_9Cu_{24}O_{41}$ (LCCO) compound

2.3.1 LCCO crystal stucture

LCCO belongs to the family of spin ladder materials and was discovered as a byproduct of the high T_c superconductors back in 1988 (McCarron III 1988). LCCO is a 1-

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D Heisenberg quantum antiferromagnet and its structure is shown in Figure 2.4. Figure 2.4 (a) shows the unit cell of high complexity and huge volume of 316 atoms. Figure 2.4 (b) shows the two types of chains and ladder planes and (c) the parallel ladders along the *c*-axis. Between the copper ions along the ladder direction and between the two copper ions forming the rung, there are bonds at 180° that lead to strong antiferromagnetic interactions and between the copper ions of two adjacent ladders there are bonds at 90°, which lead to almost 10 times weaker ferromagnetic interactions, as can derive from the Goodenough-Kanamori rule (Kanamori 1959).

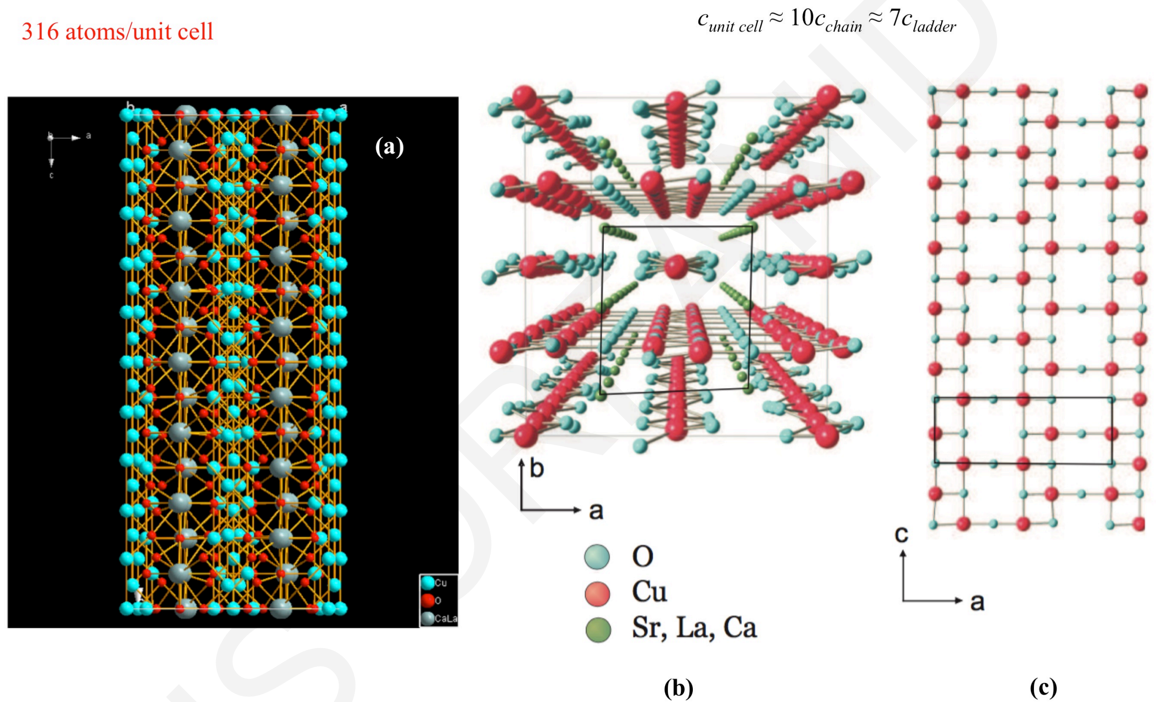

Figure 2.4 *Crystal structure of LCCO. (a) LCCO has a unit cell of high complexity with a huge volume and 316 atoms/unit cell as well as incommensurability along the c-axis. (b) Top view of the a-b plane, where the black square indicates the dimensions of the unit cell. (c) Top view of the a-c plane where the black square indicates the dimensions of the ladder unit cell. Figures (b) and (c) taken from (Otter 2012a).*

The orientation of the chains (or ladders) defines the crystallographic *c*-axis, where the lattice constants of these two subsystems satisfy in good approximation: $c_{\text{unit cell}} \approx 10c_{\text{chain}} \approx 7c_{\text{ladder}}$ (incommensurable structure). Furthermore, the spins of copper ions on the adjacent ladders are frustrated, thereby decreasing the interactions between ladders to almost zero. The copper ions are connected through super-exchange interaction, leading to a large exchange of energy. The lattice parameters are a = 11.479 Å, b = 13.406 Å, and

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c_{ladder} = 3.934 Å (Gotoh 2003). The lattice has orthorhombic symmetry with space group CCCM (Siegrist 1988, Ammerahl 1999).

2.3.2 Thermal Conductivity of LCCO

In 1997 X. Zotos *et al.* theoretically predicted that low-dimensional quantum magnet materials are expected to exhibit ballistic heat transport (Zotos 1997). Later, in 2001, these predictions were verified by C. Hess *et al.* that have measured highly anisotropic ($\kappa_c/\kappa_{a,b} \approx 50$) thermal conductivity of LCCO in single crystal form, as a function of temperature, with a steady-state method (Hess 2001). Room temperature thermal conductivity of LCCO is in the order of 100 W/(m·K)$^{-1}$ (as efficient as metallic heat conduction) along the *c*-axis of the crystal, because of magnon contribution, and ~2 W/(m·K)$^{-1}$ along *a*- and *b*-axis of the crystal, because of phonon contribution, see Figure 2.5, (Hess 2001).

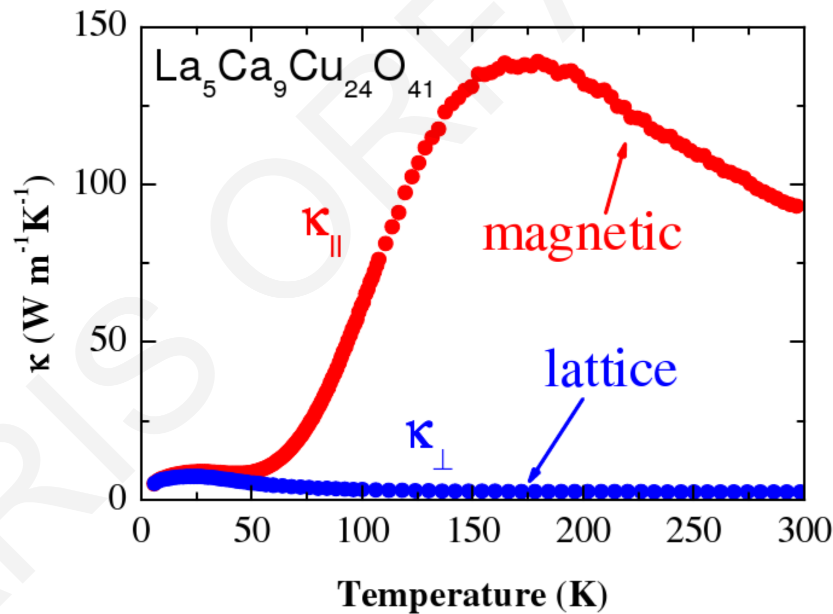

Figure 2.5 *Thermal conductivity of the spin ladder material LCCO, measured parallel ($\kappa_{||}$) and perpendicular ($\kappa_\perp$) to the ladders. Data from (Hess 2001).*

Compared to conventional materials with high thermal conductivity, this novel LCCO compound, with highly efficient magnetic mode of thermal conduction, offers essential advantages: a) It is electrically insulating and can, therefore, be used to simultaneously electrically insulate electronic circuits and carry away heat, b) heat is conducted primarily along one crystal axis, hence the material can thermally insulate in two directions and carry away heat along the other and c) heat is carried by localized spins

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which could allow for tunable heat conductivity at room temperature by manipulation of the spins with magnetic fields or light.

2.4 Model of Simulation Studies

Taking advantage of the highly anisotropic nature of LCCO, it is evaluated the potential of using LCCO BOX layer to resolve thermal management problems in transistors built on ETSoI wafers, and is demonstrated a decrease both in the operating temperature of the device and in the temperature of the adjacent to a hot-spot transistor.

2.4.1 Software used in Simulations

Simulation and modeling of physical phenomena is of increasing demand as manufacturing processes need to be faster and more precise. Simulation tools, homemade or commercial, are used for optimization, verification and validation purposes (Banks 1996, Dahl 1966), as well as for feasibility studies.

The simulation studies in this thesis performed using COMSOL Multiphysics software package, version 4.2a. COMSOL software package belongs to the wide category of computer-aided engineering (CAE) softwares and more specifically is a finite element analysis (FEA) tool. It has application-specific modules for various physics phenomena like: AC/DC Module, Batteries & Fuel Cells Module, Microfluidics Module, Heat Transfer Module and others (COMSOL 2011).

In COMSOL the design of the model involves several steps that include:

1) Specification of the geometry of the under study object (computer-aided design (CAD));
2) Division of the object into subdomains;
3) Description of every subdomain;
4) Specification of subdomains' boundaries.

During the model design in COMSOL, the user can specify the power of the heat source and the thermal conductivity of the materials used (in our case LCCO, silicon, and SiO_2). The simulation includes dividing (meshing, see Figure 2.6) of the specific geometry and structural components (for our studies an ETSoI device on a BOX layer) and solving heat conduction equations for each component.

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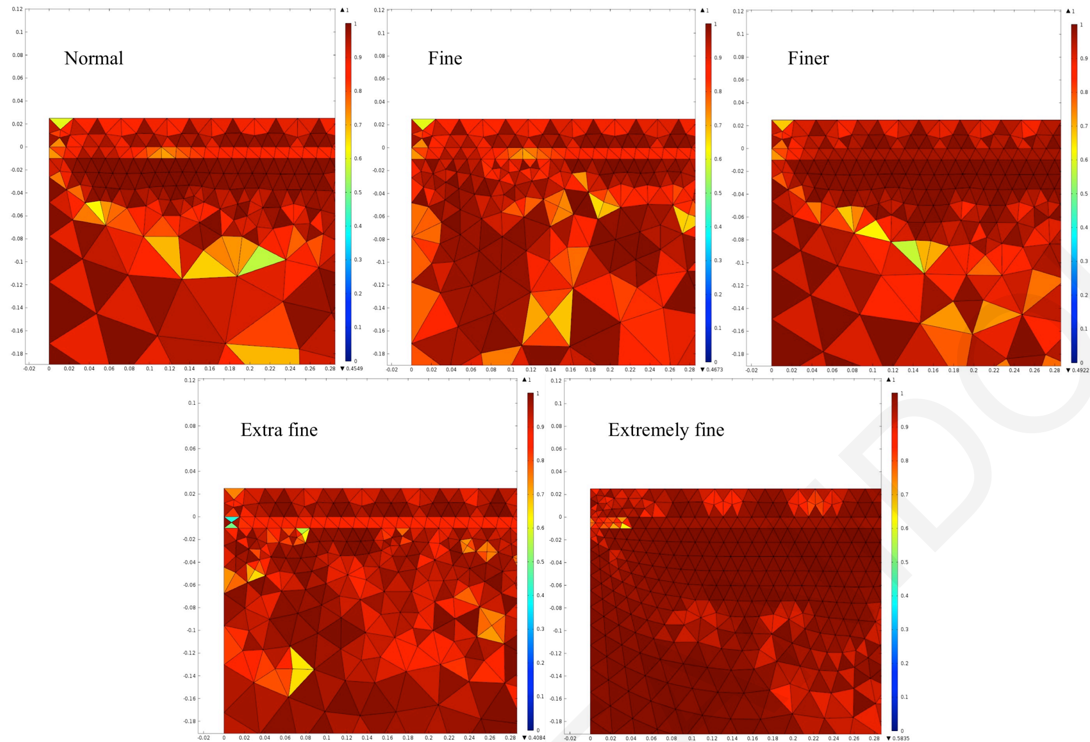

Figure 2.6 *Example of the physics-controlled mesh quality from a normal to an extremely fine element size of a 2-D structure.*

2.4.2 Finite Element Analysis (FEA)

FEA is a numerical method for finding approximate solutions of partial differential equations (PDE), boundary-value problems and integral equations (Chaskalovic 2008, Bathe 1976). The solutions are mostly based on dividing the simulated object into a large set of very small components and linearizing the differential equations within each of the components. The principle of the finite element method is to replace an entire continuous domain by a number of subdomains in which the unknown function is represented by simple interpolation functions with unknown coefficients, thus, the original boundary-value problem with an infinite number of degrees of freedom is converted into a problem with a finite number of degrees of freedom, or in other words, the solution of the whole system is approximated by a finite number of unknown coefficients. Then a set of algebraic equations or a system of equations is obtained and solution of the boundary-value problem is achieved by solving the system of equations. Therefore, a FEA of a boundary-value problem should include the following basic steps: i) Domain discretization, ii) selection of the interpolation functions, iii) formulation of the system of equations, and iv) solution of the system of equations.

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2.4.2.1 Domain discretization

The discretization of the domain, say Ω, is the first and perhaps the most important step in any FEA because the manner in which the domain is discretized will affect the computer storage requirements, the computation time, and the accuracy of the numerical results. In this step, the entire domain is subdivided into a number of small domains, denoted as (e = *1, 2, 3, …, M*), with M denoting the total number of subdomains. These subdomains are usually referred to as the elements. For a one-dimensional (1-D) domain that is actually a straight or curved line, the elements are often short line segments interconnected to form the original line. For a two-dimensional (2-D) domain, the elements are usually small triangles and rectangles (Figure 2.7 (a)). The rectangular elements are, of course, best suited for discretizing rectangular regions, while the triangular ones can be used for irregular regions. In a three-dimensional (3-D) solution, the domain may be subdivided into tetrahedral, triangular prisms, or rectangular bricks (Figure 2.7 (a)), among which the tetrahedral are the simplest, and best suited for arbitrary-volume domains. We note that the linear line segments, triangles, and tetrahedral are the basic 1-, 2-, and 3-D elements that model curved lines or surfaces by straight-line segments or planar patches. In Figure 2.7 (b), there are examples showing the finite element discretization of 3-D domains.

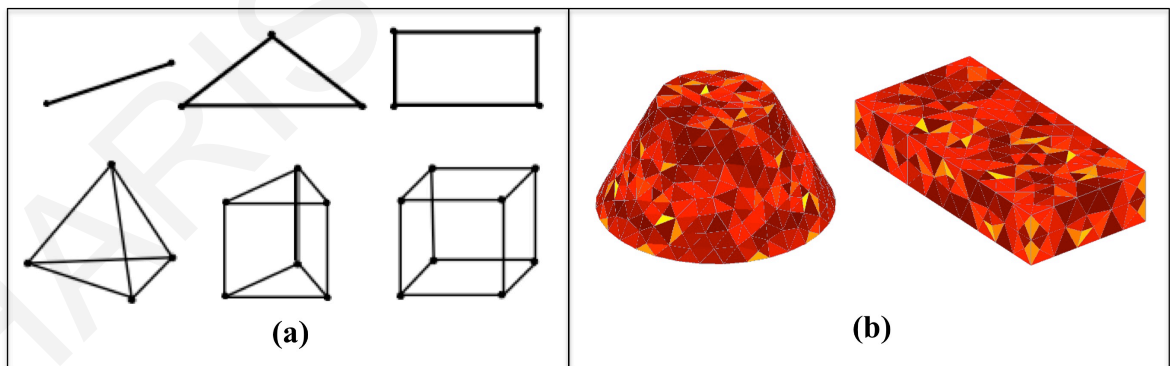

Figure 2.7 *(a) Basic finite elements: 1-D, 2-D, and 3-D. (b) Examples of 3-D finite element discretization.*

In most finite element solutions, the problem is formulated in terms of the unknown function ϕ at nodes associated with the elements. For example, a linear line element has two nodes, one at each endpoint. A linear triangular element has three nodes, located at its three vertices, whereas a linear tetrahedron has four nodes, located at its four corners. For

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implementation purposes, it is necessary to describe these nodes. A complete description of a node contains its coordinate values, local number, and global number. The local number of the node indicates its position in the element, whereas global number specifies its position in the entire system.

2.4.2.2 Selection of interpolation functions

The second step of a FEA is to select an interpolation function that provides an approximation of the unknown solution within an element. The interpolation is usually selected to be a polynomial of first (linear), second (quadratic), or higher order. Higher-order polynomials, although more accurate, usually result in a more complicated formulation. Hence, the simple and basic linear interpolation is still widely used. We can define a typical boundary-value problem as,

$$\Gamma \phi = f \tag{2.1}$$

where Γ is a differential operator, f is the excitation or forcing function, and ϕ is the unknown quantity and it is assumed that the problem is real valued.

2.4.2.3 Formulation of the System of Equations

The third step, also a major step in a FEA, is to formulate the system of equations. Both the Rayleight-Ritz variational and Galerkin methods can be used for this purpose (Chaskalovic 2008, pp. 63 – 111). Considering the Rayleight-Ritz variational formulation we end up with,

$$[W]\{\phi\} = \{b\} \leftrightarrow \left\{\frac{\partial F}{\partial \phi}\right\} = \sum_{e=1}^{M}\left([\overline{W^e}]\{\overline{\phi^e}\} - \{\overline{b^e}\}\right) = \{0\} \tag{2.2}$$

where $[W]$ is an $N \times N$ symmetric matrix with N being the total number of unknowns or nodes, $\{\phi\}$ an $N \times 1$ unknown vector whose elements are the unknown expansion coefficients, and $\{b\}$ an $N \times 1$ known vector. M is the number of the elements comprising the entire domain. All the vectors and matrices following the summation signs have been expanded or augmented.

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2.4.2.4 Simulation of the System of Equations

Solving the system of equations is the final step in a finite element analysis. The resultant system has one of the following two forms:

$$[W]\{\phi\} = \{b\} \tag{2.3}$$

or

$$[A]\{\phi\} = \lambda[B]\{\phi\} \tag{2.4}$$

Equation (2.3) is of the deterministic type, resulting from either an inhomogeneous differential equation or inhomogeneous boundary conditions or both. In the opposite, (2.4) is of the eigenvalue type, resulting from a homogeneous governing differential equation and homogeneous boundary conditions. In this case, the known vector $\{b\}$ vanishes and the matrix $[W]$ can be written as $[A] - \lambda[B]$, where λ denotes the unknown eigenvalues.

Once we have solved the system of equations for $\{\phi\}$, we can then compute the desired parameters, such as capacitance, inductance, input impedance, and scattering or radiation patterns and display the result in form of curves, plots, or color pictures, which are more meaningful and interpretable. This final stage, often referred to as post-processing, can also be separated completely from the other steps.

2.4.3 Model of Heat Conduction

2.4.3.1 Geometry

We have modeled the heat diffusion in the 2-D cross section of an ETSoI device that consists of a:

1) Si substrate at the bottom;

2) buried oxide (BOX) layer in the middle;

3) thin Si layer (Silicon-on-Insulator (SoI) layer) at the top;

4) wherein nine heat-generating transistors are embedded (Figure 2.8).

The space between the nine transistors is filled with SiO_2, the so-called field oxide (FOX). The thickness of the Si substrate is 500 μm in all the devices investigated whereas the

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thickness of the BOX layer is a parameter taking values from 10 to 150 nm. The topmost Si layer is 10-nm thick and the spacing between the transistors is also a parameter taking values from 1 to 5 μm. The total length of the device is 52 μm. We have simulated the nine transistors embedded in the thin Si layer of the device as rectangular operating elements (50 nm × 10 nm).

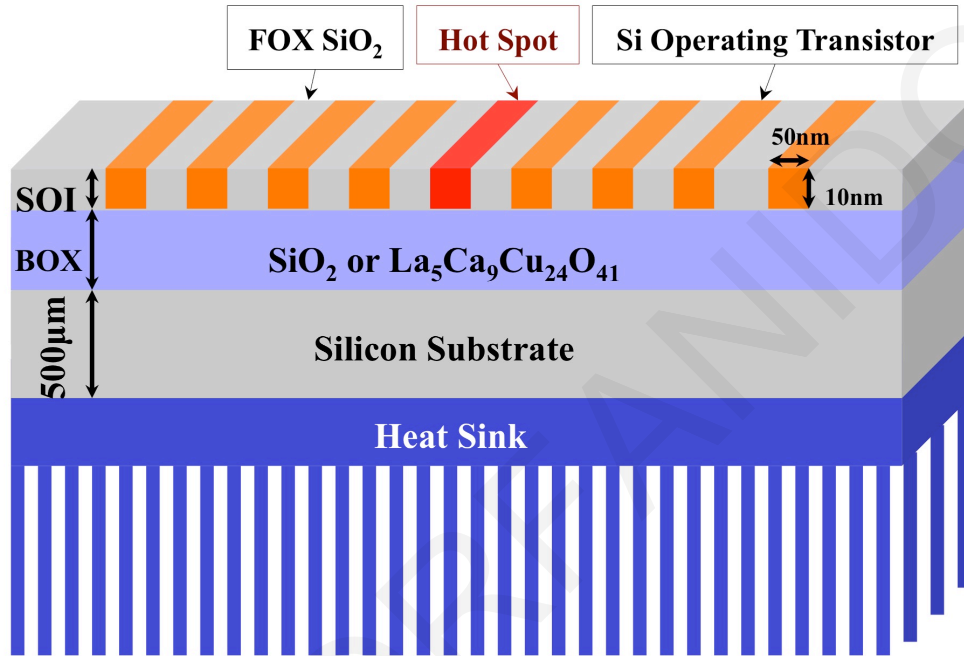

Figure 2.8 *Schematic showing the geometry of the devices we have simulated. The operating transistors are shown in orange, the hot-spot in red and the BOX layer (LCCO or SiO_2) in lilac. The thicknesses are not to scale.*

2.4.3.2 Heat transfer in Solids

We have treated "Heat Transfer in Solids *(ht)*" as a steady-state (stationary) problem (Equation 2.6). The equation governing pure conductive heat transfer in solids is:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-\kappa \nabla T) = Q \tag{2.5}$$

where ρ is the density of the material, C_p is the heat capacity at constant pressure of the material, κ is the thermal conductivity of the material, T is the absolute temperature, t the time for a time dependent study, and Q is the heat source. But since we have studied the problem at steady-state conditions equation 2.5 becomes:

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$$-\nabla \cdot (\kappa \nabla T) = Q \tag{2.6}$$

The thermal conductivities of all the three materials used in this study: LCCO, Si and SiO_2 are temperature dependent and the values have been taken from (Hess 2001, Glassbrenner 1964, Shackelford 2001), respectively. Specifically, thermal conductivity of LCCO is polar anisotropic (transverse isotropic) and is described as:

$$K = \begin{bmatrix} \kappa_a & 0 & 0 \\ 0 & \kappa_b & 0 \\ 0 & 0 & \kappa_c \end{bmatrix} \tag{2.7}$$

where $\kappa_a = \kappa_b = \kappa_x$ is the local value of the thermal conductivity in-plane (along the width of the device, *a-b* plane), and $\kappa_c = \kappa_y$ is the local value of the thermal conductivity cross-plane (along the thickness of the device, *c*-axis).

The heat conduction was modeled by solving numerically the steady state, 2-D heat diffusion equation:

$$\frac{\partial}{\partial x}\left(\kappa_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(\kappa_y \frac{\partial T}{\partial y}\right) = 0 \tag{2.8}$$

Additionally, a linear power density was applied at the silicon operating elements using Fourier's law:

$$-\left[\frac{\partial}{\partial x}\left(\kappa_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(\kappa_y \frac{\partial T}{\partial y}\right)\right] = Q \tag{2.9}$$

A linear power density of 100 W/m was used for the heat source, Q, of the operating elements, whereas for the hot-spot alone the linear power density was set to 300 W/m (Pop 2006, Subrina 2009, Ball 2012, Vassighi 2006).

The thermal conductivity of the thin Si layer is set at 14 $W/(m{\cdot}K)^{-1}$ because as the film is getting thinner, the thermal conductivity decreases due to phonon boundary scattering (Pop 2004, Fig. 2). Other material properties are shown in Table 2.1.

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	Silicon	**SiO_2**	**LCCO**
Heat capacity at constant pressure, C_p	$700\ \frac{J}{kg\cdot K}$	$730\frac{J}{kg\cdot K}$	T-dependent (Hess 2001)
Density, ρ	$2329\frac{k}{m^3}$	$2200\frac{k}{m^3}$	$5447.5\frac{k}{m^3}$
Thermal conductivity, κ	T-dependent (Glassbrenner 1964)	T-dependent (Shackelford 2001)	T-dependent (Hess 2001)

Table 2.1 *Basic material properties of Silicon, SiO_2, and LCCO for Heat transfer in solids module.*

2.4.3.3 Boundary conditions

The particular device has been studied under the following conditions:

1) when the transistors are operating under normal conditions and
2) when a hot-spot has been created.

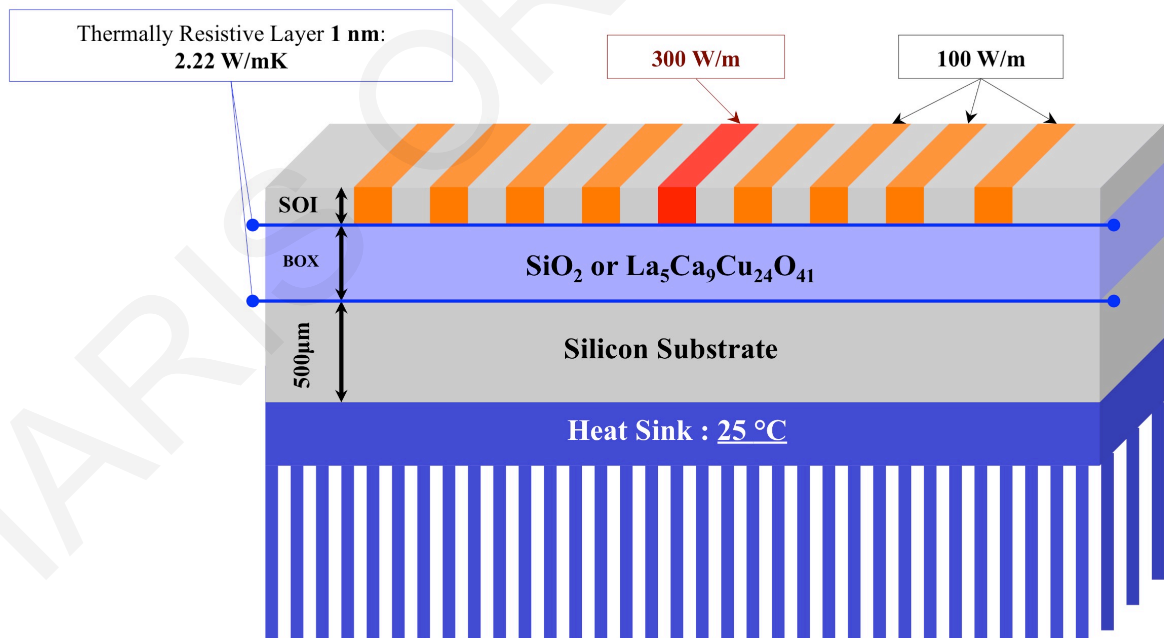

Figure 2.9 *Schematic showing the boundary conditions of the devices under study.*

In the latter case, the fifth operating element, counting from the left, plays the role of the hot-spot, as shown in Figure 2.9. In addition, we have examined and compared the effects of using as BOX layer either LCCO or SiO_2. A 1-nm-thick thermally resistive layer

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has modeled the internal boundaries between the components of the circuit with a thermal conductivity of 2.22 $W/(m \cdot K)^{-1}$ at both interfaces of Si/LCCO and Si/SiO_2 (Mahajan 2008). The external surfaces were modeled as adiabatic. Finally, a conventional heat sink is attached to the bottom of the device at a constant temperature $T = T_0 = 25°C$ (isothermal boundary condition).

2.5 Simulation Studies

2.5.1 Heat Channeling in ETSoI devices

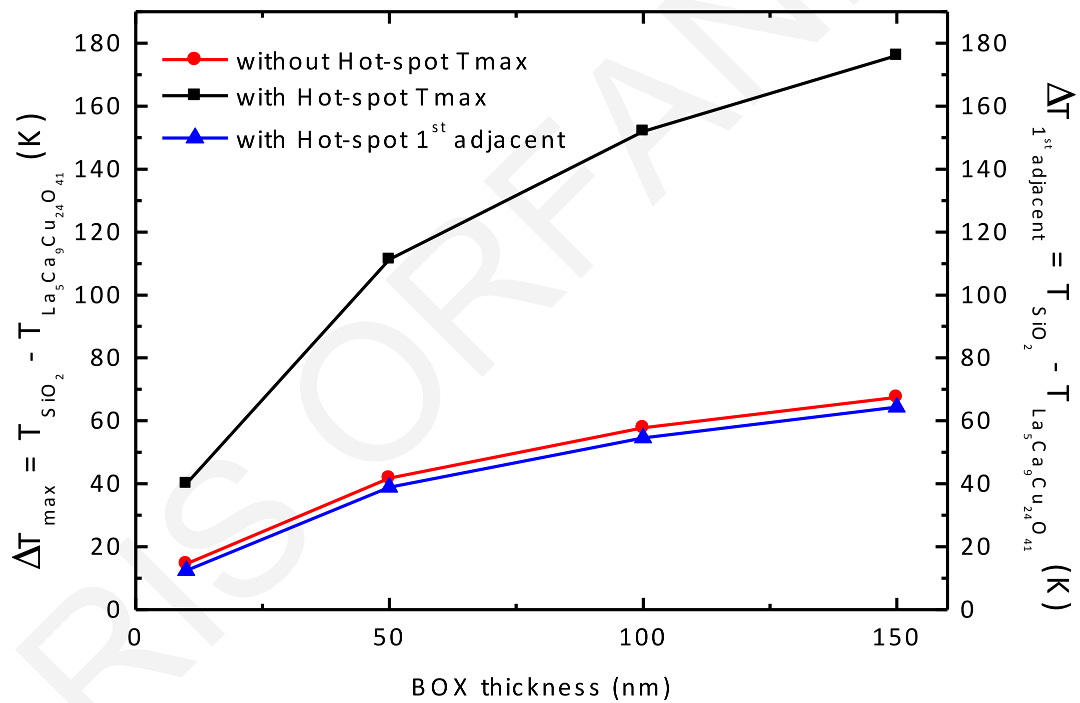

Figure 2.10 *Temperature differences for 1-μm spacing between transistors, obtained by subtracting from the temperature of the SoI device with a SiO_2 BOX layer, the temperature of the SoI device with an LCCO BOX layer. Left ordinate: circular dots (red line) are the temperature differences of the devices without the hot-spot, and square dots (black line) are the temperature differences of the devices with the hot-spot. Right ordinate: triangular dots (blue line) are the temperature differences locally at the first adjacent to the hot-spot operating transistor.*

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For the ETSoI device with 150-nm-thick SiO_2 BOX layer and 1-μm spacing between the transistors, the maximum obtained operating temperatures are 434.03 K for the case without the hot-spot and 570.55 K for the case with the hot-spot. This shows that the existence of a hot-spot increases drastically the operating temperature of all the transistors of the device and it is expected to affect even more the first adjacent transistors. Figure 2.10 shows temperature differences (ΔT_{max}) obtained by subtracting from the maximum operating temperature of an ETSoI device with a SiO_2 BOX layer, the maximum operating temperature of an ETSoI device with an LCCO BOX layer, as a function of the BOX thickness for the case of 1-μm spacing between transistors. As can be seen, T_{max} increases as the BOX thickness is increasing for both cases studied (with and without hot-spot) and higher temperature differences are obtained for the case of the device with the hot-spot.

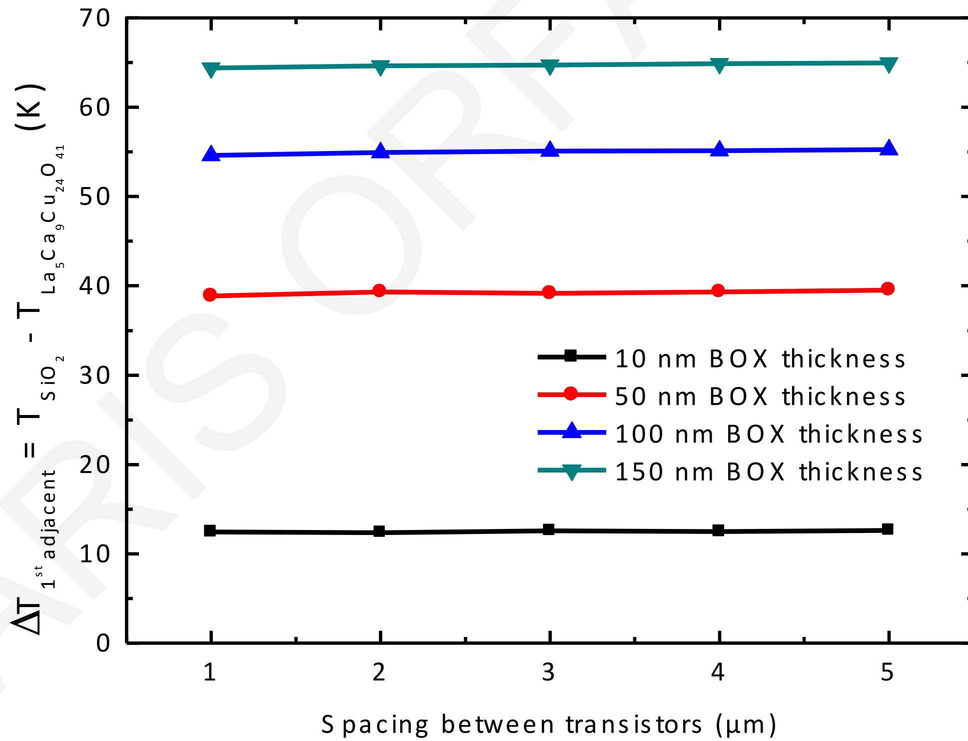

Figure 2.11 *Temperature differences obtained by subtracting from the local temperature at the first adjacent to the hot-spot operating transistor of the ETSoI device with a SiO_2 BOX layer, the local temperature of the ETSoI device with an LCCO BOX layer, for different spacing between the transistors of the device.*

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Therefore, LCCO BOX layer is even more efficient in the case of the device with the hot-spot. Additionally, Figure 2.10 shows the temperature differences $(\Delta T_{\text{first adjacent}})$ obtained by subtracting from the local temperature at the first adjacent to the hot-spot operating transistor (fourth transistor counting from the left) of an ETSoI device with a SiO_2 BOX layer, the corresponding local temperature of an ETSoI device with an LCCO BOX layer. Therefore, the use of LCCO BOX layer lowers significantly the overall operating temperature of the transistors as well as the temperature of the first adjacent to the hot-spot transistors.

Figure 2.11 shows temperature differences $\Delta T_{\text{first adjacent}}$, for different spacing between the transistors of the device. The graph demonstrates that the magnitude of $\Delta T_{\text{first adjacent}}$ is independent of the spacing between transistors. This occurred in all the studied cases (with and without hot-spot) because the space between the transistors is filled with a SiO_2 FOX that has minimum 1-μm width (in the *x*-direction) but the BOX layer has maximum thickness 150 nm (in the *y*-direction), so the heat is being conducted faster vertically than horizontally. Therefore, the results shown in Figure 2.10 are also independent of the spacing between transistors.

In Figure 2.12, we show the increase of operating temperature as the linear power density at the hot-spot is increasing from 100 to 300 W/m in devices with 10-nm BOX layer and 1-μm spacing between transistors. As can be seen, the operating temperature is increasing faster in the ETSoI device with SiO_2 BOX layer than in the ETSoI device with LCCO BOX layer. The slope is 0.25 $(\text{m·K})/\text{W}^{-1}$ for the ETSoI device with SiO_2 BOX layer and 0.15 $(\text{m·K})/\text{W}^{-1}$ for the ETSoI device with an LCCO BOX layer. Therefore, the temperature of an ETSoI device with an LCCO BOX layer is increasing significantly slower than the temperature of an ETSoI device with a SiO_2 BOX layer.

Figure 2.13 shows the temperature gradient and the isothermal lines along the cross-plane direction, $\nabla T = \frac{\partial T}{\partial y}\left(\frac{K}{m}\right)$, at the hot-spot alone. It is shown that in the case of the ETSoI device with SiO_2 BOX layer, the heat is trapped at the BOX layer and is conducted uniformly to all directions, because of the isotropic thermal conductivity of the SiO_2. In the ETSoI device with LCCO BOX layer, the heat is accumulated at the hotspot and is conducted vertically to the substrate, because of the highly anisotropic thermal conductivity of LCCO. The highest temperature gradient value in the ETSoI device with LCCO BOX layer is one order of magnitude less than that with SiO_2 BOX layer (Figure 2.13 b).

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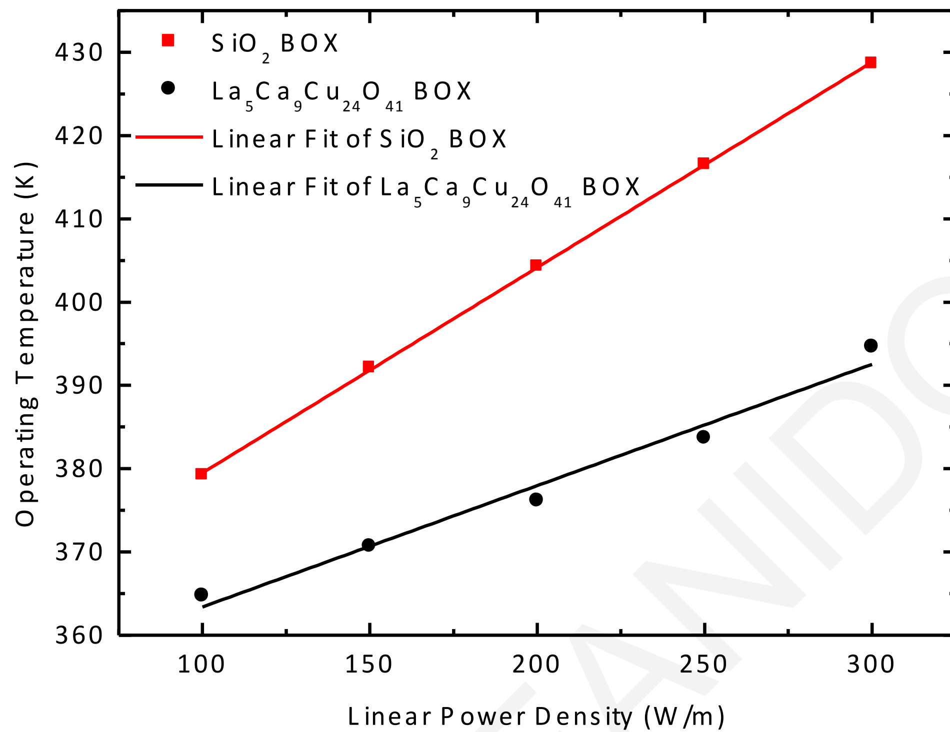

Figure 2.12 *Maximum operating temperatures obtained from an ETSOI device with a* SiO_2 *BOX layer (red square dots) and an ETSOI device with an LCCO BOX layer (black circular dots) while the linear power density of the hot-spot is increasing gradually from 100 W/m to 300 W/m. The lines are linear fittings.*

Figure 2.14 shows the heat distribution in an ETSoI device with a hot-spot, 150-nm BOX layer, and 1-µm spacing between transistors. When the BOX layer is SiO_2, the substrate temperature remains low, however, the transistors reach higher operational temperatures as the heat is trapped in the BOX layer and is distributed mainly in the BOX layer and thin Si layer (where the transistors are located). On the contrary, when the BOX layer is LCCO, the heat is distributed vertically and directly to the substrate and the heat sink, and as a result, the operational temperatures of the transistors are much lower.

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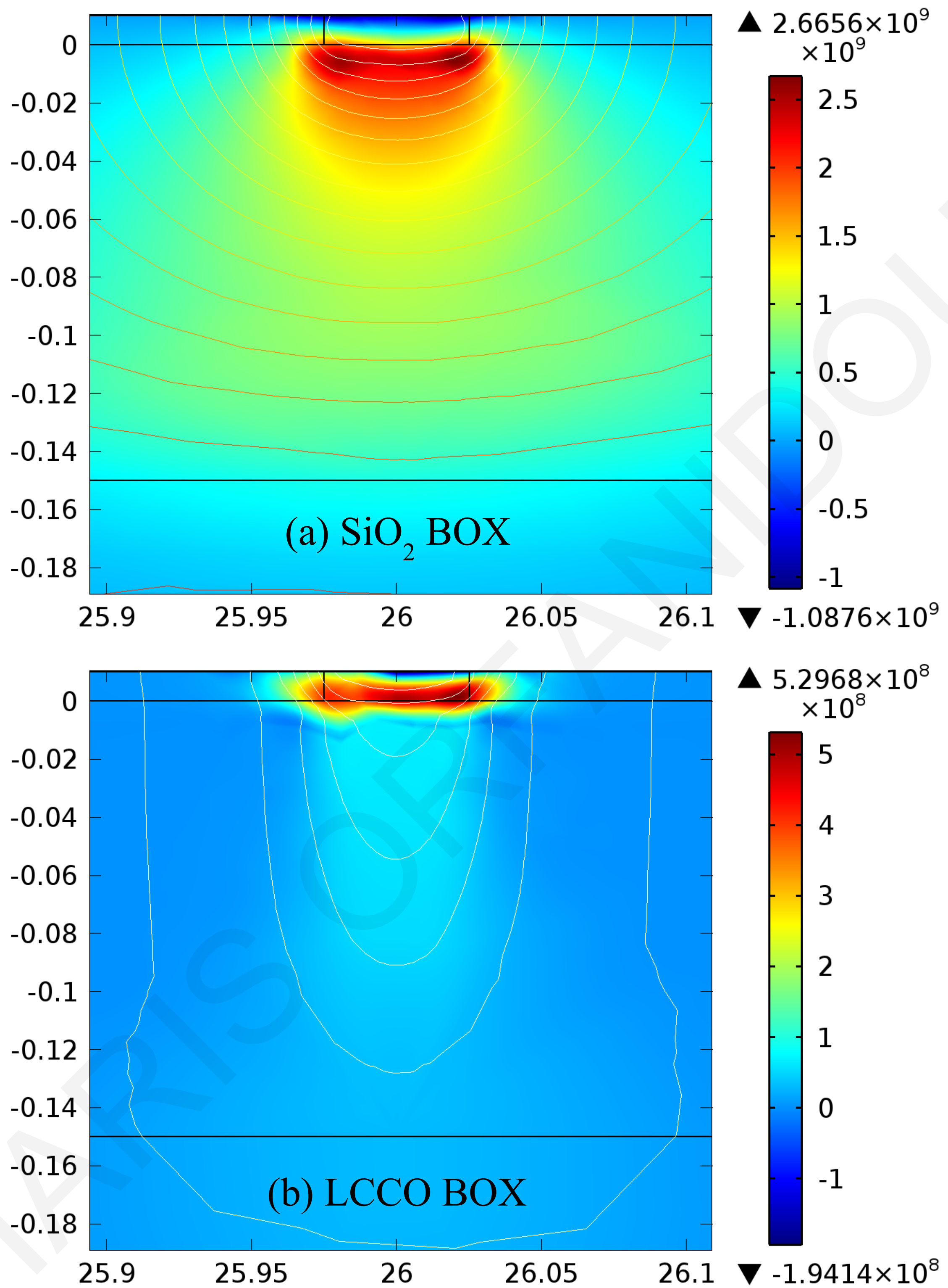

Figure 2.13 *Temperature gradient and isothermal lines along the cross-plane direction plotted for the ETSoI device with a 150-nm BOX layer of (a) SiO_2 and (b) LCCO. Plots show only the hot-spot (fifth operating transistor). Temperature gradient is given in kelvin/meter and dimensions in micrometers.*

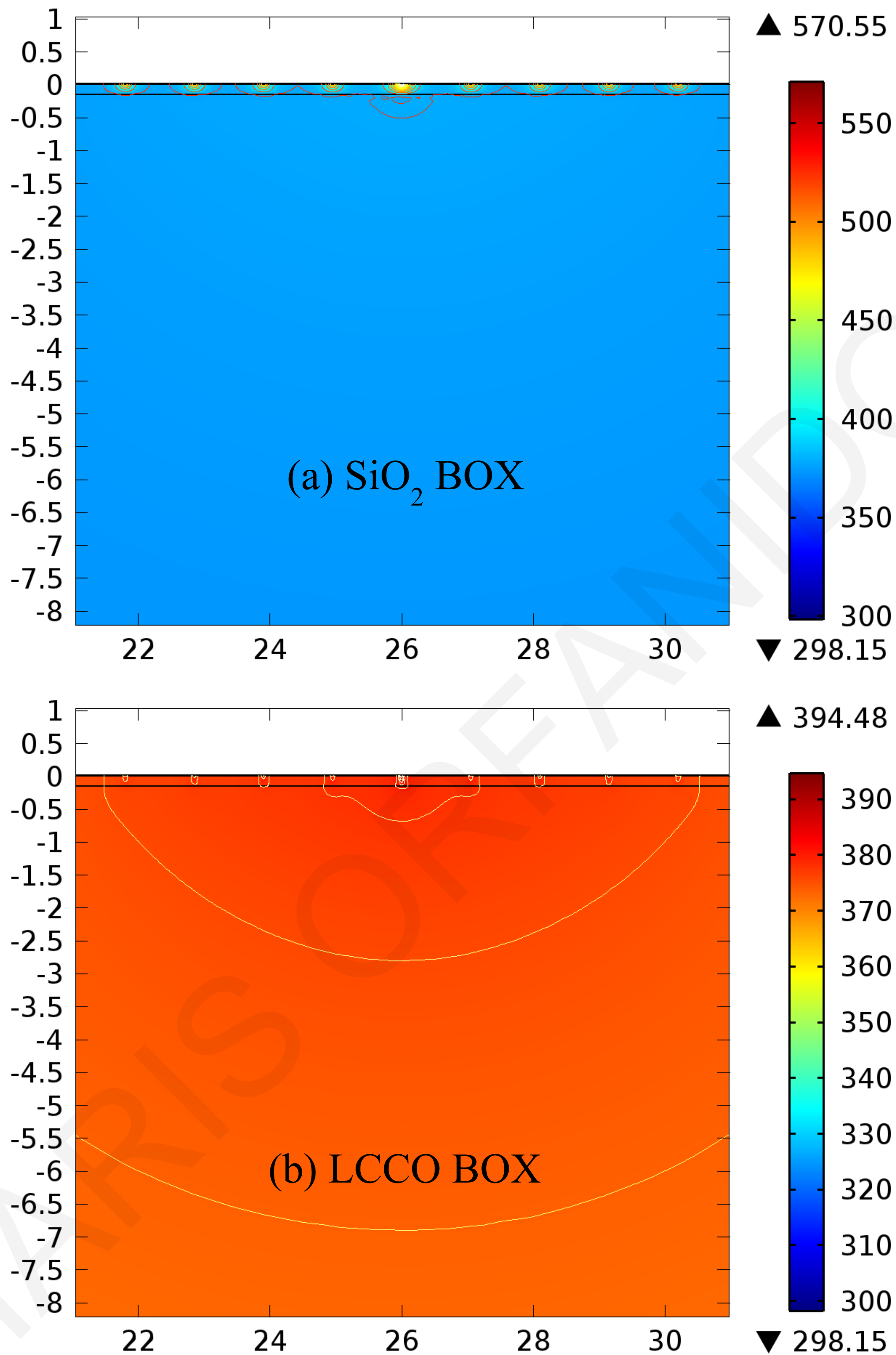

Figure 2.14 *Surface temperature and the isothermal lines plotted for the ETSoI device with a BOX layer of (a)* SiO_2 *and (b) LCCO. Plots show all the nine transistors in devices with hot-spot. For visualization reasons, we present data only for devices with 1-μm spacing between transistors and a BOX layer of 150 nm. Temperature is given in kelvin and dimensions in micrometers.*

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2.5.2 Further Analysis

Additional to the studies performed and in order to verify that the results shown above are optimized, further analysis has been done. Time dependent thermal analysis performed in order to clarify the timescale for the temperature increase and decrease in the active area. Additionally, grid sensitivity analysis (meshing), confirmed that our results are not affected by the grid size. Finally, the effects of the domain size, boundary conditions and heat sink temperature have been studied in order to test the impact on the demonstrated results.

2.5.2.1 Time dependent thermal analysis

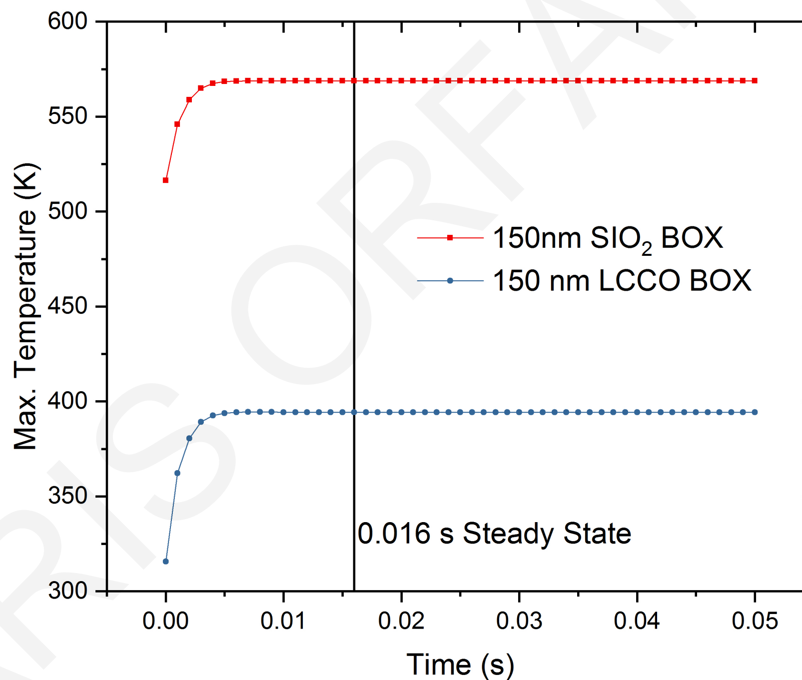

Figure 2.15 *Time dependence of the maximum temperature of the ETSoI device with a SiO_2 BOX layer (red) and with an LCCO BOX layer (blue). After a sharp increase of the temperature at the first 5 ms the steady state condition is finally obtained at 16 ms.*

The time dependent thermal analysis performed including the time derivative of temperature in the Fourier's heat transfer equation (Equation 2.5), and showed that for the thicker BOX layer studied (150 nm), either in the case that is SiO_2 or LCCO, 16 ms are needed in order to reach a steady-state condition. This is shown in Figure 2.15 for the

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maximum temperature of the ETSoI device at the hot-spot. Figure 2.16 shows the surface temperature of an ETSoI device with a hot-spot, 150-nm BOX layer of SiO_2 or LCCO, and 1-μm spacing between transistors, at 0 and 16 ms time.

BOX thickness (nm)	**SiO_2 steady state time (ms)**	**LCCO steady state time (ms)**
150	16	16
100	20	16
50	12	25
10	16	16

Table 2.2 *Time needed for steady state condition to occur at different BOX layer thicknesses of SiO_2 and LCCO.*

The steady state time needed for each different BOX layer studied for both SiO_2 and LCCO materials are shown in Table 2.2.

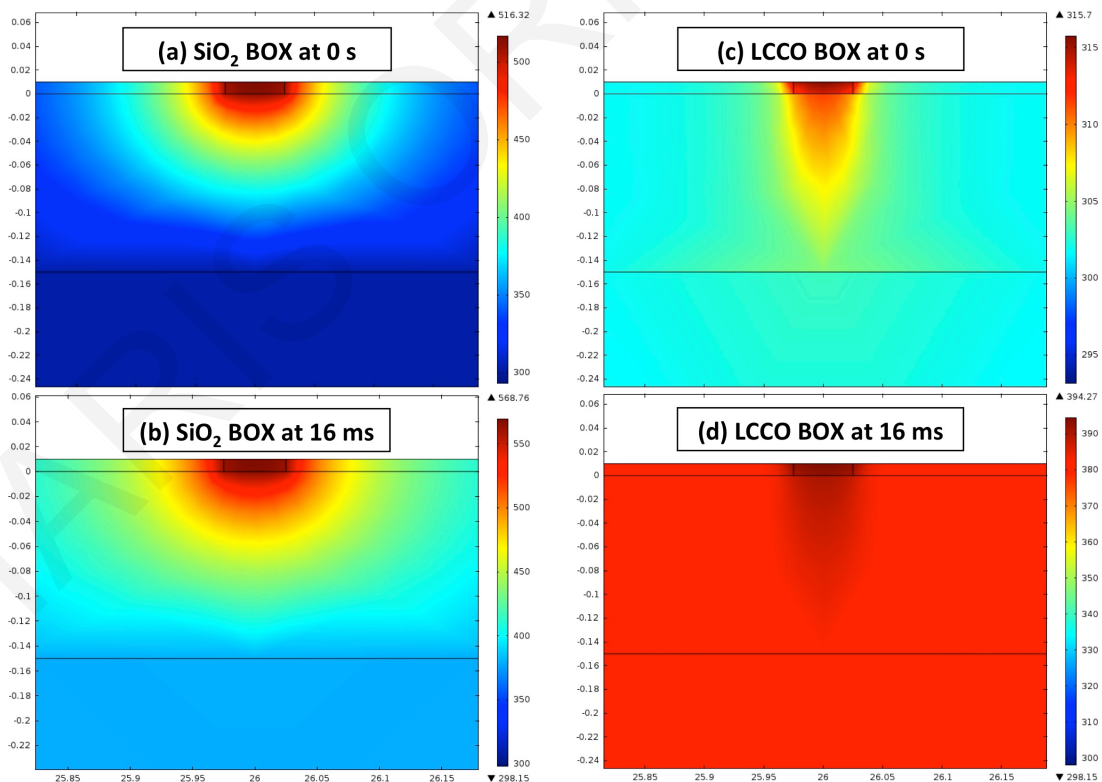

Figure 2.16 *Surface temperature plotted for the ETSoI device with a 150-nm BOX layer of (a), (b) SiO_2 and (c), (d) LCCO. Plots show only the temperature distribution at and around the hot-spot for time steps at 0 s ((a) and (c)), and 16 ms ((b) and (d)).*

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2.5.2.2 Grid sensitivity analysis

In order to verify that the results are not affected by the grid size of the specific ETSoI geometry (Figure 2.8), simulations were performed with different grid sizes that result in different number of triangular elements. Table 2.3 shows the maximum temperatures obtained at an ETSoI device with a hot-spot, 150-nm BOX layer, and 1-μm spacing between transistors, for both SiO_2 and LCCO BOX layers, as well as the temperature differences (ΔT_{max}) obtained by subtracting from the maximum operating temperature of an ETSoI device with a SiO_2 BOX layer, the maximum operating temperature of an ETSoI device with an LCCO BOX layer, for different number of triangular elements of the grid (mesh).

	Max. Temperature (K)		
Number of Elements	**SiO_2**	**LCCO**	**$\Delta T_{max} = T_{SiO2} - T_{LCCO}$ (K)**
184 481	568.7	394.54	174.16
94 661	568.82	394.56	174.26
81 358	568.83	394.47	174.36
73 688	568.78	394.26	174.52
73 672	568.78	394.26	174.52
61 899	568.63	393.51	175.12
55 486	568.56	393.46	175.1
33 789	568.68	393.8	174.88
24 389	567.73	392.53	175.2

Table 2.3 *Maximum temperatures of ETSoI devices with a 150-nm BOX layer of SiO_2 and LCCO, and temperature differences (ΔT_{max}) for different number of elements of the mesh.*

For simulation studies the meshing of the geometry is the most important step of the analysis in order to obtain high accuracy in the results. For a mesh that consists of triangular elements the triangles should be roughly the same size and should be as close to equilateral as possible. However, another very important parameter in simulations is the computation time that is closely dependent on the number of the elements of a mesh. Consequently, when choosing a mesh size and type someone needs to consider all the above-mentioned parameters.

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Mesh quality plots are shown in Figure 2.17. Figures 2.17 (a) and (c) show the meshing resulted the lower and higher number of triangular elements, respectively. Figure 2.17 (b) represents the mesh used for the simulations studies of heat channeling shown in 2.5.1 subsection of this chapter. From Table 2.3 we can come to the conclusion that the grid size and type selected is the optimum for this study.

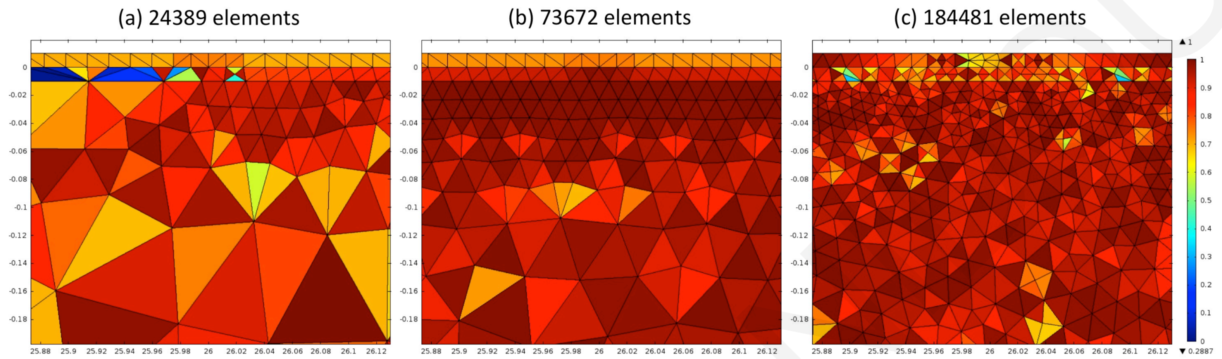

Figure 2.17 *Mesh quality plots for three different grid sizes: (a) extremely coarse, (b) fine, and (c) extremely fine meshes. A triangular element of high quality (equilateral) corresponds to value 1 (dark red color) and an element of very low quality – that deviates a lot from the triangle – corresponds to 0 (dark blue color).*

2.5.2.3 Effect of domain size

Simulation studies where the transistor population varied, were performed in order to test the effect of the domain size in the results obtained. Studies performed with 3, 5, 7, 9, and 11 operating transistors (for more than 11 transistors the computation time increases significantly). 9 operating transistors modeled for the studies shown in 2.5.1 subsection of this chapter. Figure 2.18 show that there is an increase of the maximum temperature in both ETSoI devices with 150-nm BOX layer of SiO_2 or LCCO, as the number of operating transistors is increasing. Nevertheless, the temperature differences (ΔT_{max}) obtained by subtracting from the maximum operating temperature of an ETSoI device with a SiO_2 BOX layer, the maximum operating temperature of an ETSoI device with an LCCO BOX layer, are decreasing with increasing number of operating transistors (Figure 2.19). The temperature differences though remain very high (above 160 K) for all different number of operating transistors studied.

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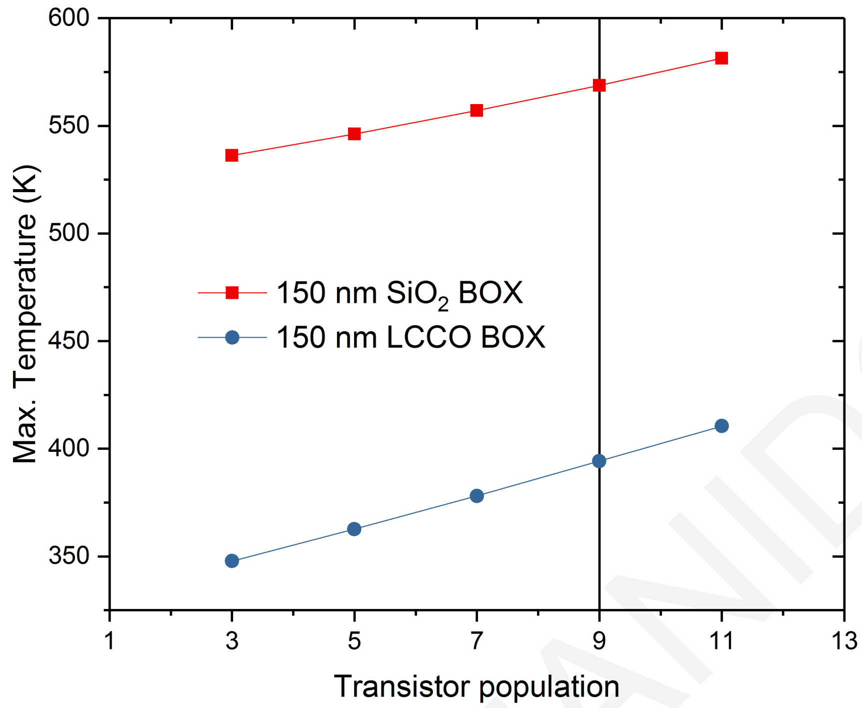

Figure 2.18 *Maximum temperature of the ETSoI device with a SiO_2 BOX layer (red) and with an LCCO BOX layer (blue) depending on the number of operating transistors.*

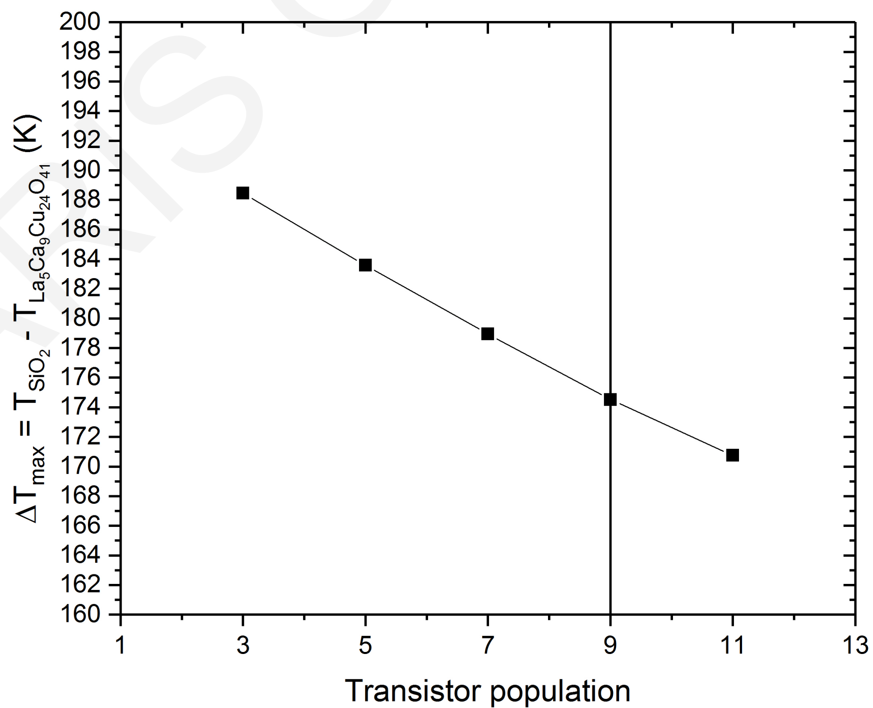

Figure 2.19 *Maximum temperature differences of the ETSoI device depending on the number of operating transistors.*

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2.5.2.4 Effect of boundary conditions and heat sink temperature

	Max. Temperature (K)		
Boundary Condition	**SiO_2**	**LCCO**	**$\Delta T_{max} = T_{SiO2} - T_{LCCO}$ (K)**
Adiabatic	568.78	394.26	174.52
Periodic & adiabatic	568.78	394.26	174.52
Convective cooling $h = 1 \frac{W}{m^2\,K}$	568.78	394.26	174.52
Convective cooling $h = 50 \frac{W}{m^2\,K}$	568.69	394.14	174.55
Convective cooling $h = 100 \frac{W}{m^2\,K}$	568.59	394.01	174.58
Periodic & convective cooling $h = 100 \frac{W}{m^2\,K}$	568.75	394.23	174.52

Table 2.4 *Maximum temperatures of ETSoI devices with a 150-nm BOX layer of SiO_2 and LCCO, and temperature differences (ΔT_{max}) for different boundary conditions.*

The external surfaces of the ETSoI device were modeled as adiabatic and a conventional heat sink is attached to the bottom of the device at a constant temperature $T = T_0 = 25°\text{C}$ (isothermal boundary condition), see 2.4.3.3 subsection of this chapter, and Figure 2.9. Simulation studies were performed varying the boundary conditions and the heat sink temperatures in order to test their impact. Table 2.4 demonstrates the maximum temperatures obtained at an ETSoI device with a hot-spot, 150-nm BOX layer, and 1-μm spacing between transistors, for both SiO_2 and LCCO BOX layers, as well as the temperature differences (ΔT_{max}) obtained by subtracting from the maximum operating temperature of an ETSoI device with a SiO_2 BOX layer, the maximum operating temperature of an ETSoI device with an LCCO BOX layer, for different boundary conditions of the external surfaces. In addition to the adiabatic boundary condition, simulation studies tested the cases where periodic condition was applied at the two lateral sides and adiabatic on top of the operating transistors, convective cooling with different heat transfer coefficients $h = 1\ or\ 50\ or\ 100 \frac{W}{m^2\,K}$, and finally periodic condition at the

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two lateral sides and convective cooling with $h = 100 \frac{W}{m^2\,K}$ on top of the operating transistors.

Different heat sink temperatures were applied $T = T_0 = 20\ or\ 25\ or\ 40\ or\ 60\ ℃$ and the results show an increase of the maximum temperature in both ETSoI devices with 150-nm BOX layer of SiO_2 or LCCO, as the temperature is increasing (Figure 2.20). Figure 2.21 shows that the temperature differences (ΔT_{max}) obtained by subtracting from the maximum operating temperature of an ETSoI device with a SiO_2 BOX layer, the maximum operating temperature of an ETSoI device with an LCCO BOX layer, are decreasing with increasing heat sink temperatures. However, the temperature differences remain very high (above 160 K).

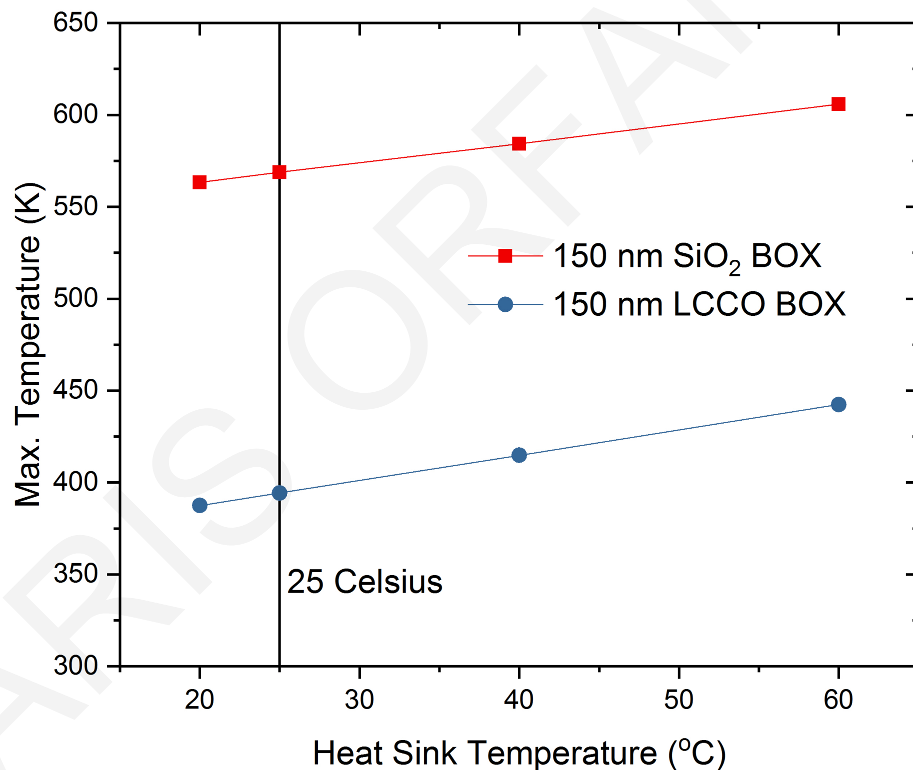

Figure 2.20 *Maximum temperature of the ETSoI device with a SiO_2 BOX layer (red) and with an LCCO BOX layer (blue) depending on the heat sink temperature.*

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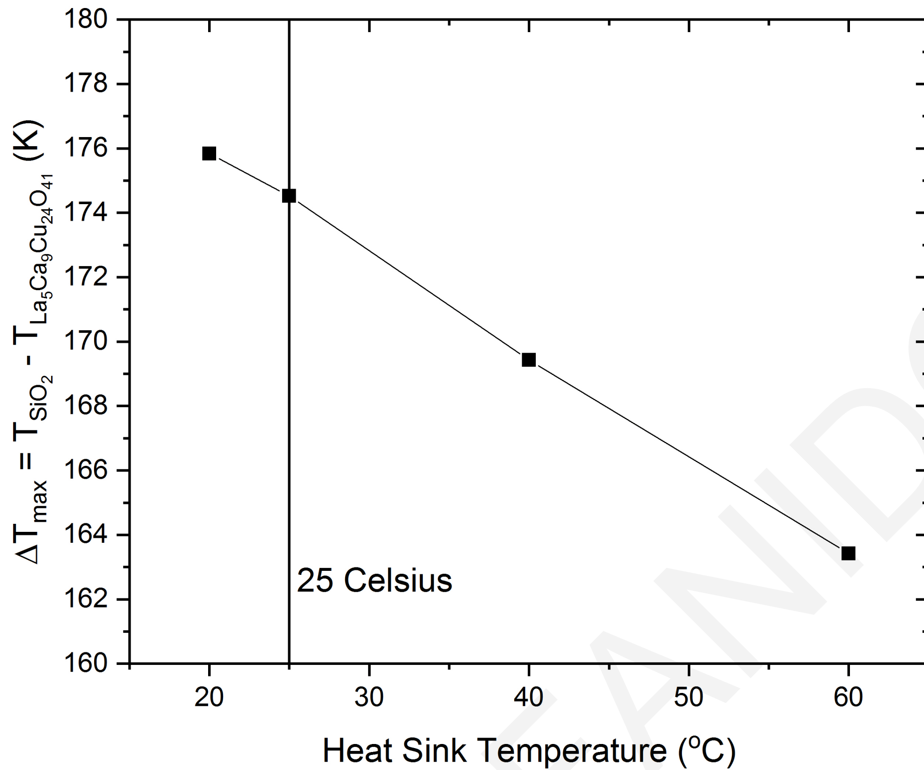

Figure 2.21 *Maximum temperature differences of the ETSoI devices depending on the heat sink temperature.*

2.6 Conclusion

Incorporating an LCCO BOX layer in ETSoI devices leads to a reduction of the maximum operating temperature of the transistors. The highly anisotropic thermal conductivity of LCCO results in a much lower operating temperature of the adjacent hot-spot operating transistors and thus could protect them from the exceeding heat generated at the hot-spot region of the chip. The efficiency of the hot-spot heat removal with an LCCO BOX layer depends on the specifics of the device structure. It was also noticed that when the linear power density is being gradually increased at a transistor, the temperature increases at a lower rate when LCCO BOX is being used, which shows that the heat channeling effect is more pronounced when a hot-spot is created. For today's ever-decreasing semiconductor feature sizes, an effective thermal management solution is needed and the simulation studies herein provide encouraging results for future semiconductor devices. The developed models and obtained results could be important for the design of heat-channeling-based thermal solutions using LCCO heat conductors.

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The exploitation of LCCO in thermal management applications, as the one discussed in this thesis, requires the growth of high-quality *c*-axis-oriented epitaxial LCCO thin films on technologically useful substrates such as Si. However, this has proven to be rather challenging because of the structural complexity of the investigated compound (316 atoms/unit cell accompanied by incommensurability along the *c*-axis) (Svoukis 2012, Pervolaraki 2012, Pervolaraki 2010, Pervolaraki 2009, Athanasopoulos 2011, Athanasopoulos 2010).

As P. Ball discusses in his featured paper in Nature (Ball 2012), scientists believe that the thermal management problem could find a solution if the architecture of CMOS devices will change. It is mentioned that in a computer machine, 96% of its volume is used to carry away the heat, whereas in contrast, the human brain is using only 10% of its volume for heat transport. Consequently, it is contemplated by scientists that the fabrication of neuromorphic, brain-like device structures will have a big impact on computers' output temperatures.

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Chapter 3

Resistive Switching Applications & State of the Art

3.1 Introduction

This chapter introduces to the topic of resistive switching (RS) phenomena. Initially the roadmap of non-volatile memories is discussed as well as the background theory of RS phenomena and the electrochemical processes involved.

Li_xCoO_2 material structure and electrical properties are also presented. Research already published on RS phenomena in Li_xCoO_2-based memory cells are discussed subsequently.

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3.2 Non-Volatile Memories

Since the 1960s, high-density storage started to develop using stages of square crossbar switches in an array form, with each stage having *N* inlets and *N* outlets (Beneš 1964). Random Access Memory (RAM) is typically used for data storage; while Read-only Memory (ROM) is used for firmware or application software storage in plug-in cartridges.

RAM memories, can be divided into two categories: volatile and non-volatile. Volatile RAM memories must be refreshed every split second and they lose their data quickly after power is removed. Static RAM (SRAM) and Dynamic RAM (DRAM) are volatile memories. DRAM allows for higher density storage compared to SRAM, but SRAM allows faster access (Nanoelectronics 2012).

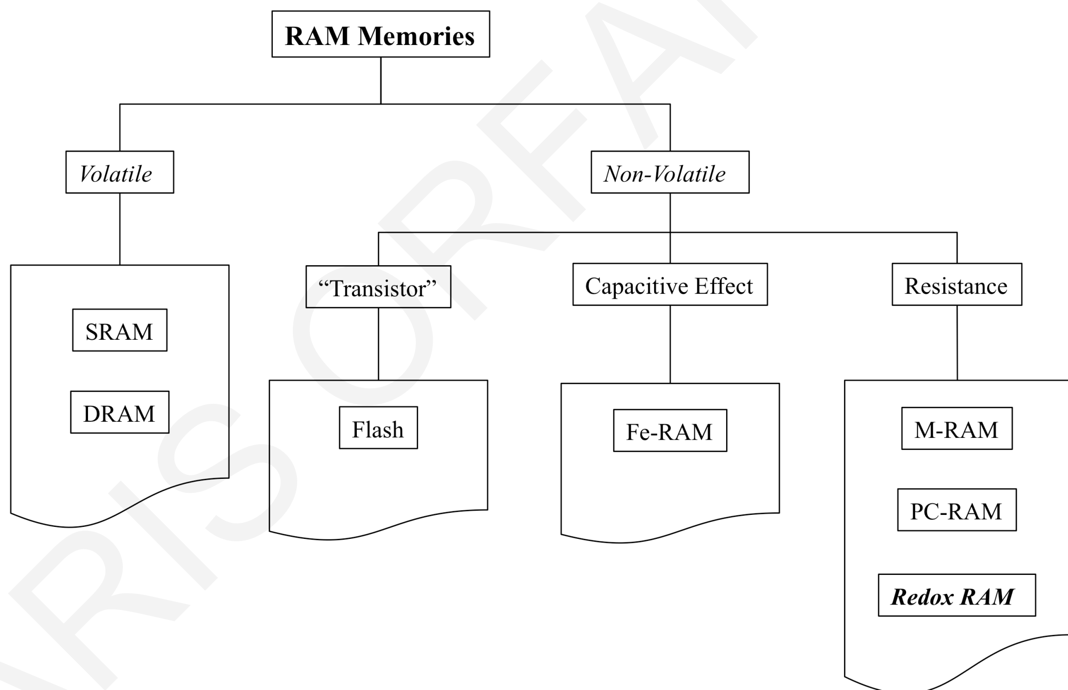

Figure 3.1 *Simplified diagram of RAM memories (Nanoelectronics 2012).*

Non-volatile memory (NVM) has the advantage to retain information for a long period of time (10 years or more) after power is removed. Different types of NVM memories have been developed, as shown in the flow diagram below (Figure 3.1). Examples include flash memory (Flash RAM), and Ferroelectric memory (Fe-RAM). Memories that rely on the resistive state of the materials are classified as Resistive RAM (RRAM or Re-RAM). This category includes magnetic memory (M-RAM), phase change memory (PC-RAM), and especially memories whose resistance depends on redox

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reactions (Redox RAM). However, this list is not complete and is only an overview of the many types of memories that research is currently addressing (Ielmini 2016, Kent 2015, Yang 2013, Wong 2012, Akinaga 2010, Burr 2010, Raoux 2010, Chappert 2007, Waser 2007, Wuttig 2007).

In terms of performance, and in order to move on from “lab” to “fab” manufacturing, the four most important parameters to consider are:

1) write/read speed;
2) endurance (write/erase cycles);
3) density and scalability (minimum feature size);
4) Write/read Voltages.

3.2.1 Flash memory

The general operating principle of flash memories is shown in Figure 3.2. For the read operation of information (0 or 1), the drain-source current depends on the presence (or lack) of electrons in an isolated area, called floating gate. If the electrons are stored in the grid, the current will be lower. The write operation is the transfer of electrons to the grid (or vice versa) via an applied voltage (higher) on the control gate (V_{CG}), relative to V_{BULK}.

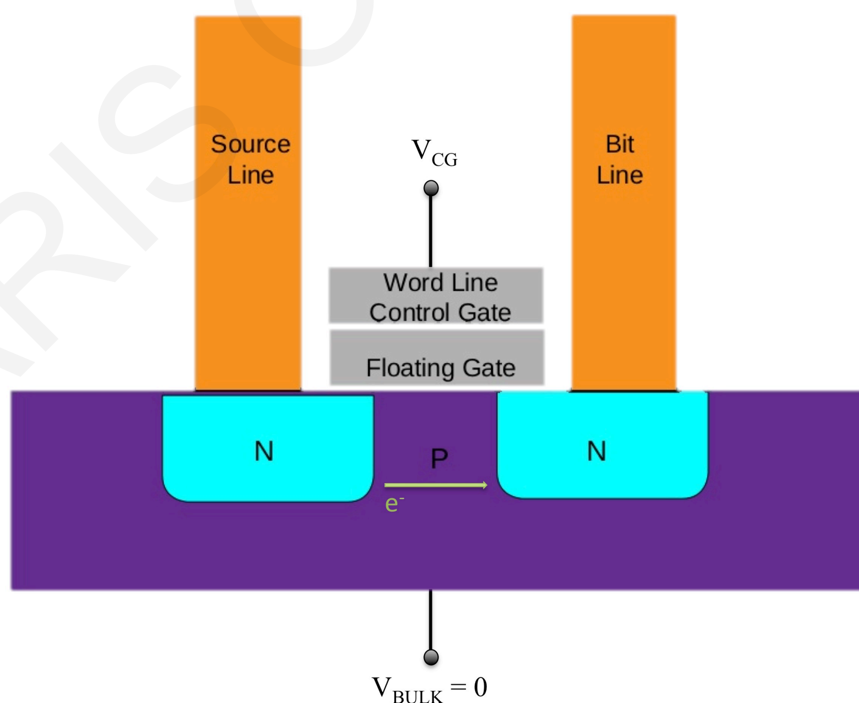

Figure 3.2 *Simplified diagram showing the operation of Flash memory (Cyferz Oct-2016).*

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Flash memories, which appeared in 1987 (Masuoka 1987), are very well-suited for many applications; including the best-known USB data storage. In terms of performance, the write speed is of the order of 100 microseconds, endurance lying in the interval of 10^4-10^5 cycles. The current size of the cells is of the order of 90 nm. Researchers reached the size of 20 nm but the same time endurance has degraded (Xu 2011, Bez 2003). Storage in three dimensions is also currently studied (Technology 2014 & 2015).

The write speed and density are the main limitations of Flash memories (Ielmini 2009a, Kim 2004). To overcome these limitations, several other types of non-volatile memories are being investigated, such as Fe-RAM, M-RAM and PC-RAM that are discussed briefly below.

3.2.2 Fe-RAM memory

A simplified diagram of the operating principle of a Fe-RAM memory is shown in Figure 3.3. Fe-RAM memories allow permanent storage of information that is based on the use of ferroelectric materials, whose spontaneous polarization can be reversed by applying an electric field. In 2011, Texas Instruments introduced the first microcontroller Fe-RAM memory (Zwerg 2011).

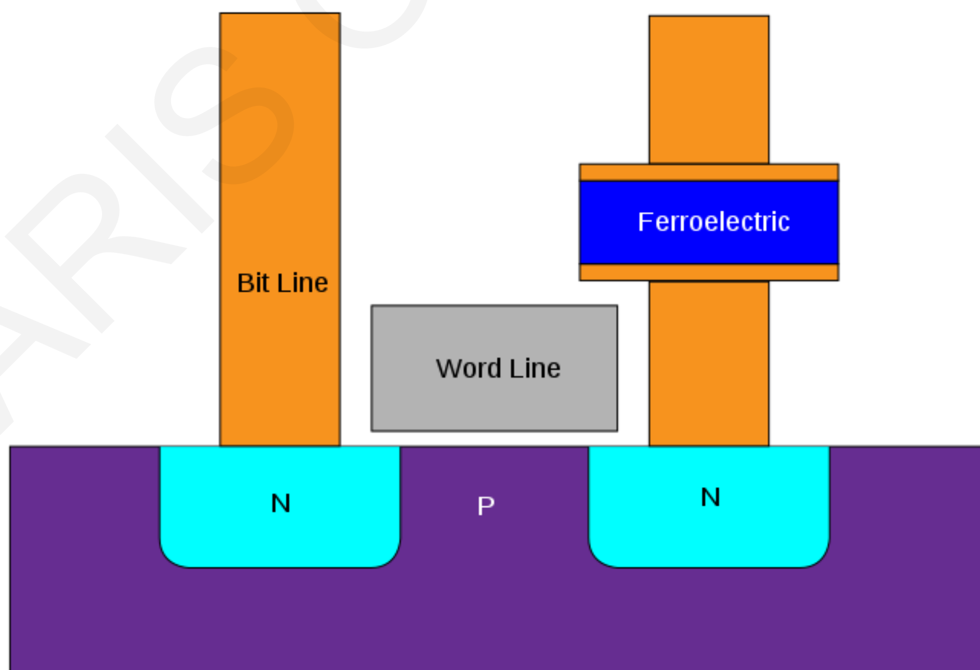

Figure 3.3 *Structure of a Fe-RAM cell (Cyferz Aug-2016).*

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These memories are characterized by a high writing speed (10 ns), and a very good endurance (> 10^{12} cycles). The main limitations concern the density (current minimum size of about 130 nm). Indeed, ferroelectric materials lose their properties when the dimensions are very small (Junquera 2003).

3.2.3 M-RAM memory

Tunnel magnetoresistance (TMR) phenomena were discovered at room temperature back in 1995 (Moodera 1995). The principle is based on the use of two layers of ferromagnetic material separated by a thin insulating barrier (1-2 nm) (Figure 3.4). The direction of magnetization of one of the layers is variable; the magnetization of the other remaines fixed. When the magnetizations are in parallel orientation it is more likely that electrons will tunnel through the insulating film,. Tunneling is less likely though when they are opposingly oriented (antiparallel). A simplified M-RAM cell is presented in Figure 3.4.

M-RAM is characterized by a high writing speed (10 ns), and a very good endurance (> 10^{12} cycles). The main limitations concern the high current density (and therefore energy) required to achieve the ferromagnetic switching (Ha 2011) and the device density that currently cannot be reduced very easily because of the complex structure of the magnetic free layer that is difficult to control (Fujisaki 2010).

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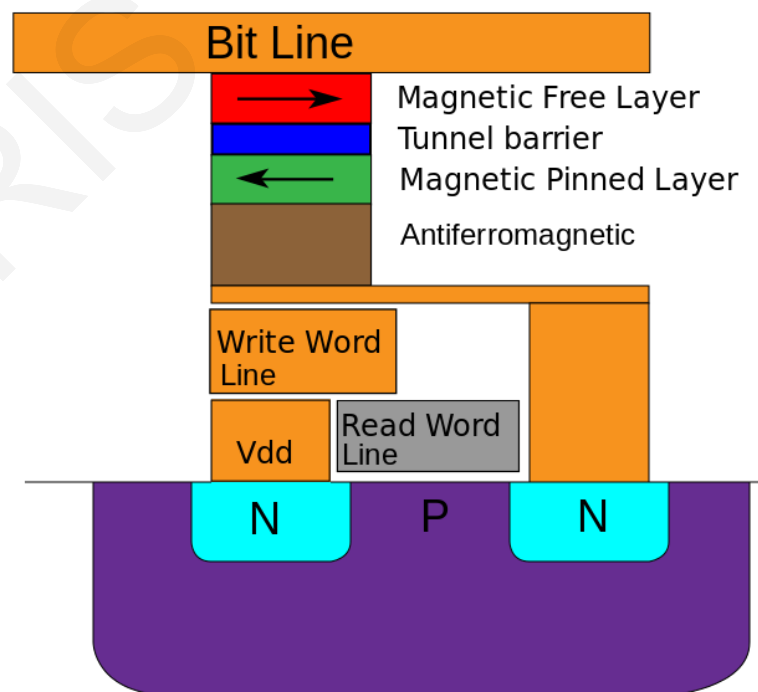

Figure 3.4 *Simplified diagram showing the structure of a M-RAM memory (Cyferz Sep-2016a).*

3.2.4 PC-RAM memory

The principle is based on materials having a different electrical conductivity, according to whether they are in an amorphous (high resistance) or in a crystalline (low resistance) phase. This type of information storage was first introduced in the late 1960s (Ovshinsky 1968). PC-RAM memories exploit the unique behavior of chalcogenide glass (S, Sb, Te). $Ge_2Sb_2Te_5$ (GST) has been extensively studied for use in PC-RAM memories (Simpson 2010, Ielmini 2009b, Ielmini 2009c, Lavizzari 2009, Ielmini 2007). A diagram of a PC-RAM memory cell is shown in Figure 3.5.

The fast atomic rearrangements in phase-change materials, combined with the large resistivity contrast between amorphous and crystalline phases in this material class, can be used to store information for several years (Pirovano 2004), with access times of a few nanoseconds (Bruns 2009). Additionally, high-scalability (dimensions as low as 3 nm × 20 nm) has been shown (Raoux 2008). Disadvantages include a fairly high current (so a significant amount of energy) that is required (up to 100 uA) for switching (Fujisaki 2010). Currently, research is looking to reduce this weakness.

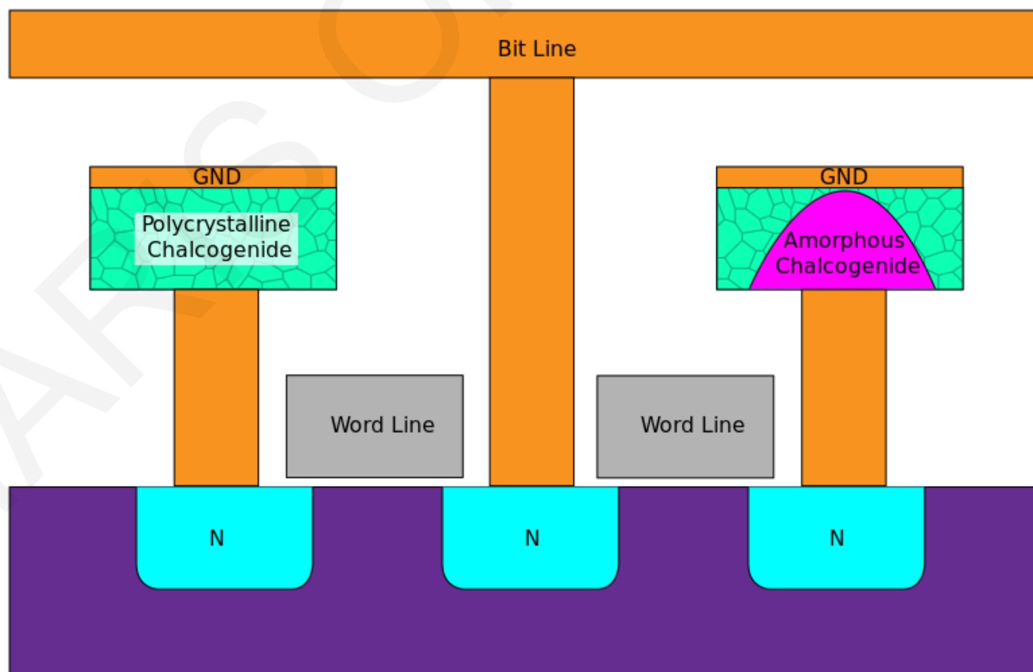

Figure 3.5 *A cross-section of two PC-RAM memory cells. One cell is in low resistance crystalline state, the other in high resistance amorphous state (Cyferz Sep-2016b).*

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3.3 Resistive Switching Phenomena

3.3.1 Resistive-RAM memory (RRAM)

As a part of this thesis, the subject of resistive switching (RS) phenomena with a major application in Resistive RAM (RRAM) memories will be discussed more extensively in this section.

A RRAM memory cell is generally built by a capacitor-like MIM structure (Metal / Insulator / Metal), where I is an electronic/ionic mixed conduction material, which is much less conductive than the electrodes (M). Such an array of RRAM memory cells is shown in Figure 3.6.

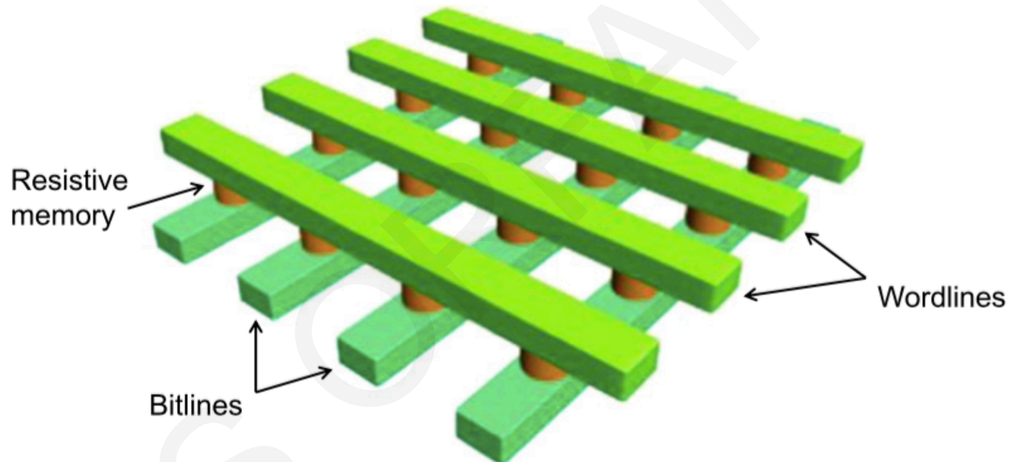

Figure 3.6 *Schematic showing crossbar array architecture where wordlines (rows) and bitlines (columns) stand for M, and resistive memory stands for I of an MIM memory cell (Ielmini 2016, Jo 2009).*

The read operation is performed by applying a voltage ($\leq$ 1V) lower than the voltage values used for the write operation (that change the state of the resistance of the insulator, I).

Advantages of RRAM memories can be listed as: 1) high density, 2) relatively low manufacturing cost even compared to the available Flash technologies, 3) relatively acceptable endurance compared to predictions for 16 nm Flash technology, 4) architectural flexibility by using a simple and flexible crossbar array, 5) a variety of materials with RS behavior can be used, and finally 6) significant potential in implementing learning algorithms and neuromorphic engineering (Kavehei 2011).

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In summary, RRAM compared to Flash memory requires lower voltage so it can be used in low-power applications, compared to M-RAM has a smaller and simpler cell structure, while compared to PC-RAM operates at faster timescale (switching time can be less than 10 ns). Therefore, it seems to be a promising type of NVM that merits further investigation.

3.3.2 Electrical polarization schemes for RS memory cells

The electrical resistance of an MIM cell can be switched between at least two values: OFF (high resistance) and ON (low resistance). To classify the different types of RRAM, a distinction is often made between two systems, called "unipolar switching" and "bipolar switching" (Waser 2007). The RS is called unipolar when the transition from one state to another (OFF → ON or ON → OFF) does not depend on the polarity of the write voltage signal, as shown in Figure 3.7a. Switching is called bipolar when the OFF → ON transition and the ON → OFF occur for a different polarity of the voltage (Figure 3.7b).

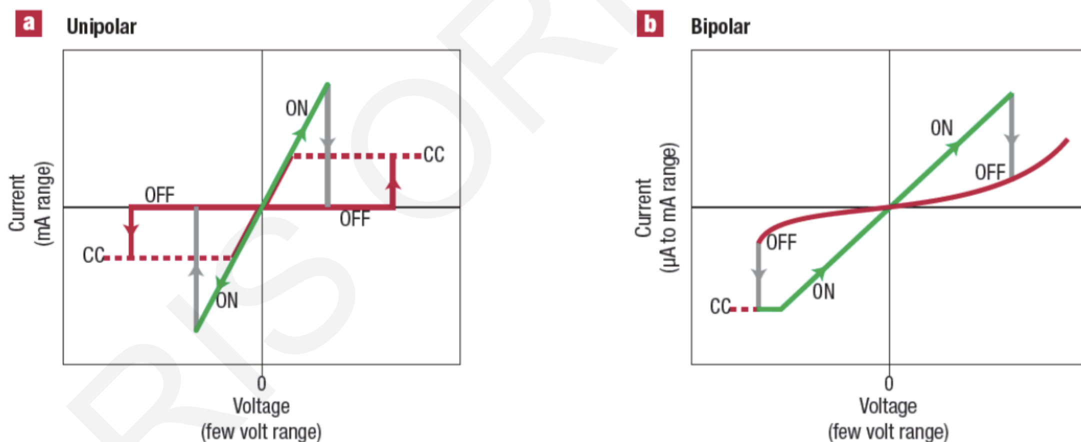

Figure 3.7 *Diagrams showing (a) Unipolar RS, and (b) Bipolar RS, according to (Waser 2007).*

3.3.3 Electrochemical processes

In a redox-reaction process, there is always an oxidation reaction in which a chemical element (an atom or a molecule) loses one or more electrons (a valence electron) in favor of another chemical element, which will gain one or more electrons through a reduction reaction. Oxidation and reduction are inseparable, an oxidation cannot occur without a reduction (and vice versa).

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The diagram in Figure 3.8 gives an overview of all possible redox-reaction processes, which may be involved in the electrochemical RS (Waser 2011). The metal electrodes M´ and M´´ transfer the electric current, I, while the intermediate resistive material (MX), can transfer electronic and ionic currents. The ionic current can be formed by an anion X^-, moving to the left electrode with positive polarization, and the M^+ cations are then moving toward the right electrode that is biased negatively. Additionally, M'^+ ions can possibly come from the anode metal M´. The relative contributions depend strongly on the type of RRAM cells and conditions. The Joule heating generally occurs within the MX layer and/or close to the contact.

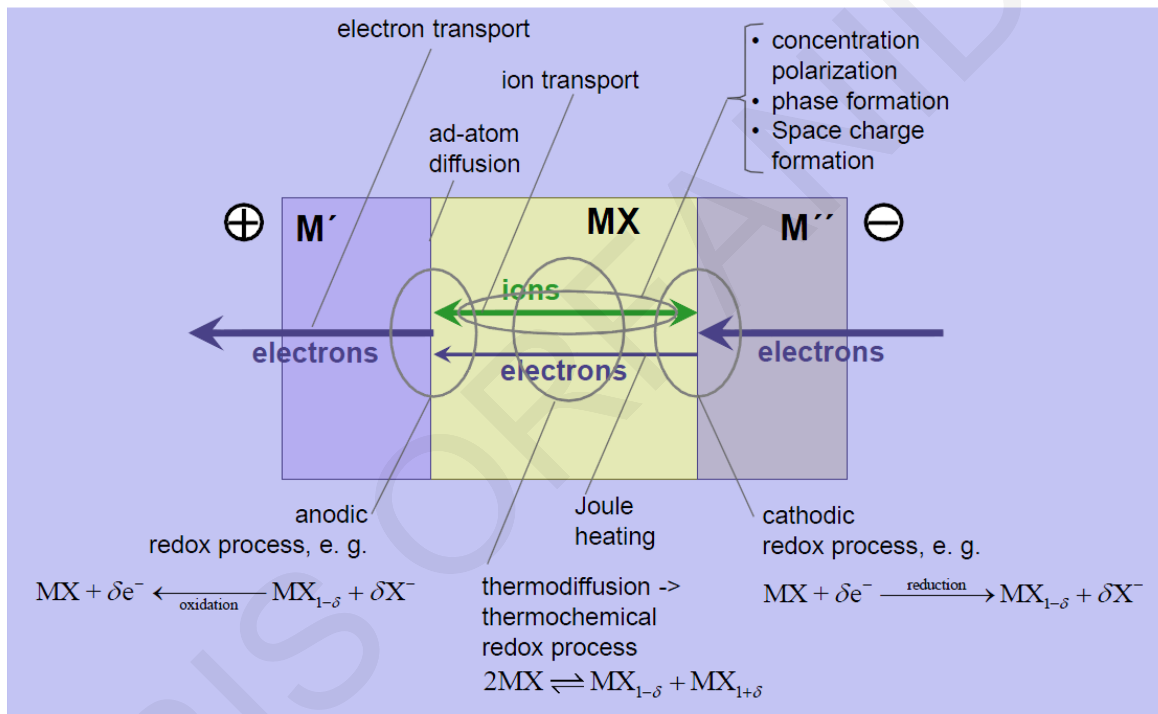

Figure 3.8 *Conceivable redox-reaction processes during RS (Waser 2011).*

The ion current in the MX material leads to electrochemical reactions (oxidation and reduction of the RRAM cell). In addition, the ionic current can, at least partially, be blocked at the interfaces with the electrodes, M. This leads to the so-called concentration polarization that is the accumulation of mobile ions near an electrode and the near depletion of the other.

Other processes that may occur involve phase formation, and also space change formation where, excess electric charge is treated as a continuum of charge distributed over MX space. Additionally, ad-atom diffusion may occur by the motion of ad-atoms at the MX/M´ interface, and thermodiffusion that results into a thermochemical redox process.

3.3.4 Classification of the electrochemical mechanisms involved in RS phenomena

Although it is still a difficult task to identify the mechanism governing RS phenomena in RS memory cells, it has been the subject of considerable effort from research groups to classify mechanisms of different MIM device structures (Waser 2011, Akinaga 2010, Waser 2009, Waser 2007, Sawa 2008).

R. Waser *et al.* (Waser 2009) classified several types of mechanisms based on the resistive switching effects (Figure 3.9). In the following sections, the three mechanisms that are redox-related are discussed more extensively: 1) electrochemical metallization mechanisms (ECM), 2) valence change mechanisms (VCM) and 3) thermochemical mechanisms (TCM).

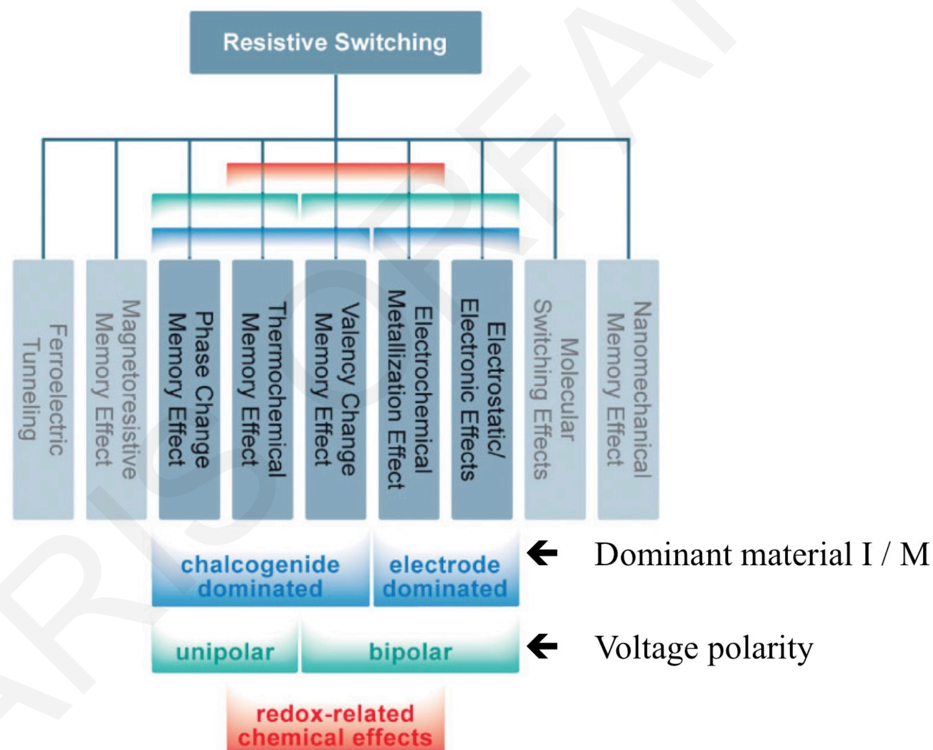

Figure 3.9 *Classification of the resistive switching effects that are considered for non-volatile memory applications. Switching mechanisms based on thermal, chemical, and electronic/electrostatic effects (Waser 2009).*

3.3.4.1 Electrochemical Metallization Memory (ECM)

This type of mechanism is based on the existence of an active metal electrode (AE, typically made of Ag, Cu, or Ni), and a chemically inert electrode (counter electrode, CE,

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such as Pt, Ir, Au, W). The film is placed between these two electrodes either as an insulator doped with ions of the AE, or a solid electrolyte containing ions of the active electrode AE (Waser 2009).

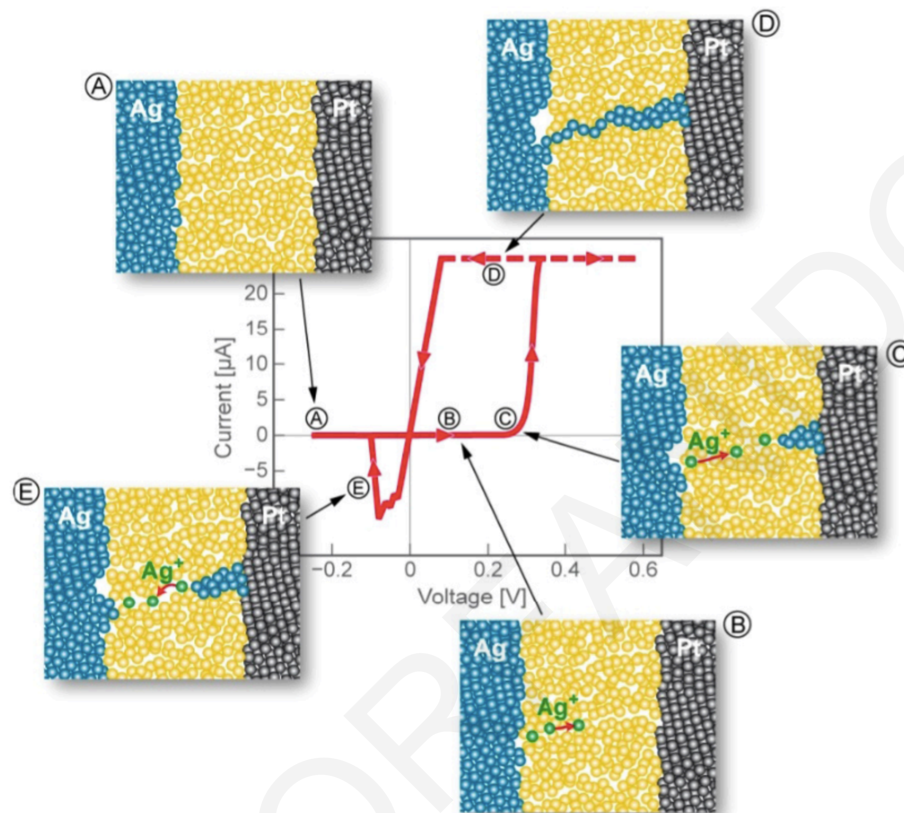

Figure 3.10 *Schematic showing an-inside of the electrochemical reactions that take place in an ECM during a complete cycle. (A) to (D) show the SET process ($Ag \rightarrow Ag^{+} + e^{-}$) and (E) the RESET process (Valov 2011).*

At a preliminary stage of activation, that is called electroforming, when a sufficient positive voltage is applied to the positive electrode (AE), anodic oxidation starts and there is dissolution of the metal M – oxidation – (Figure 3.10 B). M^{+} cations migrate to the CE, and are reduced to the metallic state – growth of filaments – (Figure 3.10 C) and migrate towards the AE. When the filaments touch the active electrode (Figure 3.10 D), a transition from OFF (HRS) to ON (LRS) (SET process) occurs. By reversing the voltage polarity, partial dissolution of the conducting filament occurs where the system turns back to the initial HRS (RESET process) – reduction – (Figure 3.10 E) (Waser 2009, Valov 2011, Valov 2012).

$$M^{z+} + ze^{-} \leftrightarrows M \tag{3.1}$$

This mechanism appears to be clearly of a bipolar type.

3.3.4.2 Valence Change Memory (VCM)

In VCM effect the metal electrodes do not inject ions into the film placed between the electrodes, as was the case for the ECM. VCM mechanisms include many possible ones, filamentary, homogeneous or intermediates. The materials involved are transition metal oxides with the metals having at least two different oxidation states. Some of the wide variety of ionic/electronic mechanisms reported in the literature in (Waser 2009) are:

- The injection of charges in the insulating film, which causes a change in the electrostatic barrier (Ouyang 2004);
- Changing the interface metal electrode/semiconductor film, which locally affects the Schottky barrier (that meets the homogeneous mechanism proposed by A. Sawa (Sawa 2008);
- A purely electronic mechanism type transition metal/insulator in strongly correlated electron systems (Rozenberg 2004);
- A tunnel junction, of which the resistance depends on the polarization (parallel/antiparallel) of a ferroelectric material (Esaki 1971).

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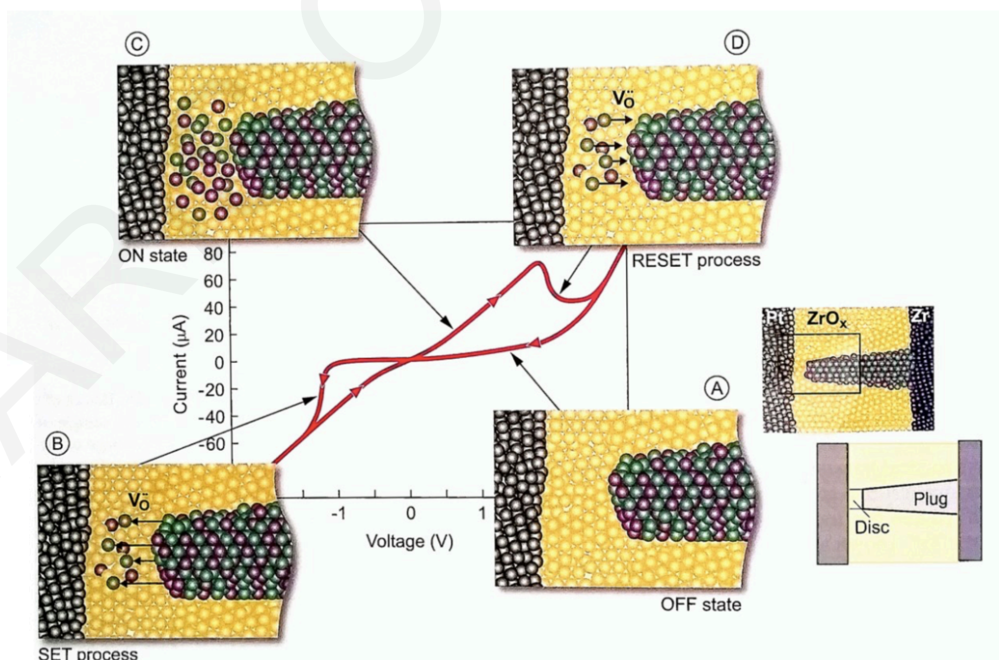

Figure 3.11 *Current-voltage (I-V) plot of a Pt/ZrO_x/Zr VCM cell. Pt acts as the active electrode, while Zr is the ohmic electrode. The insets show the different stages of the RS process. (A) OFF (HRS) state; (B) SET process; (C) ON (LRS) state; (D) RESET process. (Nanoelectronics 2012).*

Apart from this, it was observed that in a large number of transition metal oxides, the switching resistance involves the migration of oxygen vacancies. These migrations alter the oxidation state of the metal cations (which remain stationary), and therefore the local conductivity of the film. In particular, materials such as TiO_x, TaO_x, WO_x, HfO_x, $SrTiO_3$ refer to VCM (Nanoelectronics 2012). RS is of bipolar type, and an electroforming step is usually necessary. The structure includes an active electrode, for example Pt, Ir, TiN, electronic/ionic mixed conductor, and an ohmic electrode.

A typical I-V bipolar curve of a $Pt/ZrO_x/Zr$ VCM cell is shown in Figure 3.11. In the OFF state a filament appears that consists of conducting “plug” and a potential barrier that is called “disc”. When a voltage is applied to initialize the SET process (a negative voltage in this case), oxygen vacancies are attracted from the plug into the barrier. This results in a significant reduction of the disc’s space due to a local reduction reaction, and the cell switches to the ON state. Reversing the voltage bias repels the oxygen vacancies, leading to re-oxidation of the disc area, and the cell switches back to the OFF state (Nanoelectronics 2012).

3.3.4.3 Thermochemical memory (TCM)

In TCM the thermal effects are predominant with respect to the electrochemical processes. Thermochemical systems show unipolar characteristics. In a Pt/NiO/Pt TCM cell (Figure 3.12), an initial electroforming step results to the formation of a filament. Upon applying a current compliance (cc, compliance resistance) the cell is preserved at the ON state. After removal of the cc and application of a voltage at the Pt electrodes a kind of “breakdown” of the filament occurs locally, which causes significant heating (thermodiffusion, Equation 3.2). Thus, a RESET process takes place and the cell moves from HRS to LRS. For the SET process to occur a lower value cc is applied.

$$2NiO \leftrightharpoons NiO_{1-\delta} + NiO_{1+\delta} \qquad (3.2)$$

This mechanism is observed for all metal oxides (NiO, CuO, Al_2O_3,...). The electrodes are often made symmetrical. The type of Pt/NiO/Pt cells are among the most important that are being investigated because of their reliability and scaling prospects (Ielmini 2011).

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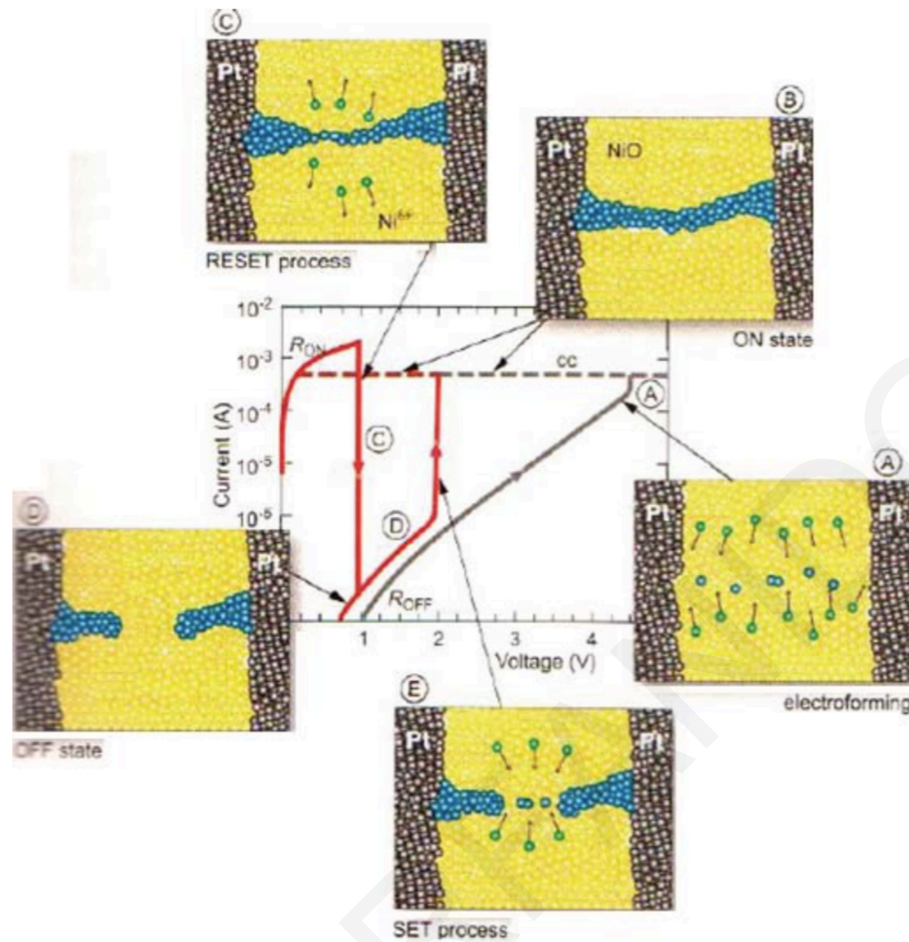

Figure 3.12 *Schematic showing an inside of the electrochemical reactions that take place in a Pt/NiO/Pt TCM memory. The process is of a unipolar type and it is shown in insets from (A) to (E) (Nanoelectronics 2012).*

3.4 Li_xCoO_2 material

3.4.1 Li_xCoO_2 crystal structure

Li_xCoO_2 has two crystal structures, HT- Li_xCoO_2 (High Temperature) and LT-Li_xCoO_2 (Low Temperature). HT-Li_xCoO_2 is often synthesized at high temperatures (600 °C) and has a layered structure that belongs to the space group ($R\bar{3}m$), which may be represented by a hexagonal symmetry. LT-Li_xCoO_2 is often synthesized at lower temperatures ($400 - 600$ °C), has cubic spinel symmetry and belongs to the space group $Fd3m$ (Rossen 1993, Antolini 2004). The differentiation of these two phases is, however, difficult by X-ray diffraction (XRD), because their XRD patterns are very similar (Kang 1999).

The structure of HT-Li_xCoO_2 can be represented by a hexagonal lattice with alternating planes of CoO_2 sheets and Li^+ ions (Shao-Horn 2003), as shown in Figure 3.13. The lattice parameters are $a_{hex} = b_{hex} = 2.8138$ Å and $c_{hex} = 14.0516$ Å. The CoO_2 sheets, wherein the Co-O bonds are strong, form a rigid structure.

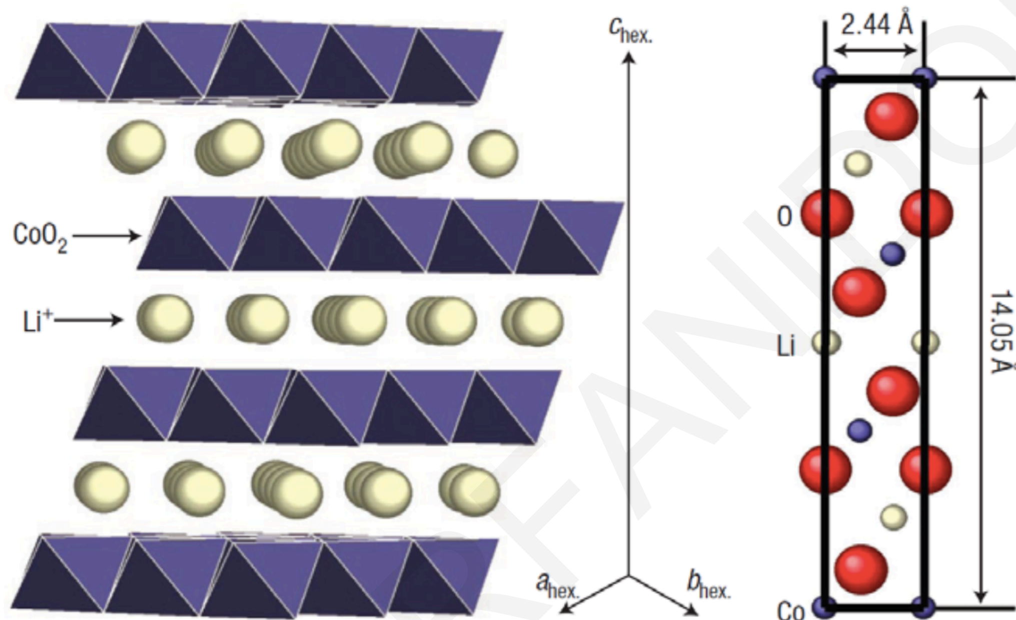

Figure 3.13 *HT- Li_xCoO_2 crystal structure (Shao-Horn 2003).*

In HT-Li_xCoO_2 with hexagonal symmetry, Li^+ ions can be extracted by electrochemical or chemical processes and result in a non-stoichiometric phase.

Different Li content (x) in Li_xCoO_2 leads to different phases. For Li content $\mathbf{0.94 \leq x \leq 1.0}$, Li_xCoO_2 exhibits the Hex-I phase and an insulating behavior. For Li content $\mathbf{0.75 \leq x \leq 0.94}$, the material exhibits both the Hex-I and Hex-II phases, and this is known as the biphasic domain. For Li content $\mathbf{0.5 \leq x \leq 0.75}$, Li_xCoO_2 exhibits the Hex-II phase and metallic behavior, whereas for Li content $\mathbf{x \leq 0.5}$ the structure is monoclinic and remains stable.

Experimental studies have shown that the biphasic domain of both Hex-I and Hex-II is formed not because of structural reasons but because of a metal-to-insulator (MIT) transition (Ménétrier 1999) that is characterized as a first order Mott transition (Marianetti 2004).

A relation of Li content, x, with the lattice parameters *a* and *c* of Li_xCoO_2 has been reported in the literature (Molenda 1989, Garcia 1997). For HT- Li_xCoO_2, J. Molenda *et al.*

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showed changes in lattice parameters *a,* and *c*. When x decreases from 1.00 to 0.80, the lattice parameter *a* rapidly decreases, and then remains constant. The lattice parameter *c* gradually increases for x ranging from 1.00 to 0.20. M. Ménétrier *et al.* have confirmed these results later, as shown in Table 3.1 from (Ménétrier 1999). The existence of two very similar phases (both hexagonal), for $\mathbf{0.75 \leq x \leq 0.93}$ has been demonstrated by J. N. Reimers *et al.* in 1993 (Reimers 1993).

x (of Li_xCoO_2)	$\boldsymbol{a}$(Å)	$\boldsymbol{c}$(Å)	$\boldsymbol{c/a}$
1.00	2.8155	14.049	4.99
0.98	2.815	14.051	4.99
0.94	2.813	14.056	4.99
0.75	2.810	14.193	5.05
0.70	2.811	14.196	5.05
0.60	2.810	14.287	5.08

Table 3.1 *Lattice parameters a, c and c/a ratio as a function of x in Li_xCoO_2 (Ménétrier 1999).*

3.4.2 Electrical properties of Li_xCoO_2

In 1980, Goodenough *et al.* demonstrated for the first time the ability of Li_xCoO_2 to reversibly de-intercalate lithium ions (Mizushima 1980). Due to this property, Li_xCoO_2 is used as a cathode material in Li-ion batteries. Later on, studies on the electrical properties of Li_xCoO_2 were carried out in order to improve cycling charge/discharge (Levasseur 2000, Ménétrier 1999, Wang 1996, Molenda 1989).

Figure 3.14 illustrates the abrupt change of resistivity, ρ, for lithium content between 0.50 and 1.00 that is over 5 orders of magnitude.

Surface resistance modifications of Li_xCoO_2 cells have reported for the first time back in 2011 by A. Moradpour *et al.* (Moradpour 2011). In that case, electrochemical reactions occur within the condensation water capillary meniscus at the probe/substrate contact.

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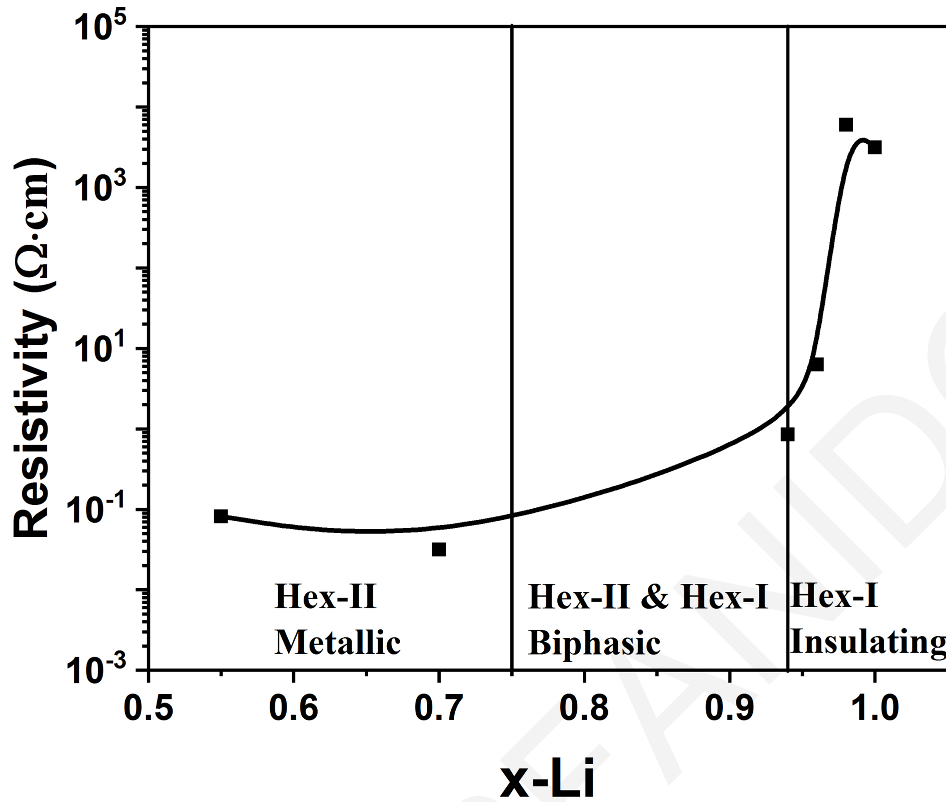

Figure 3.14 *Resistivity, ρ, as a function of Li stoichiometry at room temperature (Ménétrier 1999).*

3.5 Resistive Switching in Li_xCoO_2-based memory cells

In 2011 Moradpour *et al.* studied for the first time Li_xCoO_2 thin films in an MIM configuration and RS phenomena were observed. Figure 3.15 shows an I-V RS cycle obtained from the configuration as seen in the inset schematic (Moradpour 2011).

In 2015, Mai *et al.* studies of memristive characteristics show multilevel RS, which indicates possible neuromorphic circuit applications. Figure 3.16 shows four well-separated resistance states (Mai 2015).

The mechanism that governs RS phenomena of the Au/Li_xCoO_2/SiO_2/Si memory cell is first discussed in Mai *et al.* and suggests a homogeneous (bulk) effect, rather than a filamentary one (Mai 2015, Orfanidou 2018). In Nguyen *et al.* Secondary Ion Mass Spectroscopy (SIMS) shows direct evidence of the homogeneous effect, where Li ions were found to reach the Si substrate (Nguyen 2018). The advantage of such a mechanism over a filamentary one is related to the miniaturization of devices, which in the latter case of a filamentary one, it would be controlled by the filament size. Such a homogeneous RS

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mechanism is involving both an electrochemical effect, due to the valence change of Co, and an electronic effect of the MIT transition of the Li_xCoO_2 material.

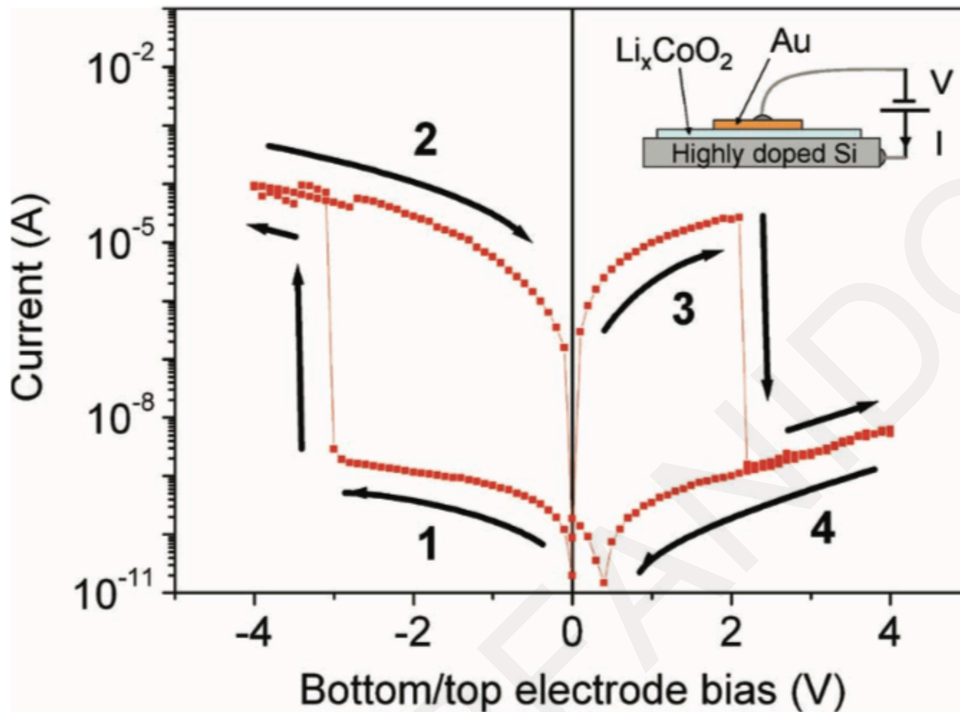

Figure 3.15 *I-V characteristics of a Li_xCoO_2 MIM cell (Moradpour 2011).*

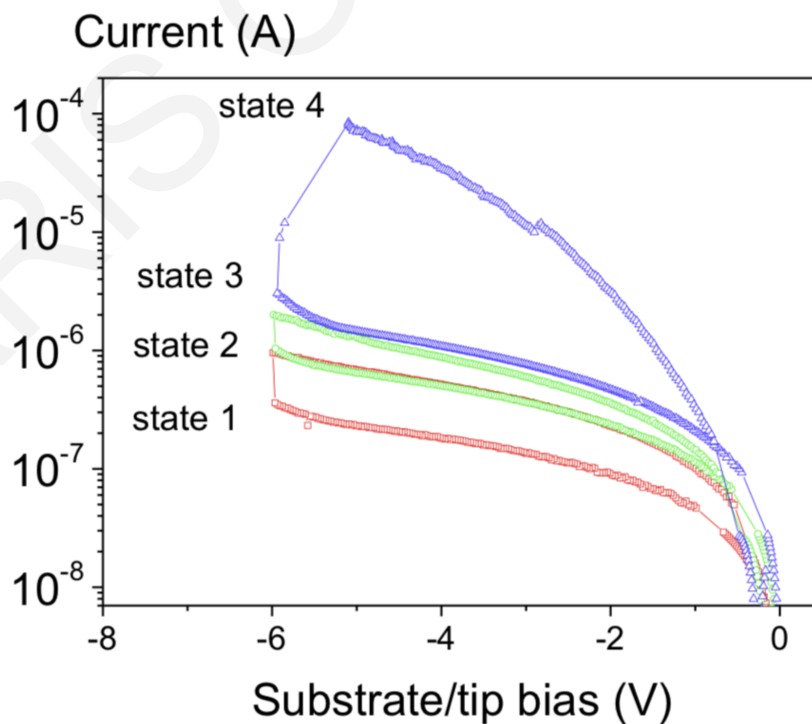

Figure 3.16 *Multilevel RS, four well-separated resistance states (Mai 2015).*

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All above-mentioned studies indicate the feasible use of Au/Li_xCoO_2/SiO_2/Si cells, as RRAM memories and neuromorphic circuit cells, and this would be easier because of the compatibility with CMOS technology, since the cells are built on Si substrate.

3.6 Conclusion

In order to improve non-volatile memories, write/read speed, number of cycles, and decrease of write/read voltages is required. RRAM memories are very promising candidates since they are based on electrochemical RS that could lead in the future to downscaling to ion dimensions.

Li_xCoO_2 as an already very well studied material that is used in Li ion batteries since 2011 proposed to be used in RS memory cells.

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Chapter 4

Li_xCoO_2 for Resistive Switching Applications

4.1 Introduction

In this chapter, the experimental techniques used in order to realize this thesis are presented. Firstly, the thin film deposition techniques are discussed, and secondly the characterization techniques. Subsequently, the obtained results from parametric studies on the Au/Li_xCoO_2/SiO_2/Si memory cell are shown, followed by the interpretation of each experiment.

The target of this part of the thesis is to unfold the RS mechanism that governs Au/Li_xCoO_2/SiO_2/Si memory cells. Memory cells based on Li_xCoO_2 thin films have been grown on Si substrates and two-probe current-voltage measurements were employed to investigate the origin and nature of RS behavior exhibited by these cells. The obtained results indicate that a voltage-driven metal-to-insulator transition of the active Li_xCoO_2 layer is responsible for the resistive switching behavior, which has a homogeneous nature.

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4.2 Experimental techniques

4.2.1 Pulsed Laser Deposition (PLD)

PLD belongs to the Physical Vapor Deposition (PVD) techniques and has been developed significantly in recent years, due to its ease of use and the ability to deposit complex stoichiometry materials. It was the first technique used to deposit thin films of $YBa_2Cu_3O_7$ (YBCO) superconductors (Dijkkamp 1987). Since then, many materials that are normally difficult to prepare by other methods (particularly complex oxides), were successfully deposited by PLD.

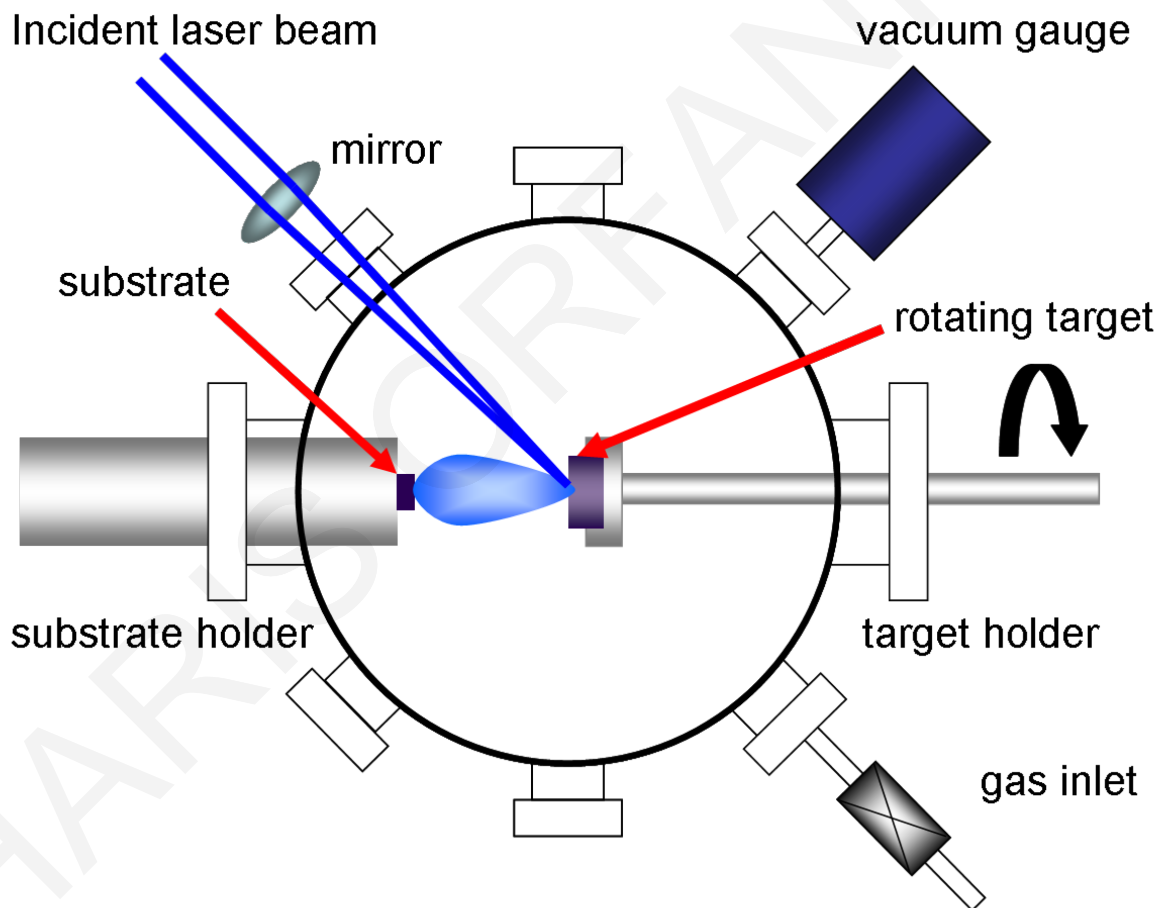

Figure 4.1 *Schematic of the PLD chamber configuration (Wang 2013).*

Figure 4.1 shows a schematic of the PLD technique. In a vacuum chamber, a focused laser beam is hitting a target of the desired stoichiometry. The wavelength of the laser beam is in ultraviolet region. Inside the chamber, the interaction of photons with the target material creates a plume. This plume of particles from the target material is collected on a substrate placed at a short distance from the target. Although the actual physical

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processes are quite complex, we can consider that the ejection of material occurs due to the rapid explosion of the surface of the target because of the heating caused by the laser beam. Unlike thermal evaporation, that produces a vapor whose composition depends on the partial pressures of the target items, the plume generated by PLD has a composition similar to the stoichiometry of the target.

Various experimental parameters have a strong influence on the properties of produced films. There are many laser parameters (laser intensity, pulse duration and repetition rate) that can be changed to result in different material. Moreover, the preparation conditions, which include the substrate temperature, target-substrate distance, the type of gas, and the pressure in the chamber, play a significant role in the formation of the films.

Some Li_xCoO_2 thin films were deposited employing the PLD technique. Pulses from a KrF laser (COMPexPro 201; $\lambda = 248$ nm, $\tau = 25$ ns and pulse repetition frequency of 1 Hz) impinged at an incidence angle of 45° on a rotating/toggling home-made polycrystalline $LiCoO_2$ target placed 60 mm away from the substrate (Svoukis 2012). The focused laser spot size was 2×5 mm^2 on the target resulting in a fluence of approximately 1.3 J/cm^2. Prior to each deposition, the chamber was evacuated to a base pressure $< 5\times10^{-6}$ mbar and during the deposition process the oxygen pressure in the chamber was kept constant at 0.1 mbar. Films were grown at 350 °C, using heating and cooling rates of 10 °C/min. The number of laser pulses was varied between 1250 and 10000 resulting into different Li_xCoO_2 thin film thicknesses. The thickness of the films has been determined by X-ray reflectivity (XRR) measurements using a 9 kW rotating anode Rigaku SmartLab X-ray diffractometer.

4.2.2 Radio Frequency (RF) and Direct Current (DC) Sputtering techniques

Sputtering is another type of PVD technique. Its operating principle involves ejecting material from a source target onto a substrate such as a silicon wafer, glass, etc. Sputtered atoms ejected from the target have a wide energy distribution. The sputtered atoms can ballistically fly from the target in straight lines and impact energetically on the substrates or the vacuum chamber walls. The sputtering gas is often an inert gas, such as argon. Sputtering involves many parameters that control the deposition and this makes it a complex process that allows a large degree of control over the growth and microstructure of the film. A simplified schematic is shown in Figure 4.2.

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RF magnetron sputtering is a low-cost and well-controlled method for thin film growth, and allows depositions of high quality and homogeneous Li_xCoO_2 thin films. RF magnetron Li_xCoO_2 sputtered thin films have been deposited at CEA Grenoble. Li_xCoO_2 thin films were deposited on highly doped p^{++}-type Si (111) wafers by RF magnetron reactive sputtering (Alcatel SCM 600 apparatus) using a stoichiometric $LiCoO_2$ target, with an applied RF power of 500 W. The films were grown at room temperature in a 3:1 Ar/O_2 atmosphere (process pressure 2.2 Pa) and a bias of 250 V was applied to the substrate. The films were measured using cross-section transmission electron microscopy (TEM) and determined to have a thickness of 100 nm. They were subsequently annealed at 580 ºC for 1 h in air in order to obtain the R-3m high-temperature Li_xCoO_2 phase. The crystallinity and phase purity of the Li_xCoO_2 films were investigated by GIXRD and measurements were carried out using a 9 kW rotating anode Rigaku SmartLab X-ray diffractometer. TEM studies have shown that the particular annealing step increases the native SiO_2 layer thickness from ~2-3 nm to ~8-9 nm (Mai 2015).

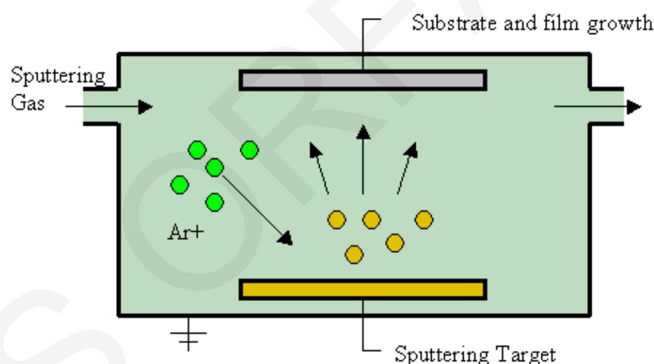

Figure 4.2 *Simplified schematic of sputtering deposition technique (Pub.Dom. 2016).*

After PLD or RF magnetron sputtering deposition of Li_xCoO_2 thin films and their structural characterization by X-ray diffraction (as described in section 4.2.3 below), 100 nm-thick Au electrodes were deposited by DC sputtering technique on Li_xCoO_2 thin films using hard electroformed Ni shadow masks with aperture sizes of: $0.5\times0.5, 0.4\times0.4, 0.3\times 0.3, 0.2\times0.2, 0.1\times0.1, 0.06\times0.06, 0.03\times0.03\ mm^2$ (Figure 4.3).

The Li_xCoO_2 films were grown on Si substrates of different dopant type (n^{++}, p^{++}) and orientation [(100), (111)] covered with very thin layers of SiO_2, which were either native in nature (~2 nm) or deposited by a radio-frequency (RF) sputtering technique (3-12 nm) following an HF treatment. All Si/SiO_2 substrates were thoroughly cleaned just prior to film deposition. The crystallinity and phase purity of the Li_xCoO_2 films, following post-annealing in air at 550 °C for 1 hour, were investigated by grazing incidence X-ray

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diffraction (GIXRD) using a 9 kW rotating anode Rigaku SmartLab X-ray diffractometer. The post-annealing step enhances the film crystallinity and also increases the SiO_2 thickness by ca. 5-6 nm.

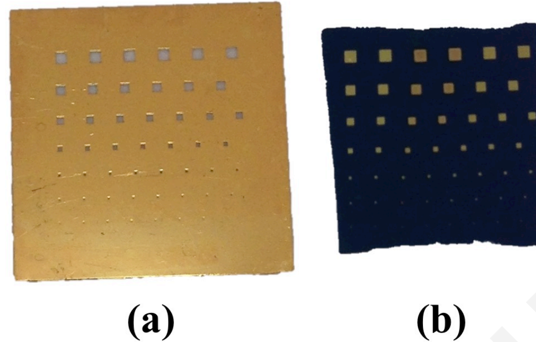

Figure 4.3 (a) *Veco B.V. high electroformed Ni shadow mask with aperture sizes of* $0.5\times0.5, 0.4\times0.4, 0.3\times0.3, 0.2\times0.2, 0.1\times0.1, 0.06\times0.06, 0.03\times0.03\ mm^2$, *(b) Au/$Li_xCoO_2$/$SiO_2$/Si memory cells after top electrode deposition using the Ni shadow mask.*

4.2.3 X-ray diffraction (XRD)

After PLD or RF magnetron sputtering deposition of the desired films, XRD analysis was required to characterize structurally the Li_xCoO_2 thin films. XRD is a very common non-destructive technique that is used for powder and thin film materials. It has a high penetration depth that allows precise determination of parameters of the crystal structure like lattice parameters, crystallographic orientation, grain size, etc. Additionally the wavelengths used are comparable with the interatomic distances of the material structure, and that allows for investigation of the crystal structures.

Generally, an intense beam of X-rays is placed on the crystal under study, and an X-ray intensity pattern is observed. The scattered X-rays interfere with each other, so the intensity has maxima in certain directions, if they satisfy Bragg's law:

$$2d_{hkl}\sin\vartheta = n\lambda \quad (4.1)$$

where hkl are the Miller indices of the crystallographic planes, d_{hkl} is the inter-planar spacing distance, ϑ is the incident angle, n the order of diffraction, and λ the wavelength of the X-ray beams (Figure 4.4).

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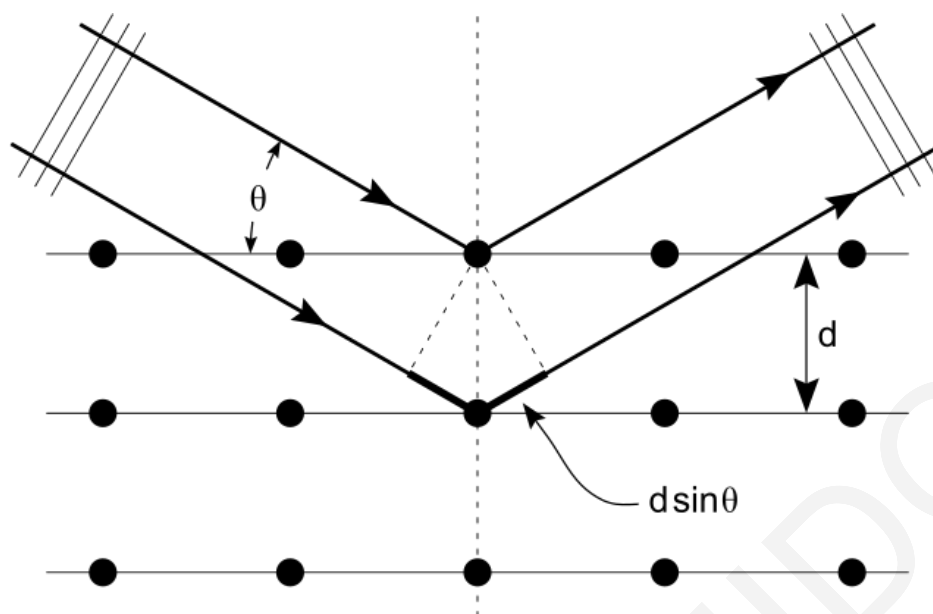

Figure 4.4 *Bragg's law schematic (Hydrargyrum 2016).*

The most commonly used diffraction geometry is the Bragg-Brentano geometry. In this arrangement, the X-ray source remains fixed, the sample rotates at a ϑ angle, and the detector rotates at a 2ϑ angle.

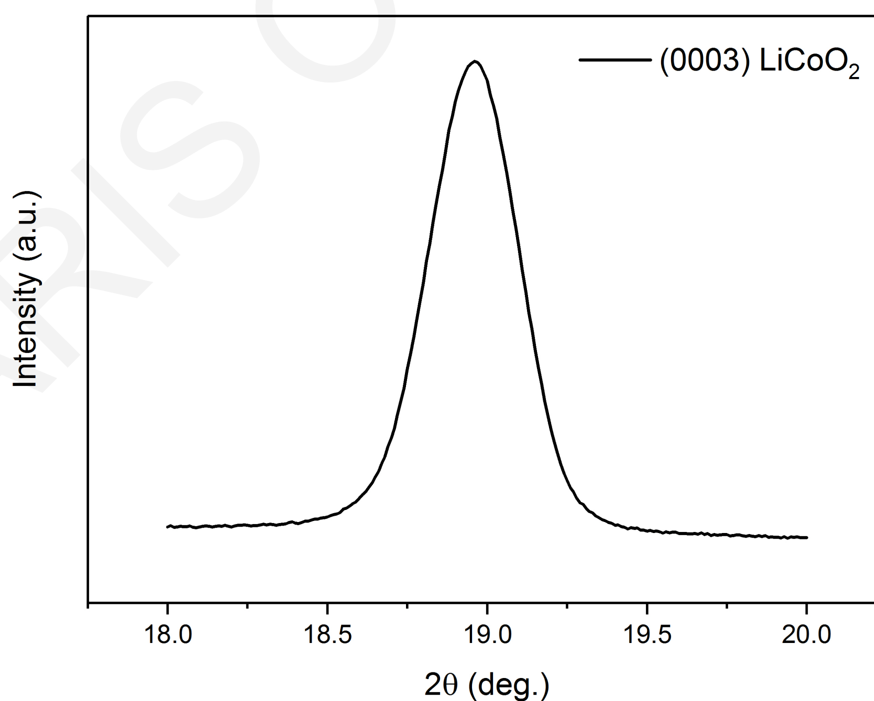

Figure 4.5 *Typical GIXRD pattern of a Li_xCoO_2 thin film.*

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All Li_xCoO_2 films were polycrystalline and partially textured. Grazing incidence X-ray diffraction (GIXRD) patterns exhibited two relatively strong Bragg reflections that correspond to the (003) and (101) planes of the high-temperature (HT) phase of $LiCoO_2$. Taking into account that there is no epitaxy and thus no strain effects, the calculated value of the c-axis lattice parameter corresponds to Li content x~1 based on the empirical relationship between x and c-axis lattice parameter length for bulk materials (Ménétrier 1999). Therefore, the annealed, sputtered-grown Li_xCoO_2 films are in the insulating phase.

A typical GIXRD pattern with only one Bragg reflection that corresponds to the (003) plane of the high-temperature (HT) phase of Li_xCoO_2 is shown in Figure 4.5.

4.2.4 I-V measurements setup

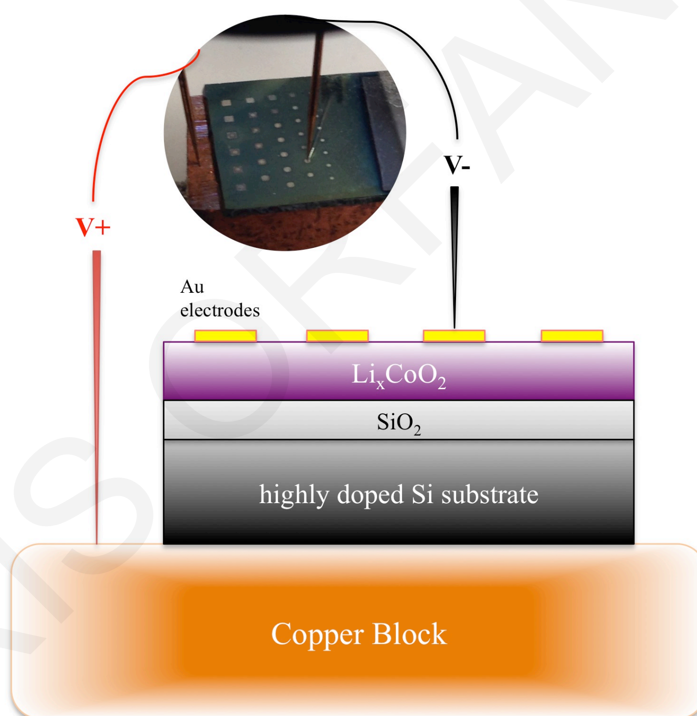

Figure 4.6 *Cross-section diagram of an Au/Li_xCoO_2/SiO_2/Si sample glued with Ag-paste on top of a copper block. Inset shows a photograph of the sample with the probe tips mechanically attached on the top and bottom electrodes of a memory cell.*

After sample fabrication, GIXRD characterization and top electrode deposition, I-V characterization with the homemade I-V setup takes place. The room-temperature current-voltage (I-V) characteristics of all cells were measured in air ambience using a two-probe setup (Keithley 6487) sourcing voltage and measuring current. 20 μm-radius Be-Cu probe tips, controlled using micro-manipulators, were used to make contact with the top (Au) and

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bottom (Si) electrodes (Figures 4.6, 4.7). The bottom electrode was in contact with the tip via a Cu block on which the sample was attached with Ag paste. The sample holder is controlled with micro-positioners. The I-V setup is noise shielded and grounded (Model 6487 2011).

The measurements were carried out by voltage sweeping with a current limit of 25 mA imposed by the instrument (or with an external resistor of 200 kΩ as a current limiter in order to protect our samples from uncontrolled high currents and also to obtain controlled RS cycles, where indicated). High-voltage electrode (V^+) is connected with the highly doped Si substrate and low-voltage electrode (V^-) is connected at the top Au electrode. In addition to the experimental studies, simulation studies were performed using COMSOL Multiphysics®.

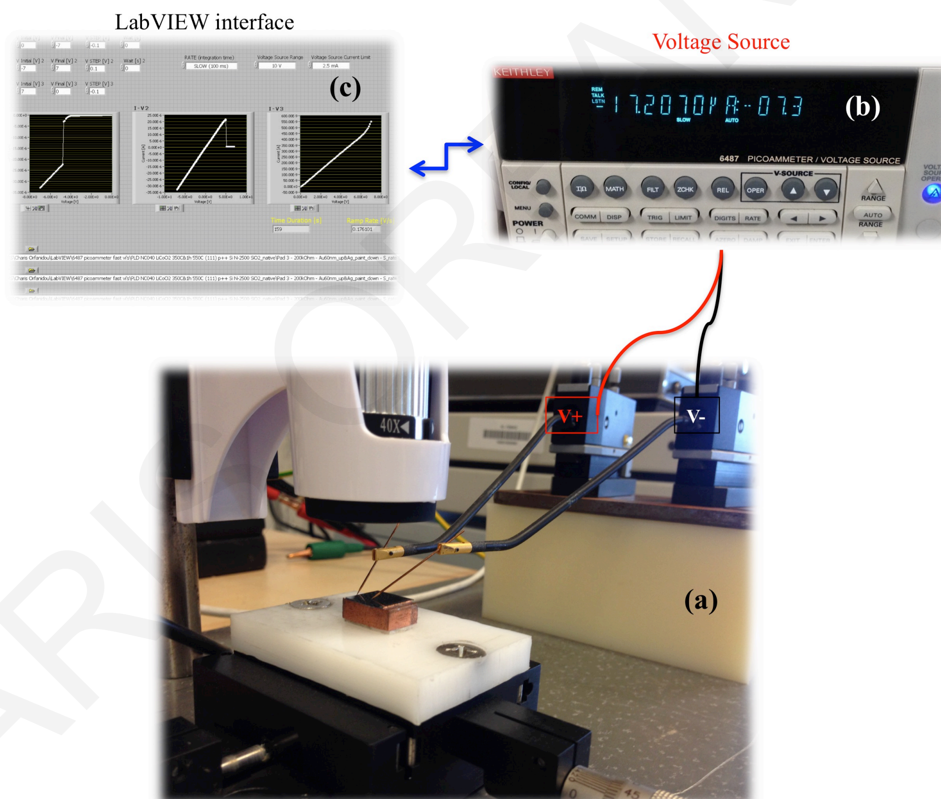

Figure 4.7 *Schematic of the I-V setup. (a) An Au/Li_xCoO_2/SiO_2/Si sample is mounted on the sample holder and probe tips are mechanically attached on the top and bottom electrodes of a memory cell. (b) A Keithley 6487 instrument sourcing voltage and measuring current is connected with the micro-manipulators. (c) The LabVIEW .vi program is controlling the voltage source and recording current measurements data.*

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The Keithley 6487 instrument, sourcing voltage and measuring current, is controlled by a homemade LabVIEW *.vi* program (Figure 4.8).

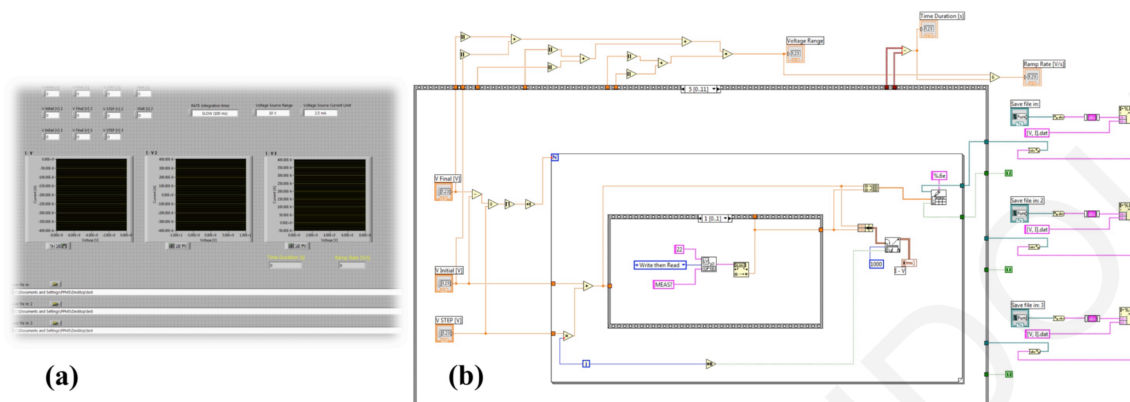

Figure 4.8 *(a) Homemade LabVIEW interface, and (b) block diagram.*

4.3 Resistive Switching in Au/Li_xCoO_2/SiO_2/Si memory cells

4.3.1 Resistive switching behavior

4.3.1.1 PLD-grown Li_xCoO_2 thin films

All Li_xCoO_2 films were polycrystalline and partially textured. Taking into account that there is no epitaxy – and thus no strain effects – the calculated value of the *c-axis* lattice parameter corresponds to Li content x≈1 based on the empirical relationship between x and *c-axis* lattice parameter length for bulk materials (Ménétrier 1999). Therefore, the annealed PLD-grown Li_xCoO_2 films are in the insulating phase.

Figure 4.9 depicts a typical I-V hysteresis loop and two following cycles of an Au/Li_xCoO_2/SiO_2/Si memory cell. For this type of cell to exhibit RS behavior, it is necessary to start the cycle by applying a negative bias voltage to the Si bottom electrode (i.e., the applied electric field has direction from the Au top electrode toward the Si bottom electrode); starting the other way only capacitive effects are observed. Apart from the RS observed, the upper electrode (Au) and bottom electrode (doped Si) behave like a capacitor, which can explain the minimum current obtained at ≈ +1.5V and not at 0V, at the end of the cycle.

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The same cell structure but with x≈0.7 (i.e., Li_xCoO_2 in the metallic phase) has been investigated as a potential thin-film solid-state source of electric power and no RS behavior has been reported to occur (Ariel 2006, Ariel 2005). In this configuration, Si functions as the anode, Li_xCoO_2 thin film functions as the cathode, and SiO_2 layer functions as the solid electrolyte.

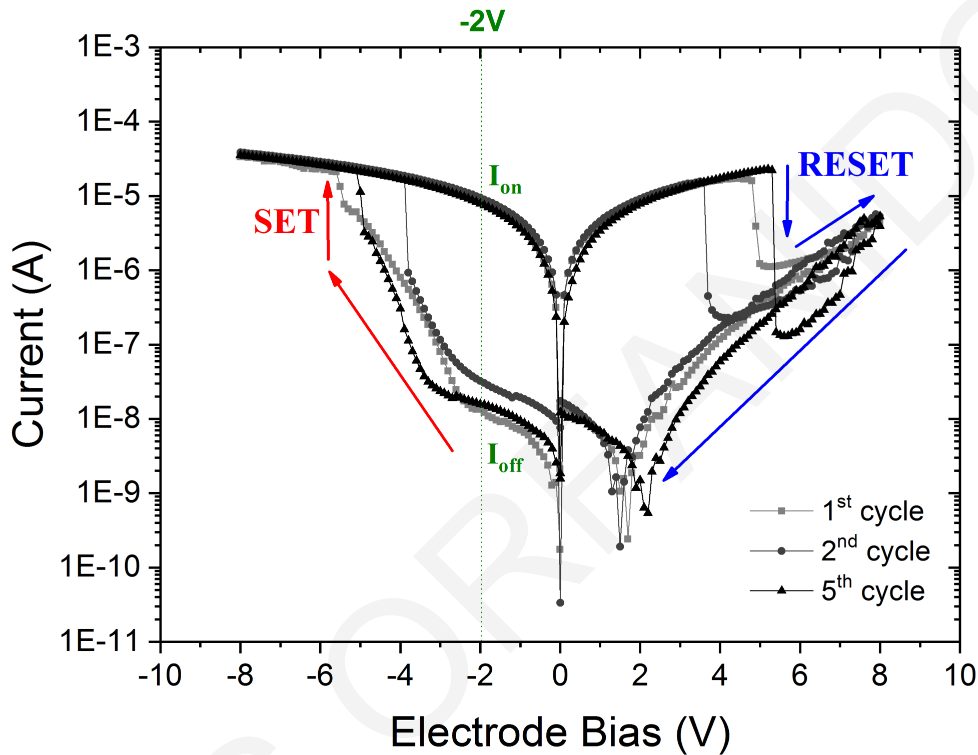

Figure 4.9 *Typical I-V characteristics of Au/Li_xCoO_2/SiO_2/Si PLD grown memory cells. Shown here are different cycles for a cell composed of a 50 nm-thick Li_xCoO_2 film deposited on a p++ type Si (111) substrate with a 3 nm SiO_2 layer as deposited by RF-sputtering, (I-V sweeps were performed on 500x500 μm^2 Au electrodes and 200 kΩ external resistor). The vertical dashed line at -2 V indicates the voltage bias at which I_{on} (LRS) and I_{off} (HRS) values were extracted in order to plot Figures 4.13, 4.14, and 4.15.*

4.3.1.2 RF magnetron sputtering grown Li_xCoO_2 thin films

Figure 4.10 depicts a typical I-V hysteresis loop of an Au/Li_xCoO_2/SiO_2/Si memory cell indicating RS behavior. The observed RS behavior is of bipolar type, i.e., the SET process (switching from high resistive state (HRS), to low resistive state (LRS); ON) occurs for a negative bias voltage while the RESET process (switching from LRS to HRS; OFF) occurs for a positive bias voltage (resistance ratio R_{HRS} / R_{LRS} = 71).

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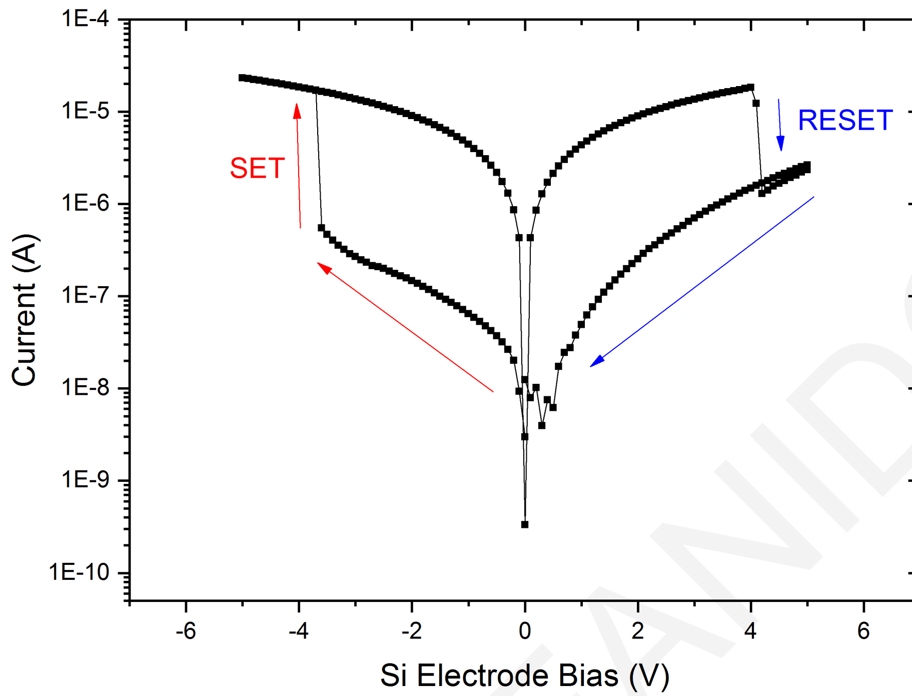

Figure 4.10 *Voltage sweep of a Au/Li_xCoO_2/SiO_2/Si RF magnetron sputtering grown memory cell (I-V sweeps were performed on 500x500 μm^2 Au electrodes).*

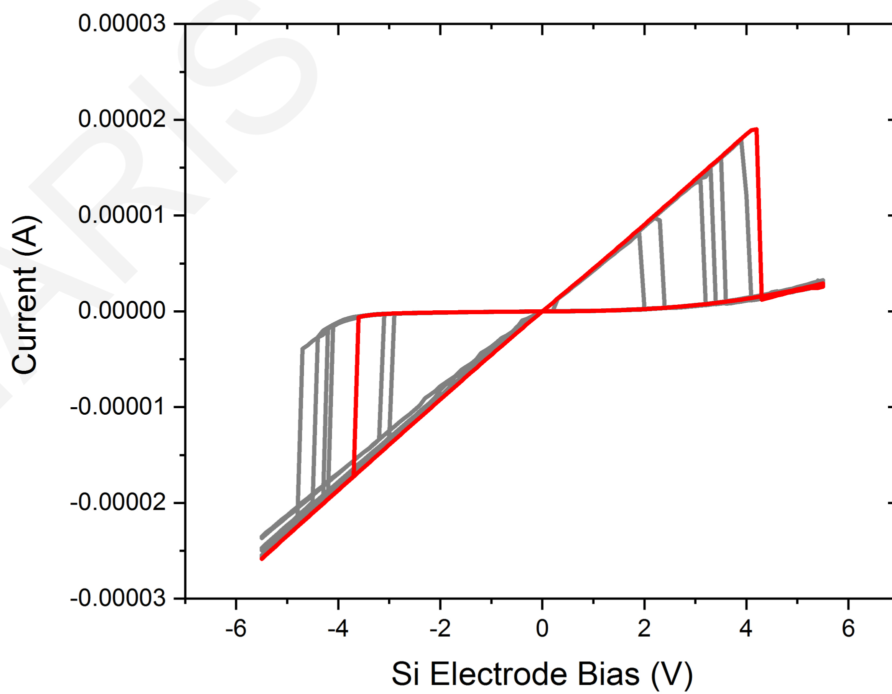

Figure 4.11 *I-V measurement of 10 consecutive (occasionally overlapping) RS cycles.*

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Good performance of the memory cells is investigated by repeated I-V sweeps shown in Figure 4.11. Additionally, highly coherent cycling endurance is demonstrated in Figure 4.12. As shown in the figure, degradation of the phenomena is occurring after 115 cycles. On the 116th switching cycle the memory cell reaches LRS typically at negative voltages, but at the positive voltages it does not switch back to the HRS. Possible mechanisms that lead to failure could be SiO_2 breakdown, since it is a very thin dielectric layer – of the order of 2-3 nm. In some cases severe damage of the top Au electrode could occur, if high temperatures are reached during sweeping.

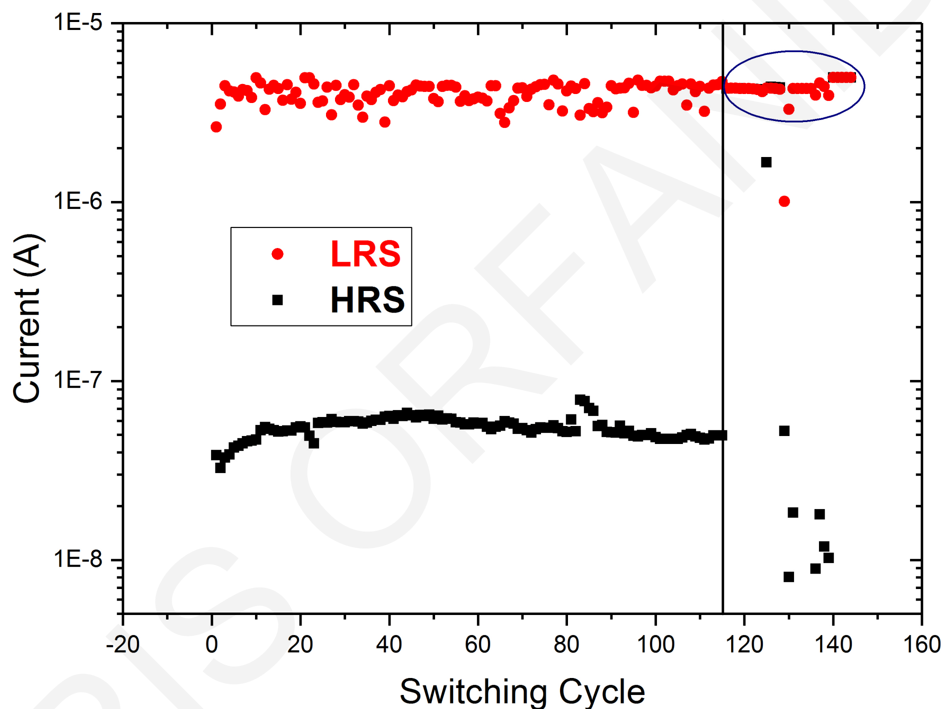

Figure 4.12 *LRS and HRS distribution over 144 RS cycles. Degradation of the RS performance is beginning to occur on the 116th switching cycle. The areas of overlapping HRS and LRS are indicated.*

The obtained results show that there are no significant differences in the behavior of the Au/Li_xCoO_2/SiO_2/Si memory cells, whether the Li_xCoO_2 thin films were deposited by the PLD technique or the RF magnetron sputtering deposition technique. Consequently, results obtained in studying the RS behavior in Au/Li_xCoO_2/SiO_2/Si memory cells are shown in following sections of this chapter by both deposition techniques. Additionally, Li_xCoO_2 thin films deposited by PLD occur to be less repeatable than RF magnetron

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sputtered thin films, so it was more controlled to use the sputtered samples for the top electrode experiments.

4.3.2 Effect of Li_xCoO_2 layer thickness

The effect of the Li_xCoO_2 layer thickness on the RS behavior of $Au/Li_xCoO_2/SiO_2/Si$ cells is discussed herein. A series of cells with varying Li_xCoO_2 thickness (different number of laser pulses: 1250, 2500, 5000, and 10000) were fabricated on p^{++} Si (111) substrates covered with a 3-nm-thick SiO_2 layer. A correlation between the number of laser pulses and the thickness of the Li_xCoO_2 layers was extracted by fitting XRR data.

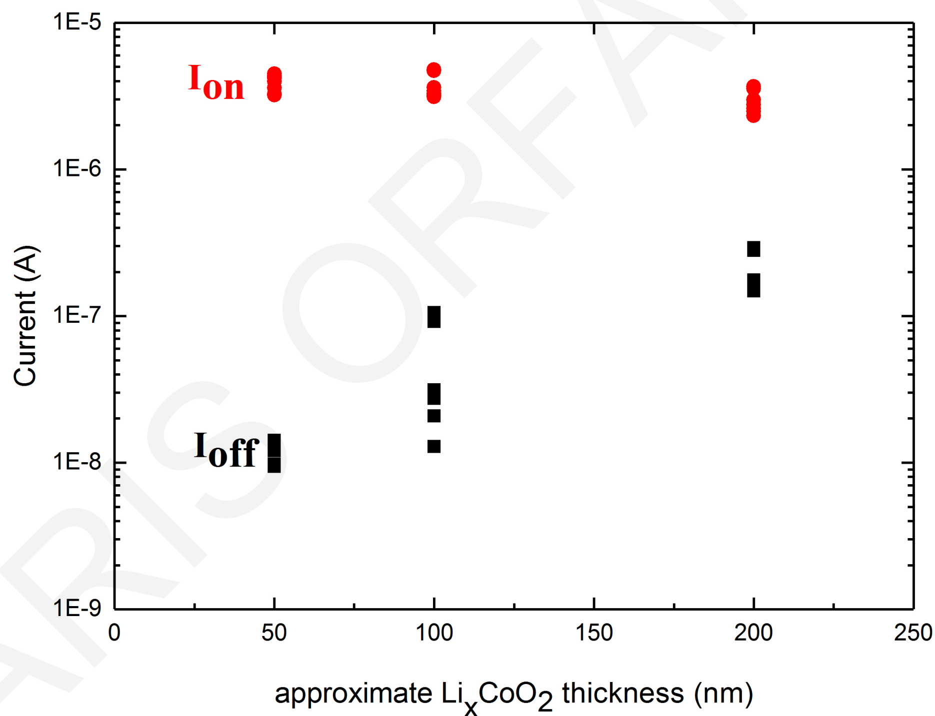

Figure 4.13 *Dependence of I_{on} and I_{off} on Li_xCoO_2 thickness. SiO_2 thickness is 3 nm (RF-sputtered) for all cells shown in the graph (I-V measurements with a 200 kΩ external resistor). Different data points for the same Li_xCoO_2 thickness correspond to different cells, and also to different cycles for the same cell. The cells have been fabricated on p++ type Si (111) substrates.*

It was concluded that 50 laser pulses correspond to the growth of 1 nm-thick Li_xCoO_2 layer and thus, the thickness of the Li_xCoO_2 films in our cells were: 25, 50, 100

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and 200 nm. Figure 4.13 shows the dependence of LRS current (I_{on}) and HRS current (I_{off}) on Li_xCoO_2 thickness (t_L). These currents correspond to the bias voltage of -2 V during voltage sweeping. Specifically, I_{off} corresponds to the initial HRS current of every cycle and I_{on} corresponds to the LRS current after setting the cell (see Figure 4.9).

We observe that I_{off} decreases (thus, the HRS resistance increases) and the I_{on}/I_{off} ratio increases as t_L decreases. This is opposite to what was initially expected. Indeed, if we assume the following HRS resistance expression: $R_{HRS} = \rho.t_L / S$, where ρ is the film resistivity and S the Au top electrode surface, R_{HRS} should decrease for a decreasing t_L Li_xCoO_2 thickness. A plausible explanation for the unusual observation is that x, the Li content, is higher for lower Li_xCoO_2 layer thickness; so ρ increases and, consequently, R_{HRS} increases and I_{off} (that flows through the cell) decreases, when t_L decreases. Moreover, no RS is observed in the cells with t_L=25 nm, indicating that there is a critical thickness between 25 and 50 nm for Li_xCoO_2 that results in functional RS cells. For such thin films, the applied electric field intensity (>4×10^5 V/cm) could be high enough to induce breakdown in many insulators, so this may be the reason why we do not observe RS in thinner films.

4.3.3 Effect of SiO_2 layer thickness

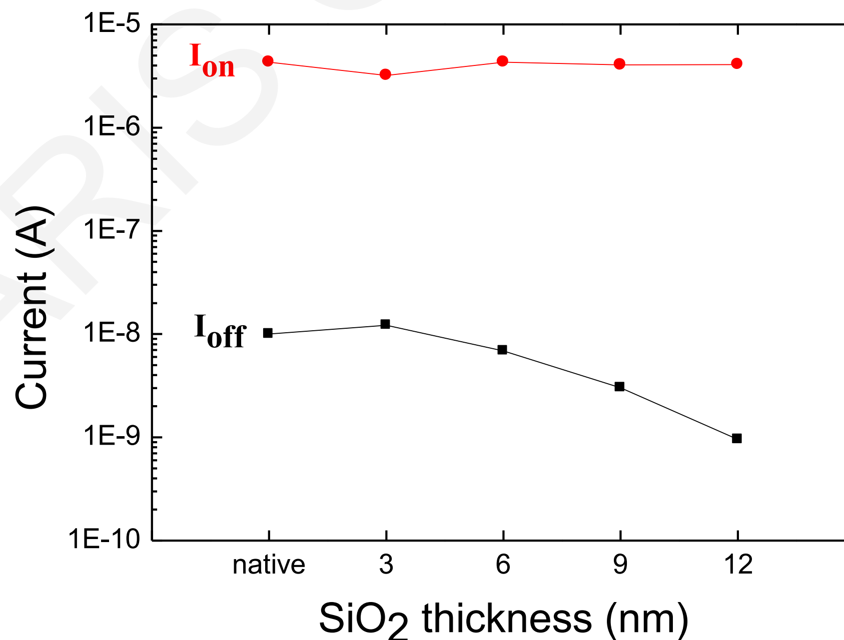

Figure 4.14 *Dependence of I_{on} and I_{off} on the deposited SiO_2 thickness (I-V measurements with a 200 kΩ external resistor). The thickness values correspond to the ones of the as-*

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grown SiO_2 films prior to post-deposition annealing. Li_xCoO_2 films have an approximate thickness of 50 nm and the substrates are p^{++} type Si (111).

Figure 4.14 shows the dependence of I_{on} and I_{off} on the thickness of the deposited SiO_2 (t_S). As expected I_{off} decreases and the I_{on}/I_{off} ratio increases with increasing t_S. Therefore, the contribution of SiO_2 to the total resistance of the cell depends simply on its thickness.

4.3.4 Effect of type and orientation of Si substrates

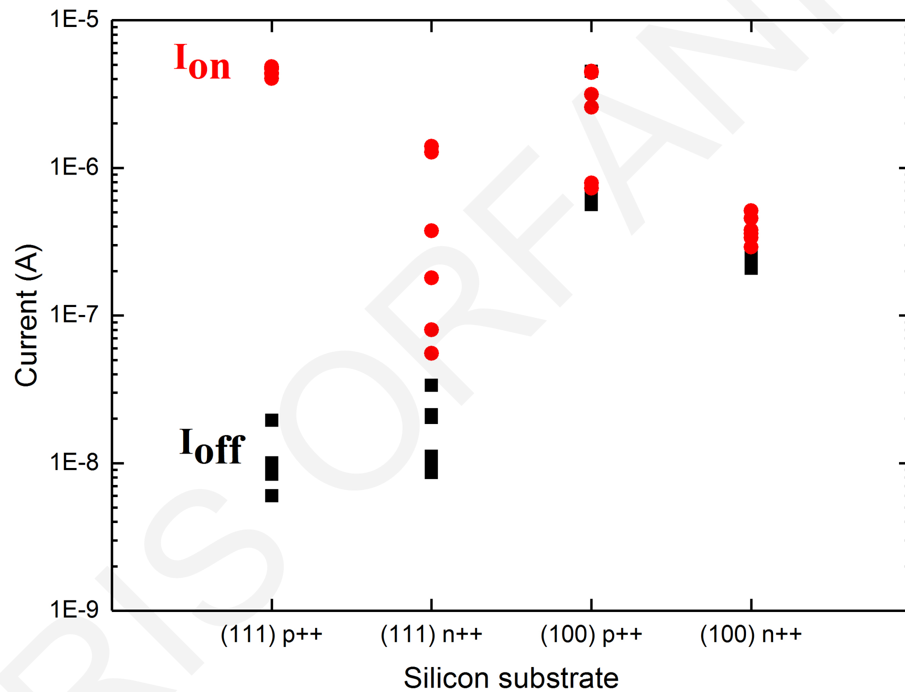

Figure 4.15 *Dependence of I_{on} and I_{off} on the type and orientation of Si substrates (I-V measurements with a 200 kΩ external resistor). Different data points for the same Si substrate correspond to different cells, and also to different cycles for the same cell. Li_xCoO_2 films have an approximate thickness of 50 nm and the SiO_2 is native.*

Figure 4.15 shows the dependence of I_{on} and I_{off} on the type and orientation of the Si substrates. Four different combinations have been examined: p^{++} Si (111), p^{++} Si (100), n^{++} Si (111) and n^{++} Si (100). All cells were fabricated using similar components (i.e., similar Li_xCoO_2 thickness of approximately 50 nm, and similar Au electrode thickness (60nm) and lateral area (500 μm × 500 μm)) and underwent the same post-annealing

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treatment. More frequent and clear RS behavior was exhibited by devices based on p^{++} (111) Si substrates. This observation is attributed to the growth of a thicker SiO_2 layer during post-annealing in the case of (111)-oriented Si substrates (May 2006) and also to the fact that in the case of n-type Si substrates the cell could be negatively affected by the p-i-n junction behavior (Kittel 2005, Shockley 1949).

4.3.5 Effect of Au top electrode size

To determine whether the nature of RS is homogeneous or filamentary, the dependence of I_{on} (measured current at LRS) and I_{off} (measured current at HRS) on the surface area of the top Au electrode was investigated (a schematic diagram of the investigated cells is shown in the inset of Figure 4.16).

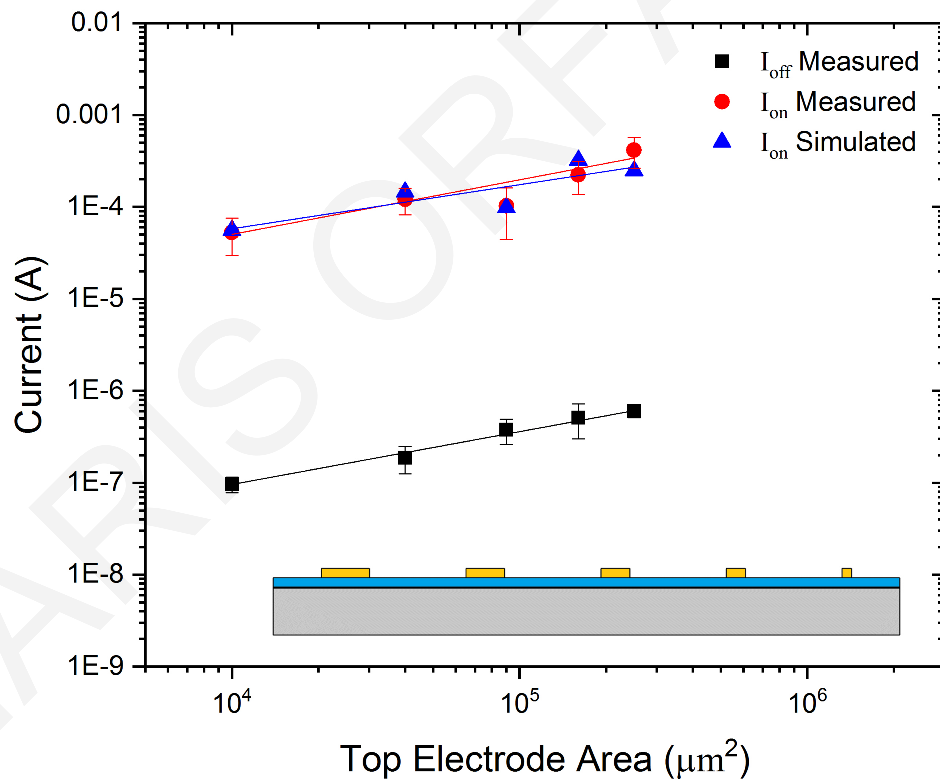

Figure 4.16 *Dependence of current on top electrode area of Au/Li_xCoO_2/SiO_2/Si memory cells: experimental I_{off} (at -2 V; black squares), experimental I_{on} (at -2 V; red circles) and simulated I_{on} (at -2 V; blue triangles). Inset: a cross-section schematic diagram of five cells defined by the Au (yellow) top electrodes of 500x500, 400x400, 300x300, 200x200*

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and 100x100 μm², as deposited on a Li_xCoO_2 thin film (blue) grown on a Si (grey) / native SiO_2 (black) substrate. The x and y dimensions are not to scale.

Filamentary switching should result in a very low (or no) correlation (Sim 2005) of electrode area with I_{on} or I_{off}. Conversely, homogeneous switching, which is a bulk effect, is expected to exhibit a direct correlation between electrode area and I_{on} and I_{off}.

Figure 4.16 is a log-log plot of I_{on} and I_{off} currents as a function of Au electrode area. A quasi linear dependence of log(I_{on}) and log(I_{off}) on the logarithm of the top electrode area is observed with positive slopes of ~0.6 for both measured resistance states. The difference of almost three orders of magnitude between the HRS and LRS current levels is attributed to the modification in the resistivity of Li_xCoO_2 layer upon its switching from insulating to metallic phase, as discussed above and shown in Figure 3.14. These results entrench the hypothesis of a homogeneous mechanism for Au/Li_xCoO_2/SiO_2/Si thin film memory cells (Orfanidou 2018).

Simulation studies on the same cell configuration were carried out in order to corroborate the experimental results discussed above. For the simulation, specific resistivity value has been assigned to the Li_xCoO_2 layer corresponding to LRS (Ménétrier 1999), typical literature resistivity values have been used for the rest of the cell constituent layers (Cho 2014, Hart 1998, Andriyevsky 2014), and a homogeneous effect is inherently adopted. A comparison of the experimental with the simulated data indicates that a quasi linear dependence of log(I_{on}) on the logarithm of the top electrode area is observed. Additionally, the current levels are similar in both experimental and simulated LRS states. Therefore, the simulation results provide additional support for the proposed homogeneous nature of RS in Au/Li_xCoO_2/SiO_2/Si thin film memory cells.

4.3.6 Effect of top electrode material

In order to define whether the top electrode material has an active role in the RS observed in Au/Li_xCoO_2/SiO_2/Si thin film memory cells or not, positive voltage sweeping were applied (0 V → +5 V → 0 V, with 0.1 V step) on Al/Li_xCoO_2/SiO_2/Si, Ni/Li_xCoO_2/SiO_2/Si, and Ti/Li_xCoO_2/SiO_2/Si memory cells. The Al top electrode was selected as a Li receiver and was compared with the Au top electrode. The Ni and Ti top electrodes were selected as Li barrier metals.

Figure 4.17 shows the behavior of Au and Al top electrodes. Even though a small hysteresis is observed, this cannot be attributed to RS phenomena since for memory cells

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with Li_xCoO_2 thin films the hysteresis attributed to RS phenomena is of a greater size by two to three orders of magnitude, as can be seen in Figures 4.9 and 4.10. Also the obtained curves lack other characteristics like sharp transition.

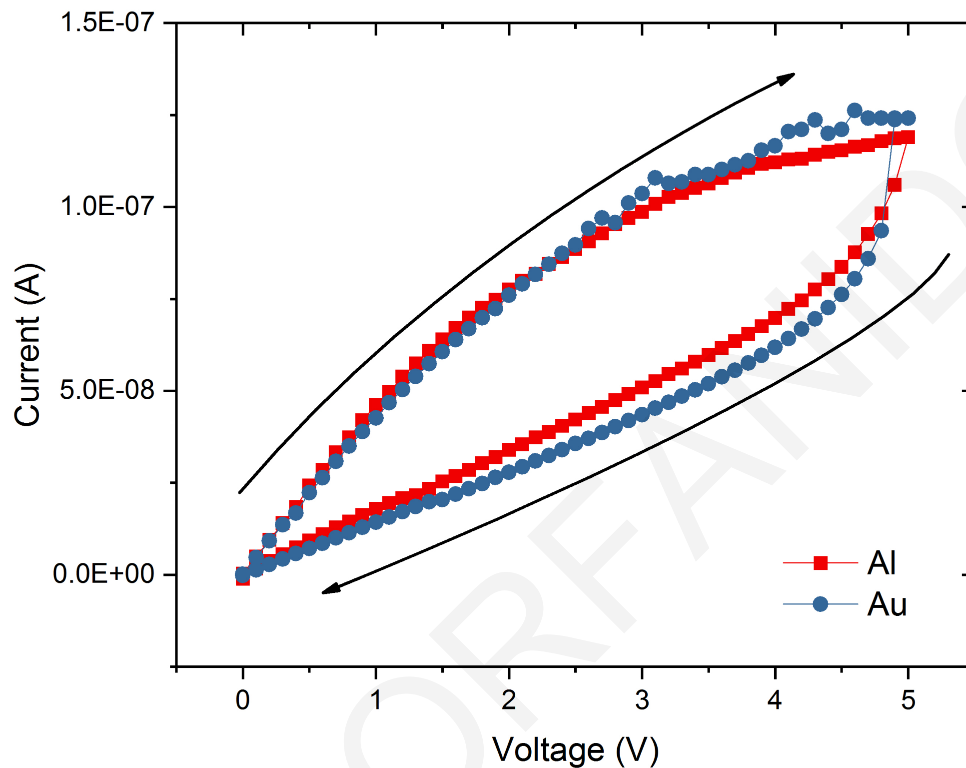

Figure 4.17 *Positive voltage sweeps of a Al/Li_xCoO_2/SiO_2/Si (red squares) and a Au/Li_xCoO_2/SiO_2/Si (blue circles) memory cells.*

Figure 4.18 shows the behavior obtained for positive voltage sweeps on Ni and Ti top electrodes. The results indicate a capacitive effect, since the measured currents are very low and negative currents are obtained at positive voltages. Ni and Ti metallic electrodes are Li barriers, so with Ni or Ti as the first plate, the highly doped Si the second plate, and the Li_xCoO_2 thin film and SiO_2 layer as the dielectric, the cell with that positive biasing behaves more like a capacitor.

The obtained results indicate that the top electrode material does not play a significant role to the RS phenomena observed in Au/Li_xCoO_2/SiO_2/Si, so choosing a good metallic top electrode, as is Au, further studies can be performed.

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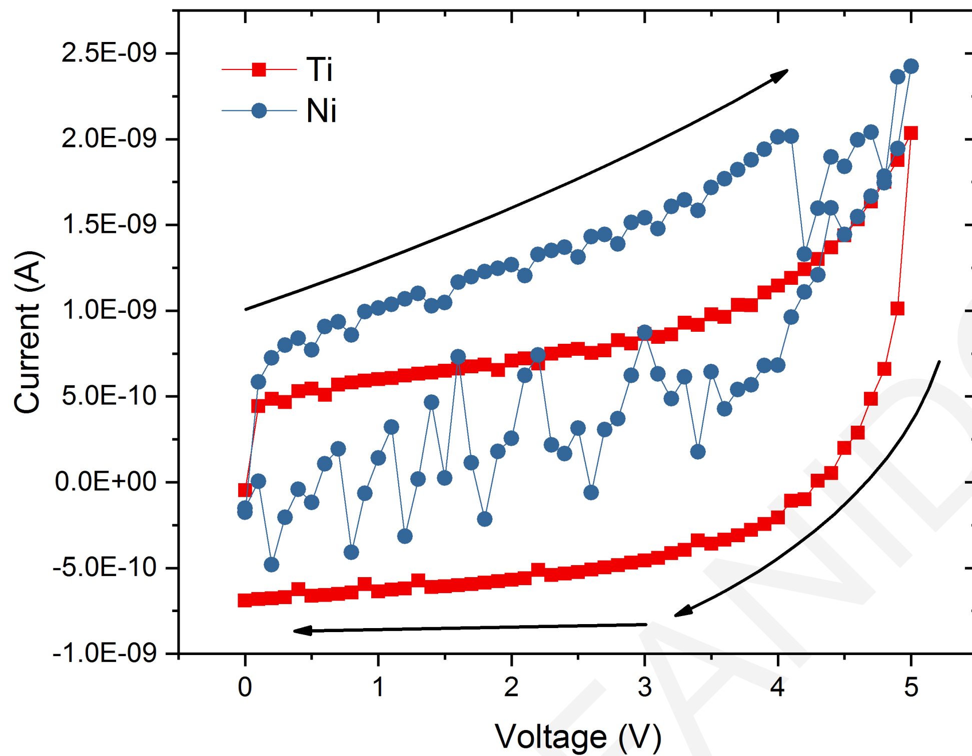

Figure 4.18 *Positive voltage sweeps of a Ti/$Li_xCoO_2/SiO_2/Si$ (red squares) and a Ni/$Li_xCoO_2/SiO_2/Si$ (blue circles) memory cells.*

4.3.7 Effect of Li content in Li_xCoO_2 thin films

In order to determine whether the Li-ion intercalation/deintercalation – and the consequent reversible metal-to-insulator transition of the Li_xCoO_2 layer – is responsible for the observed RS behavior of Au/$Li_xCoO_2/SiO_2/Si$ memory cells, a comparison of the J-V characteristics of a cell with different stoichiometry (x) of Li_xCoO_2 was made. The Li content modification was achieved through a chemical delithiation process as described in the experimental section. I-V sweeps were performed on the same cells (500x500 μm^2) before and after chemical delithiation. Chemical affinity of loosely bound Li^+ ions to the acidic solution leads to the deintercalation and diffusion of Li^+ ions from the laminar Li_xCoO_2 structure toward the main solution.

Chemical delithiation experiments of Li_xCoO_2 films were carried out in $K_2S_2O_8$ aqueous solutions (25 mg/ml) (Ishida 2010). Temporally regulated infusions of the thin film devices in the acidic aqueous solution under moderate agitation and at 50 ºC were carried out. Three successive delithiation infusions, followed by deionized water rinsing,

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drying under N_2 stream, and GIXRD measurements of the (003) peak shift enabled the time-depended observation of Li^+ diffusion from the film to the acidic solution. The total delithiation process time was 1 hour and 45 minutes.

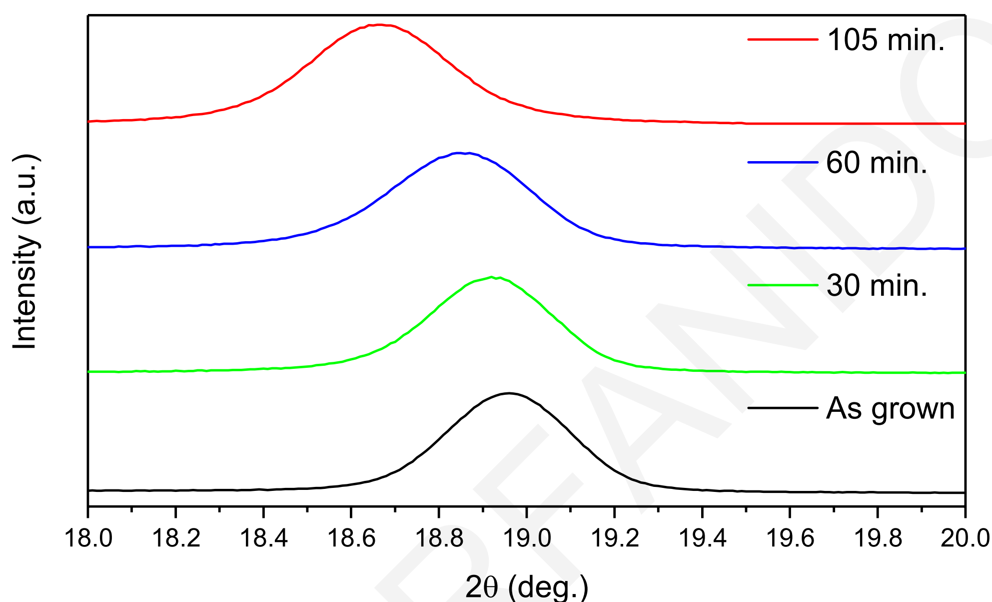

Figure 4.19 *GIXRD patterns showing the shift of the (003) Li_xCoO_2 peak after repeated delithiation steps, indicating a reduction of the Li content (incidence angle is 1°).*

Temporal monitoring of the removal of Li^+ ions from the structure was undertaken through GIXRD analysis of the chemically treated thin film for various infusion durations. Figure 4.19 shows the shift of the (003) Li_xCoO_2 peak with increasing (total) infusion time, which indicates a modification of the c-axis lattice parameter. Figure 4.20 shows the correlation of infusion time with the gradual enlargement of the c-axis lattice parameter in the film (left side), due to the increasing electrostatic repulsion between the CoO_2 layers, and the Li content value (right side) (Ménétrier 1999). It is apparent that Li^+ ions are gradually removed from the octahedral sites between the CoO_2 layers resulting in the formation of a Li-deficient Li_xCoO_2 thin film. The chemical delithiation process was terminated when the Li content reached x~0.65 ensuring that Li_xCoO_2 was in the metallic Hex-II phase, as is evident from the dependence of Li_xCoO_2 resistivity on the Li content shown in Figure 3.14.

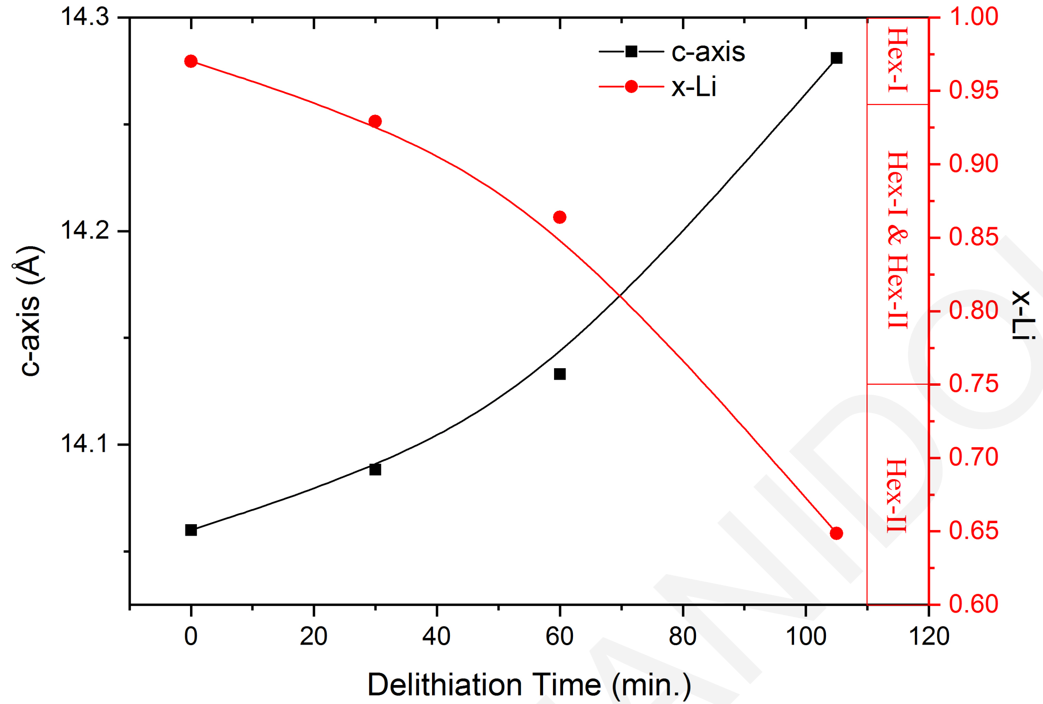

Figure 4.20 *c-axis lattice parameter (left, black squares) and Li content (right, red circles) of a Li_xCoO_2 layer as a function of delithiation time.*

Figure 4.21 shows the corresponding J-V sweeps for the same Au/Li_xCoO_2/SiO_2/Si cell before and after chemical delithiation. The cell before delithiation (x~0.97) shows RS behavior, as discussed previously, whereas the same cell following delithiation (x~0.65) displays no hysteretic behavior, indicating that no RS takes place. It can therefore be deduced that in order to observe RS phenomena in this type of cells, the Li_xCoO_2 films must be initially in the insulating Hex-I phase, which requires the initial Li content of the film to be x > 0.93. Hence, this is the first time direct proof is provided concerning the critical relation of Li stoichiometry to the RS mechanism, and is indicative of the underlying mechanism being the metal-to-insulator transition of the Li_xCoO_2 film (Orfanidou 2018).

Additionally, these results indicate that Li-ion intercalation/deintercalation originating from the active Li_xCoO_2 layer plays the dominant role in RS and no contribution is made to RS from the other constituent layers of the memory cells, apart from the bottom Si electrode, which acts as the host of the Li^+ ions according to the proposed mechanism. It is noted that a similar cell structure albeit with x~0.7 (i.e., Li_xCoO_2 in the metallic phase) has been investigated as a potential thin film solid-state source of electric power and no RS behavior has been reported to occur (Ariel 2006, Ariel

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2005). In this configuration, the Si substrate functions as the anode, the Li_xCoO_2 thin film functions as the cathode, and the SiO_2 layer functions as the solid electrolyte.

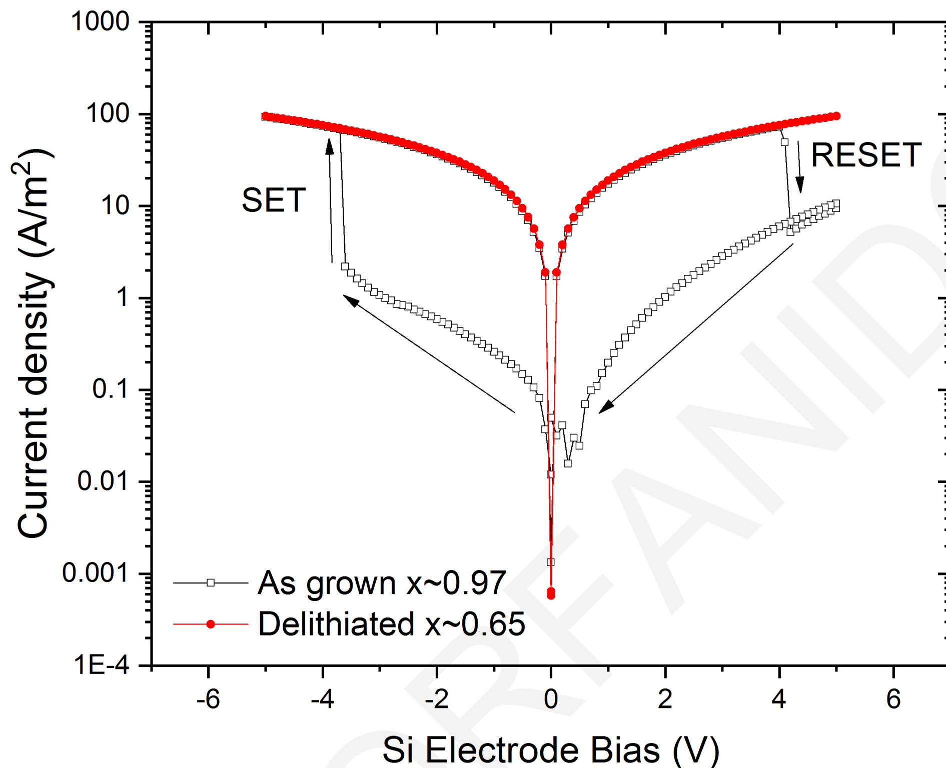

Figure 4.21 *Voltage sweeps before (x~0.97, black open squares) and after (x~0.65, red filled circles) chemical delithiation of a Au/Li_xCoO_2/SiO_2/Si memory cell.*

4.4 Resistive switching mechanism in Au/Li_xCoO_2/SiO_2/Si memory cells

RS behavior has already been observed in memory cells based on Li_xCoO_2 thin films grown by RF-sputtering (Moradpour 2011, Mai 2015). The proposed mechanism responsible for the RS behavior of the investigated Au/Li_xCoO_2/SiO_2/Si memory cells involves voltage-driven diffusion of Li ions (Mai 2015). Specifically, it has been proposed that the electrochemical redox reactions that take place under the application of bias voltage result in the intercalation/deintercalation of Li^+ ions to/from the Li_xCoO_2 thin film and hence, in the occurrence of a reversible metal-to-insulator transition of Li_xCoO_2 layer.

This mechanism is akin to the stages of charging and discharging of Li-ion rechargeable batteries. This is most prominently evident in the abrupt changes observed in

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the J-V curves of Fig. 1. These sharp transitions are associated with the dissociation energy of Li^+ in Li_xCoO_2 (~3.95 V (Dahéron 2008, Shibuya 1996, Molenda 1989)), which manifests – with sufficiently high sweep rates – into an abrupt change in current. Moreover, it is noted that the contribution of oxygen vacancies to RS has not been considered in this study because there has been no experimental evidence for the presence of oxygen vacancies in Li_xCoO_2 (Hertz 2008) and this has been recently attributed to their high formation energy based on density functional calculations (Hoang 2014).

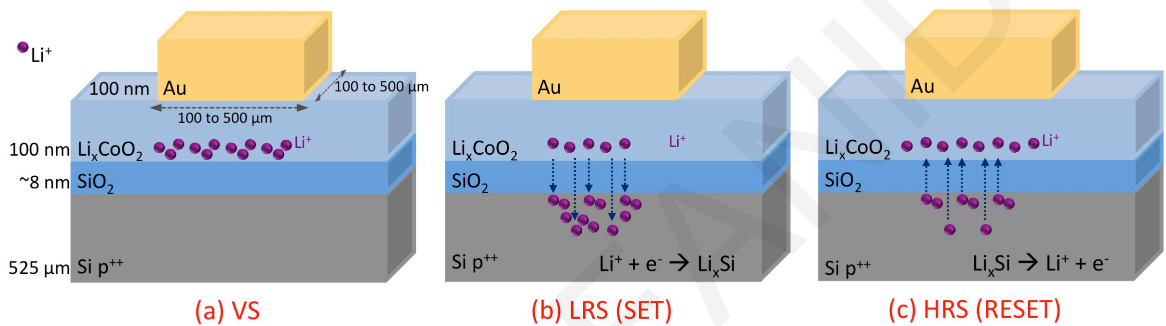

Figure 4.22 *Schematic view of a Au/Li_xCoO_2/SiO_2/Si memory cell and the mechanism proposed: (a) cell at virgin state (VS), (b) cell at LRS, and (c) at HRS (Orfanidou 2018).*

The temporal breakdown of this reversible process (i.e. the intercalation/deintercalation of Li^+ ions to/from the Li_xCoO_2 thin film) is as follows: The cells are fabricated in the battery-equivalent discharged state, in which Li^+ ions are located between the CoO_2 block layers (Figure 4.22(a)). Therefore, Li_xCoO_2 is in its insulating phase, where Li content is $0.95 < x < 1$ (Ménétrier 1999), and the cell is in HRS. Upon the action of a negative bias voltage to the Si electrode, Li^+ ions deintercalate from the Li_xCoO_2 cathode; concurrently, the valence state of Co ions shifts from 3+ to 4+ (oxidation) and electrons are released to the external circuit. The deintercalated Li^+ ions are transported through the SiO_2 layer to the negatively charged Si anode (Nguyen 2018) and upon reaching the SiO_2/Si interface are reduced to neutral Li atoms, which chemically react with the Si atoms to form Li-Si compounds (Ariel 2005). This is equivalent to the charging process of a battery and, due to Li^+ deintercalation, Li_xCoO_2 is expected to transform to a metallic phase, switching the cell to LRS (Figure 4.22(b)). Therefore, the SET process in this memory cell parallels the charging process of a Li-ion battery cell.

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Upon the application of a positive bias voltage to the Si electrode, the reverse mechanism occurs, which is the battery-equivalent discharging process and, due to Li^+ intercalation, Li_xCoO_2 is transformed to an insulating phase, switching the cell back to HRS (Figure 4.22(c)). Therefore, the RESET process in this memory cell parallels the discharging process of a Li-ion battery cell.

4.5 Conclusion

This chapter reports on the results of experiments concerning the RS behavior in $Au/Li_xCoO_2/SiO_2/Si$ memory cells. The series of experiments performed aim at the identification and validation of the RS mechanism of $Au/Li_xCoO_2/SiO_2/Si$ memory cells.

The effects of (a) Li_xCoO_2 layer thickness, (b) SiO_2 layer thickness, (c) type and orientation of Si substrate, (d) Au top electrode size, (e) top electrode material, and (f) Li content in Li_xCoO_2 thin films, where investigated.

The SiO_2 thickness affects proportionally the resistance of the cell at the HRS and p^{++} (111) Si substrates seem to be the most suitable ones on which to study RS phenomena in $Au/Li_xCoO_2/SiO_2/Si$ cells. The I_{on}/I_{off} ratio increases for thinner Li_xCoO_2 layers but there is a critical Li_xCoO_2 thickness, between 25 and 50 nm, below which no RS behavior is observed.

The obtained results shed light on two important aspects of the proposed RS mechanism: (i) the microscopic origin and (ii) the nature of the underlying RS mechanism. The microscopic origin of the RS mechanism is shown through chemical delithiation experiments to be the metal-to-insulator transition in the active Li_xCoO_2 layer. The underlying RS mechanism is shown – through experimental and simulation studies of the current dependence on the top electrode area – to be of a homogeneous nature.

Additionally, the similarity of the aforementioned proposed mechanism to battery cycling and the lack of necessity for an electroforming step have led to the speculation that the RS switching is not of filamentary nature.

A plausible mechanism has been put forward according to which electrochemical redox reactions that take place under the application of the bias voltage result in the intercalation and deintercalation of Li ions to/from the Li_xCoO_2 thin film and, hence, the occurrence of a reversible metal-to-insulator transition.

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Chapter 5

Conclusion

5.1 $La_5Ca_9Cu_{24}O_{41}$ for Thermal Management Applications

The simulation study of LCCO compound as a heat channeling BOX layer in ETSoI devices showed a significand decrease of temperature both for the operating transistors and for a hot-spot region.

Further research on this specific compound would be of high importance since LCCO offers a unique combination of properties compared to conventional materials, i.e., it exhibits a highly anisotropic thermal conductivity that constrains the heat primarily along one crystal axis, together with electrical insulation.

The exploitation of LCCO in thermal management applications, as the one discussed in this thesis, would require the growth of high-quality *c*-axis-oriented epitaxial LCCO thin films on technologically useful substrates such as Si. Even though this seems rather difficult to achieve because of the structural complexity of the compound, further investigation could may result to the desired material, and put forward the manufacturing of an ETSoI device with LCCO BOX layer.

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5.2 Li_xCoO_2 for Resistive Switching Applications

Resistive switching behavior has been observed in Au/Li_xCoO_2/SiO_2/Si cells where the Li_xCoO_2 layer has been deposited both by PLD and RF magnetron sputtering. The parametric study on Li_xCoO_2 layer thickness, SiO_2 layer thickness and different Si substrates on type and orientation is a significant step towards the understanding of the mechanism governing this type of resistive switching phenomena.

Specifically, the microscopic origin of the RS mechanism is shown through chemical delithiation experiments to be the metal-to-insulator transition in the active Li_xCoO_2 layer. The underlying RS mechanism is shown – through experimental and simulation studies of the dependence of current on the top electrode area – to be of a homogeneous nature.

Further investigation of the Au/Li_xCoO_2/SiO_2/Si cell structure in order to achieve more consistent and repeatable resistive switching phenomena is required, as well as investigation of the failure mechanisms that limit cycling endurance. Identification of the resistive switching mechanism is the most important parameter for the advancement of RRAM memories and the transition from laboratory research to industrial applications.

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References

Model 6487 Picoammeter/Voltage Source Reference Manual. March 2011. Rev. B edn. Cleveland, Ohio, U.S.A.: Keithley.

Technology Roadmap for NAND Flash memory. April 2014. techinsights.

Technology Roadmap for NAND Flash memory. April 2013. techinsights.

Nanoelectronics and Information Technology. 2012. 3rd edn. Germany: Wiley-VCH.

COMSOL Multiphysics 4.2a. 2011.

AKINAGA, H. and SHIMA, H., 2010. Resistive random access memory (ReRAM) based on metal oxides. *Proceedings of the IEEE,* **98**(12), pp. 2237-2251.

AMMERAHL, U. and REVCOLEVSCHI, A., 1999. Crystal growth of the spin-ladder compound (Ca,La)14Cu24O41 and observation of one-dimensional disorder. *Journal of Crystal Growth,* **197**(4), pp. 825-832.

AN, Y.-., RYU, K., JUNG, D.-., WOO, S.-. and JUNG, S.-., 2014. An energy efficient time-domain temperature sensor for low-power on-chip thermal management. *IEEE Sensors Journal,* **14**(1), pp. 104-110.

ANANDAN, S.S. and RAMALINGAM, V., 2008. Thermal management of electronics: A review of literature. *Thermal Science,* **12**(2), pp. 5-25.

ANDRIYEVSKY, B., DOLL, K. and JACOB, T., 2014. Electronic and transport properties of LiCoO2. *Physical Chemistry Chemical Physics,* **16**(42), pp. 23412-23420.

ANTOLINI, E., 2004. LiCoO2: Formation, structure, lithium and oxygen nonstoichiometry, electrochemical behaviour and transport properties. *Solid State Ionics,* **170**(3-4), pp. 159-171.

ARIEL, N., CEDER, G., SADOWAY, D.R. and FITZGERALD, E.A., 2005. Electrochemically controlled transport of lithium through ultrathin SiO 2. *Journal of Applied Physics,* **98**(2).

ARIEL, N., ISAACSON, D.M. and FITZGERALD, E.A., 2006. Microelectronically fabricated LiCoO 2/SiO 2/polycrystalline-silicon power cells planarized by chemical mechanical polishing. *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures,* **24**(2), pp. 562-569.

ATHANASOPOULOS, G.I., PERVOLARAKI, M., SVOUKIS, E., ANDROULAKIS, J., SAINT-MARTIN, R., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2011. Pulsed laser deposition and thermal characterization of Ni-doped La5Ca9Cu24O41 thin films. *Applied Surface Science,* **257**(12), pp. 5200-5203.

CHARIS ORFANIDOU

ATHANASOPOULOS, G.I., SVOUKIS, E., PERVOLARAKI, M., SAINT-MARTIN, R., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2010. Thermal conductivity of Ni, Co, and Fe-doped La5Ca 9Cu24O41 thin films measured by the 3ω method. *Thin Solid Films,* **518**(16), pp. 4684-4687.

AULNETTE, C., SCHWARZENBACH, W., DAVAL, N., BONNIN, O., NGUYEN, B.-., MAZURE, C., MALEVILLE, C., CHENG, K., PONOTH, S., KHAKIFIROOZ, A., HOOK, T. and DORIS, B., 2011. Ultra-thin SOI for 20nm node and beyond, *Proceedings - IEEE International SOI Conference* 2011.

BACHMANN, C. and BAR-COHEN, A., 2008. Hotspot remediation with anisotropic thermal interface materials, *2008 11th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, I-THERM*2008, pp. 238-247.

BAKER, C.A., GREEN, K., VAN DER GRINTEN, M.G.D., IAYDJIEV, P.S., IVANOV, S.N., AL-AYOUBI, S., HARRIS, P.G., PENDLEBURY, J.M., SHIERS, D.B. and GELTENBORT, P., 2002. Development of solid-state silicon devices as ultra cold neutron detectors. *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* **487**(3), pp. 511-520.

BALANDIN, A.A., 2015. Graphene heat spreaders and interconnects for advanced electronic applications, *ECS Transactions* 2015, pp. 167-172.

BALL, P., 2012. Computer engineering: Feeling the heat. *Nature,* **492**(7428), pp. 174-176.

BANKS, J., CARSON, J.S. and NELSON, B.L., 1996. *Discrete-Event System Simulation.* 2nd edn. London UK: Prentice Hall.

BARLETTA, P., VICK, E., BALDASARO, N. and TEMPLE, D., 2016. Highly integrated thermoelectric coolers, *Proceedings of the 15th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITherm 2016* 2016, pp. 1477-1481.

BATHE, K.J., 1976. *Numerical methods in finite element analysis.* Prentice Hall.

BENEŠ, V.E., 1964. Permutation Groups, Complexes, and Rearrangeable Connecting Networks. *Bell System Technical Journal,* **43**(4), pp. 1619-1640.

BEZ, R., CAMERLENGHI, E., MODELLI, A. and VISCONTI, A., 2003. Introduction to flash memory. *Proceedings of the IEEE,* **91**(4), pp. 489-501.

BRUNS, G., MERKELBACH, P., SCHLOCKERMANN, C., SALINGA, M., WUTTIG, M., HAPP, T.D., PHILIPP, J.B. and KUND, M., 2009. Nanosecond switching in GeTe phase change memory cells. *Applied Physics Letters,* **95**(4).

BURR, G.W., BREITWISCH, M.J., FRANCESCHINI, M., GARETTO, D., GOPALAKRISHNAN, K., JACKSON, B., KURDI, B., LAM, C., LASTRAS, L.A., PADILLA, A., RAJENDRAN, B., RAOUX, S. and SHENOY, R.S., 2010. Phase change memory technology. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics,* **28**(2), pp. 223-262.

BURZO, M.G., RAAD, P.E., LEE, T. and KOMAROV, P.L., 2012. Thermal conductivity measurements of novel SOI films using submicron thermography and transient thermoreflectance, *Annual IEEE Semiconductor Thermal Measurement and Management Symposium* 2012, pp. 150-156.

CHARIS ORFANIDOU

CAHILL, D.G., BRAUN, P.V., CHEN, G., CLARKE, D.R., FAN, S., GOODSON, K.E., KEBLINSKI, P., KING, W.P., MAHAN, G.D., MAJUMDAR, A., MARIS, H.J., PHILLPOT, S.R., POP, E. and SHI, L., 2014. Nanoscale thermal transport. II. 2003-2012. *Applied Physics Reviews,* **1**(1).

CENGEL, Y.A., 2002. *Heat Transfer - A practical Approach.* 2nd edn. New Delhi: Tata McGraw-Hill.

CHAPPERT, C., FERT, A. and VAN DAU, F.N., 2007. The emergence of spin electronics in data storage. *Nature Materials,* **6**(11), pp. 813-823.

CHASKALOVIC, J., 2008. *Finite Elements Methods for Engineering Sciences.* Springer Verlag.

CHENG, K. and KHAKIFIROOZ, A., 2016. Fully depleted SOI (FDSOI) technology. *Science China Information Sciences,* **59**(6).

CHENG, K., KHAKIFIROOZ, A., KULKARNI, P., PONOTH, S., HARAN, B., KUMAR, A., ADAM, T., REZNICEK, A., LOUBET, N., HE, H., KUSS, J., WANG, M., LEVIN, T.M., MONSIEUR, F., LIU, Q., SREENIVASAN, R., CAI, J., KIMBALL, A., MEHTA, S., LUNING, S., ZHU, Y., ZHU, Z., YAMAMOTO, T., BRYANT, A., LIN, C.-., NACZAS, S., JAGANNATHAN, H., EDGE, L.F., ALLEGRET-MARET, S., DUBE, A., KANAKASABAPATHY, S., SCHMITZ, S., INADA, A., SEO, S., RAYMOND, M., ZHANG, Z., YAGISHITA, A., DEMAREST, J., LI, J., HOPSTAKEN, M., BERLINER, N., UPHAM, A., JOHNSON, R., HOLMES, S., STANDAERT, T., SMALLEY, M., ZAMDMER, N., REN, Z., WU, T., BU, H., PARUCHURI, V., SADANA, D., NARAYANAN, V., HAENSCH, W., O'NEILL, J., HOOK, T., KHARE, M. and DORIS, B., 2011. ETSOI CMOS for system-on-chip applications featuring 22nm gate length, sub-100nm gate pitch, and 0.08µm2 SRAM cell, *IEEE Symposium on VLSI Circuits, Digest of Technical Papers* 2011, pp. 128-129.

CHER, C.-. and KURSUN, E., 2011. Exploring the effects of on-chip thermal variation on high-performance multicore architectures. *Transactions on Architecture and Code Optimization,* **8**(1).

CHO, E.-., CHANG-JIAN, C.-., HSIAO, Y.-., LEE, K.-. and HUANG, J.-., 2016. Three-dimensional carbon nanotube based polymer composites for thermal management. *Composites Part A: Applied Science and Manufacturing,* **90**, pp. 678-686.

CHO, J., LOSEGO, M.D., ZHANG, H.G., KIM, H., ZUO, J., PETROV, I., CAHILL, D.G. and BRAUN, P.V., 2014. Electrochemically tunable thermal conductivity of lithium cobalt oxide. *Nature Communications,* **5**.

CHOWDHURY, I., PRASHER, R., LOFGREEN, K., CHRYSLER, G., NARASIMHAN, S., MAHAJAN, R., KOESTER, D., ALLEY, R. and VENKATASUBRAMANIAN, R., 2009. On-chip cooling by superlattice-based thin-film thermoelectrics. *Nature Nanotechnology,* **4**(4), pp. 235-238.

CYFERZ, September 2016a-last update, Magnetoresistive random-access memory. Available: https://en.wikipedia.org/wiki/Magnetoresistive_random-access_memory.

CYFERZ, September 2016b-last update, Phase-change memory. Available: https://en.wikipedia.org/wiki/Phase-change_memory.

CYFERZ, October 2016-last update, Flash memory. Available: https://en.wikipedia.org/wiki/Flash_memory.

CYFERZ, August 2016-last update, Ferroelectric RAM. Available: https://en.wikipedia.org/wiki/Ferroelectric_RAM.

CHALMERS OPEN SESAME DOU

DAHÉRON, L., DEDRYVÈRE, R., MARTINEZ, H., MÉNÉTRIER, M., DENAGE, C., DELMAS, C. and GONBEAU, D., 2008. Electron transfer mechanisms upon lithium deintercalation from LiCoO2to CoO2investigated by XPS. *Chemistry of Materials,* **20**(2), pp. 583-590.

DAHL, O.-. and NYGAARD, K., 1966. SIMULA: An ALGOL-based simulation language. *Communications of the ACM,* **9**(9), pp. 671-678.

DIJKKAMP, D., VENKATESAN, T., WU, X.D., SHAHEEN, S.A., JISRAWI, N., MIN-LEE, Y.H., MCLEAN, W.L. and CROFT, M., 1987. Preparation of Y-Ba-Cu oxide superconductor thin films using pulsed laser evaporation from high Tc bulk material. *Applied Physics Letters,* **51**(8), pp. 619-621.

DITTMANN, R., MUENSTERMANN, R., KRUG, I., PARK, D., MENKE, T., MAYER, J., BESMEHN, A., KRONAST, F., SCHNEIDER, C.M. and WASER, R., 2012. Scaling potential of local redox processes in memristive SrTiO3thin-film devices. *Proceedings of the IEEE,* **100**(6), pp. 1979-1990.

ESAKI, L., LAIBOWITZ, R.B. and STILES, P.J., 1971. Polar switch. *IBM Tech.Discl.Bull.,* **13**.

FUJISAKI, Y., 2010. Current status of nonvolatile semiconductor memory technology. *Japanese Journal of Applied Physics,* **49**(10), pp. 1000011-1000014.

GARCIA, B., FARCY, J., PEREIRA-RAMOS, J.P. and BAFFIER, N., 1997. Electrochemical properties of low temperature crystallized LiCoO2. *Journal of the Electrochemical Society,* **144**(4), pp. 1179-1184.

GLASSBRENNER, C.J. and SLACK, G.A., 1964. Thermal conductivity of silicon and germanium from 3°K to the melting point. *Physical Review,* **134**(4A).

GOTOH, Y., YAMAGUCHI, I., TAKAHASHI, Y., AKIMOTO, J., GOTO, M., ONODA, M., FUJINO, H., NAGATA, T. and AKIMITSU, J., 2003. Structural modulation, hole distribution, and hole-ordered structure of the incommensurate composite crystal (Sr2Cu2O 3)0.70CuO2. *Physical Review B - Condensed Matter and Materials Physics,* **68**(22), pp. 2241081-22410815.

HA, S.D. and RAMANATHAN, S., 2011. Adaptive oxide electronics: A review. *Journal of Applied Physics,* **110**(7).

HARON, N.Z. and HAMDIOUI, S., 2008. Why is CMOS scaling coming to an END? *Proceedings - 2008 3rd International Design and Test Workshop, IDT 2008* 2008, pp. 98-103.

HART, F.X. and BATES, J.B., 1998. Lattice model calculation of the strain energy density and other properties of crystalline LiCoO2. *Journal of Applied Physics,* **83**(12), pp. 7560-7566.

HARTREE, D.R., 1946. The ENIAC, an electronic computing machine. *Nature,* **158**(4015), pp. 500-506.

HENKEL, J., EBI, T., AMROUCH, H. and KHDR, H., 2013. Thermal management for dependable on-chip systems, *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC* 2013, pp. 113-118.

HERTZ, J.T., HUANG, Q., MCQUEEN, T., KLIMCZUK, T., BOS, J.W.G., VICIU, L. and CAVA, R.J., 2008. Magnetism and structure of Lix Co O2 and comparison to Nax Co O2. *Physical Review B - Condensed Matter and Materials Physics,* **77**(7).

CHARIS ORFANIDOU

HESS, C., BAUMANN, C., AMMERAHL, U., BÜCHNER, B., HEIDRICH-MEISNER, F., BRENIG, W. and REVCOLEVSCHI, A., 2001. Magnon heat transport in (Sr, Ca, La)14Cu24O41. *Physical Review B - Condensed Matter and Materials Physics,* **64**(18), pp. 1843051-1843056.

HICKMOTT, T.W., 1962. Low-frequency negative resistance in thin anodic oxide films. *Journal of Applied Physics,* **33**(9), pp. 2669-2682.

HOANG, K. and JOHANNES, M.D., 2014. Defect chemistry in layered transition-metal oxides from screened hybrid density functional calculations. *Journal of Materials Chemistry A,* **2**(15), pp. 5224-5235.

HYDRARGYRUM, October 2016-last update, X-ray crystallography.
Available: https://en.wikipedia.org/wiki/X-ray_crystallography.

IELMINI, D., 2016. Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling. *Semiconductor Science and Technology,* **31**(6).

IELMINI, D., 2009a. Reliability issues and modeling of Flash and post-Flash memory (Invited Paper). *Microelectronic Engineering,* **86**(7-9), pp. 1870-1875.

IELMINI, D. and BONIARDI, M., 2009b. Common signature of many-body thermal excitation in structural relaxation and crystallization of chalcogenide glasses. *Applied Physics Letters,* **94**(9).

IELMINI, D., BRUCHHAUS, R. and WASER, R., 2011. Thermochemical resistive switching: Materials, mechanisms, and scaling projections. *Phase Transitions,* **84**(7), pp. 570-602.

IELMINI, D., SHARMA, D., LAVIZZARI, S. and LACAITA, A.L., 2009c. Reliability impact of chalcogenide-structure relaxation in phase-change memory (PCM) cells-Part I: Experimental study. *IEEE Transactions on Electron Devices,* **56**(5), pp. 1070-1077.

IELMINI, D. and ZHANG, Y., 2007. Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices. *Journal of Applied Physics,* **102**(5).

INTEL(R), 2016. *Intel (R) 64 and IA-32 Architectures Software Developer's Manual.* Intel.

ISHIDA, Y., MIZUTANI, A., SUGIURA, K., OHTA, H. and KOUMOTO, K., 2010. Metal-nonmetal transition in Lix CoO2 thin films and thermopower enhancement at high Li concentration. *Physical Review B - Condensed Matter and Materials Physics,* **82**(7).

JEONG, D.S., SCHROEDER, H. and WASER, R., 2009. Mechanism for bipolar switching in a Pt/ TiO2 /Pt resistive switching cell. *Physical Review B - Condensed Matter and Materials Physics,* **79**(19).

JEONG, D.S., THOMAS, R., KATIYAR, R.S., SCOTT, J.F., KOHLSTEDT, H., PETRARU, A. and HWANG, C.S., 2012. Emerging memories: Resistive switching mechanisms and current status. *Reports on Progress in Physics,* **75**(7).

JEPPSON, K., BAO, J., HUANG, S., ZHANG, Y., SUN, S., FU, Y. and LIU, J., 2016. Hotspot test structures for evaluating carbon nanotube microfin coolers and graphene-like heat spreaders, *IEEE International Conference on Microelectronic Test Structures* 2016, pp. 32-36.

JIMÉNEZ, V., GIOIOSA, R., KURSUN, E., CAZORLA, F.J., CHER, C.-., BUYUKTOSUNOGLU, A., BOSE, P. and VALERO, M., 2010. Trends and techniques for energy

CHARIS ORFANIDOU

efficient architectures, *Proceedings of the 2010 18th IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC 2010* 2010, pp. 276-279.

JO, S.H., KIM, K.-. and LU, W., 2009. High-density crossbar arrays based on a Si memristive system. *Nano Letters,* **9**(2), pp. 870-874.

JUNQUERA, J. and GHOSEZ, P., 2003. Critical thickness for ferroelectricity in perovskite ultrathin films. *Nature,* **422**(6931), pp. 506-509.

KANAMORI, J., 1959. Superexchange interaction and symmetry properties of electron orbitals. *Journal of Physics and Chemistry of Solids,* **10**(2-3), pp. 87-98.

KANG, S.G., KANG, S.Y., RYU, K.S. and CHANG, S.H., 1999. Electrochemical and structural properties of HT-LiCoO2 and LT-LiCoO2 prepared by the citrate sol-gel method. *Solid State Ionics,* **120**(1), pp. 155-161.

KANG, S.-., WEI, W.-., TSAI, S.-. and YANG, S.-., 2006. Experimental investigation of silver nano-fluid on heat pipe thermal performance. *Applied Thermal Engineering,* **26**(17-18), pp. 2377-2382.

KAVEHEI, O., 2011. *Memristive Devices and Circuits for Computing, Memory, and Neuromorphic Applications*, University of Adelaide.

KENT, A.D. and WORLEDGE, D.C., 2015. A new spin on magnetic memories. *Nature Nanotechnology,* **10**(3), pp. 187-191.

KHAKIFIROOZ, A., CHENG, K., LIU, Q., NAGUMO, T., LOUBET, N., REZNICEK, A., KUSS, J., GIMBERT, J., SREENIVASAN, R., VINET, M., GRENOUILLET, L., LE TIEC, Y., WACQUEZ, R., REN, Z., CAI, J., SHAHRJERDI, D., KULKARNI, P., PONOTH, S., LUNING, S. and DORIS, B., 2012. Extremely thin SOI for system-on-chip applications, *Proceedings of the Custom Integrated Circuits Conference* 2012.

KHAKIFIROOZ, A., CHENG, K., REZNICEK, A., ADAM, T., LOUBET, N., HE, H., KUSS, J., LI, J., KULKARNI, P., PONOTH, S., SREENIVASAN, R., LIU, Q., DORIS, B. and SHAHIDI, G., 2012. Scalability of extremely thin SOI (ETSOI) MOSFETs to sub-20-nm gate length. *IEEE Electron Device Letters,* **33**(2), pp. 149-151.

KIM, K. and KOH, G.-., 2004. Future memory technology including emerging new memories, *Proceedings of the International Conference on Microelectronics* 2004, pp. 377-384.

KITTEL, C., 2005. *Introduction to solid state physics.* 8th edn. John Wiley & Sons, pp. 503-506.

KULKARNI, P., LIU, Q., KHAKIFIROOZ, A., ZHANG, Y., CHENG, K., MONSIEUR, F. and OLDIGES, P., 2011. Impact of substrate bias on GIDL for thin-BOX ETSOI devices, *International Conference on Simulation of Semiconductor Processes and Devices, SISPAD* 2011, pp. 103-106.

KURSUN, E. and CHER, C.-., 2009. Temperature variation characterization and thermal management of multicore architectures. *IEEE Micro,* **29**(1), pp. 116-126.

KUTBEE, A.T., GHONEIM, M.T., AHMAD, S.M. and HUSSAIN, M.M., 2016. Free-form flexible lithium-ion microbattery. *IEEE Transactions on Nanotechnology,* **15**(3), pp. 402-408.

LAVIZZARI, S., IELMINI, D., SHARMA, D. and LACAITA, A.L., 2009. Reliability impact of chalcogenide-structure relaxation in phase-change memory (PCM) cells-Part II: Physics-Based Modeling. *IEEE Transactions on Electron Devices,* **56**(5), pp. 1078-1085.

CHARIS ORFANIDOU

LEVASSEUR, S., MÉNÉTRIER, M., SUARD, E. and DELMAS, C., 2000. Evidence for structural defects in non-stoichiometric HT-LiCoO2: electrochemical, electronic properties and 7Li NMR studies. *Solid State Ionics,* **128**(1-4), pp. 11-24.

LIN, S.-. and BANERJEE, K., 2008. Cool chips: Opportunities and implications for power and thermal management. *IEEE Transactions on Electron Devices,* **55**(1), pp. 245-255.

LINN, E., ROSEZIN, R., KÜGELER, C. and WASER, R., 2010. Complementary resistive switches for passive nanocrossbar memories. *Nature Materials,* **9**(5), pp. 403-406.

LU, W. and LIEBER, C.M., 2007. Nanoelectronics from the bottom up. *Nature Materials,* **6**(11), pp. 841-850.

MAHAJAN, R., CHIU, C.-. and CHRYSLER, G., 2006. Cooling a microprocessor chip. *Proceedings of the IEEE,* **94**(8), pp. 1476-1485.

MAHAJAN, S.S., SUBBARAYAN, G. and SAMMAKIA, B.G., 2008. Estimating Kapitza resistance between Si-SiO2 interface using molecular dynamics simulations, *2008 11th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, I-THERM* 2008, pp. 1055-1062.

MAI, V.H., MORADPOUR, A., SENZIER, P.A., PASQUIER, C., WANG, K., ROZENBERG, M.J., GIAPINTZAKIS, J., MIHAILESCU, C.N., ORFANIDOU, C.M., SVOUKIS, E., BREZA, A., LIOUTAS, C.B., FRANGER, S., REVCOLEVSCHI, A., MAROUTIAN, T., LECOEUR, P., AUBERT, P., AGNUS, G., SALOT, R., ALBOUY, P.A., WEIL, R., ALAMARGUY, D., MARCH, K., JOMARD, F., CHRÉTIEN, P. and SCHNEEGANS, O., 2015. Memristive and neuromorphic behavior in a Li x CoO 2 nanobattery. *Scientific Reports,* **5**.

MAJUMDAR, A., REN, Z., KOESTER, S.J. and HAENSCH, W., 2009. Undoped-body extremely thin SOI MOSFETs with back gates. *IEEE Transactions on Electron Devices,* **56**(10), pp. 2270-2276.

MAJUMDAR, A., REN, Z., SLEIGHT, J.W., DOBUZINSKY, D., HOLT, J.R., VENIGALLA, R., KOESTER, S.J. and HAENSCH, W., 2008. High-performance undoped-body 8-nm-thin SOI field-effect transistors. *IEEE Electron Device Letters,* **29**(5), pp. 515-517.

MAJUMDAR, A., WANG, X., KUMAR, A., HOLT, J.R., DOBUZINSKY, D., VENIGALLA, R., OUYANG, C., KOESTER, S.J. and HAENSCH, W., 2009. Gate length and performance scaling of undoped-body extremely thin SOI MOSFETs. *IEEE Electron Device Letters,* **30**(4), pp. 413-415.

MALVIYA, A.K. and CHAUHAN, R.K., 2018. Analysis of source/drain engineered 22nm FDSOI using high-k spacers, *AIP Conference Proceedings* 2018.

MARIANETTI, C.A., KOTLIAR, G. and CEDER, G., 2004. A first-order Mott transition in LixCoO2. *Nature Materials,* **3**(9), pp. 627-631.

MARSCHEWSKI, J., BRECHBÜHLER, R., JUNG, S., RUCH, P., MICHEL, B. and POULIKAKOS, D., 2016. Significant heat transfer enhancement in microchannels with herringbone-inspired microstructures. *International Journal of Heat and Mass Transfer,* **95**, pp. 755-764.

MARSCHEWSKI, J., JUNG, S., RUCH, P., PRASAD, N., MAZZOTTI, S., MICHEL, B. and POULIKAKOS, D., 2015. Mixing with herringbone-inspired microstructures: Overcoming the diffusion limit in co-laminar microfluidic devices. *Lab on a Chip - Miniaturisation for Chemistry and Biology,* **15**(8), pp. 1923-1933.

CHARIS ORFANIDOU

MASUOKA, F., MOMODOMI, M., IWATA, Y. and SHIROTA, R., 1987. NEW ULTRA HIGH DENSITY EPROM AND FLASH EEPROM WITH NAND STRUCTURE CELL. *Technical Digest - International Electron Devices Meeting* 1987, pp. 552-555.

MAY, G.S. and SPANOS, C.J., 2006. *Fundamentals of semiconductor manufacturing and process control.* John Wiley & Sons, pp. 30-31.

MCCARRON III, E.M., SUBRAMANIAN, M.A., CALABRESE, J.C. and HARLOW, R.L., 1988. The incommensurate structure of (Sr14-xCax)Cu24O41 (0 < x ~ 8) a superconductor byproduct. *Materials Research Bulletin,* **23**(9), pp. 1355-1365.

MEIJER, G.I., STAUB, U., JANOUSCH, M., JOHNSON, S.L., DELLEY, B. and NEISIUS, T., 2005. Valence states of Cr and the insulator-to-metal transition in Cr-doped SrTiO3. *Physical Review B - Condensed Matter and Materials Physics,* **72**(15).

MÉNÉTRIER, M., SAADOUNE, I., LEVASSEUR, S. and DELMAS, C., 1999. The insulator-metal transition upon lithium deintercalation from LiCoO2: Electronic properties and 7Li NMR study. *Journal of Materials Chemistry,* **9**(5), pp. 1135-1140.

MERKEL, C.E. and KUDITHIPUDI, D., 2014. Temperature sensing RRAM architecture for 3-D ICss. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* **22**(4), pp. 878-887.

MIZUSHIMA, K., JONES, P.C., WISEMAN, P.J. and GOODENOUGH, J.B., 1980. LixCoO2 (0<x<-1): A new cathode material for batteries of high energy density. *Materials Research Bulletin,* **15**(6), pp. 783-789.

MOLENDA, J., STOKLOSA, A. and BA¸K, T., 1989. Modification in the electronic structure of cobalt bronze LixCoO2 and the resulting electrochemical properties. *Solid State Ionics,* **36**(1-2), pp. 53-58.

MOODERA, J.S., KINDER, L.R., WONG, T.M. and MESERVEY, R., 1995. Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions. *Physical Review Letters,* **74**(16), pp. 3273-3276.

MORADPOUR, A., SCHNEEGANS, O., FRANGER, S., REVCOLEVSCHI, A., SALOT, R., AUBAN-SENZIER, P., PASQUIER, C., SVOUKIS, E., GIAPINTZAKIS, J., DRAGOS, O., CIOMAGA, V.-. and CHRÉTIEN, P., 2011. Resistive switching phenomena in Li xCoO 2 thin films. *Advanced Materials,* **23**(36), pp. 4141-4145.

MORIN, P., MAITREJEAN, S., ALLIBERT, F., AUGENDRE, E., LIU, Q., LOUBET, N., GRENOUILLET, L., POFELSKI, A., CHEN, K., KHAKIFIROOZ, A., WACQUEZ, R., REBOH, S., BONNEVIALLE, A., LE ROYER, C., MORAND, Y., KANYANDEKWE, J., CHANEMOUGAMME, D., MIGNOT, Y., ESCARABAJAL, Y., LHERRON, B., CHAFIK, F., PILORGET, S., CAUBET, P., VINET, M., CLEMENT, L., DESALVO, B., DORIS, B. and KLEEMEIER, W., 2016. A review of the mechanical stressors efficiency applied to the ultra-thin body & buried oxide fully depleted silicon on insulator technology. *Solid-State Electronics,* **117**, pp. 100-116.

MUENSTERMANN, R., MENKE, T., DITTMANN, R. and WASER, R., 2010. Coexistence of filamentary and homogeneous resistive switching in Fe-doped SrTiO3 thin-film memristive devices. *Advanced Materials,* **22**(43), pp. 4819-4822.

NGUYEN, V.S., MAI, V.H., AUBAN SENZIER, P., PASQUIER, C., WANG, K., ROZENBERG, M.J., BRUN, N., MARCH, K., JOMARD, F., GIAPINTZAKIS, J., MIHAILESCU, C.N., KYRIAKIDES, E., NUKALA, P., MAROUTIAN, T., AGNUS, G., LECOEUR, P., MATZEN, S., AUBERT, P., FRANGER, S., SALOT, R., ALBOUY, P.-., ALAMARGUY, D., DKHIL, B.,

CHRIS ORFANIDOU

CHRÉTIEN, P. and SCHNEEGANS, O., 2018. Direct Evidence of Lithium Ion Migration in Resistive Switching of Lithium Cobalt Oxide Nanobatteries. *Small,* **14**(24).

ORFANIDOU, C.M. and GIAPINTZAKIS, J., 2013. Heat channeling in extremely thin silicon-on-insulator devices: A simulation study. *IEEE Transactions on Electron Devices,* **60**(10), pp. 3330-3334.

ORFANIDOU, C.M., IOANNOU, P.S., KYRIAKIDES, E., NICOLAOU, C., MIHAILESCU, C.N., NGUYEN, V.S., MAI, V.H., SCHNEEGANS, O. and GIAPINTZAKIS, J., 2018. Stoichiometry and volume dependent transport in lithium ion memristive devices. *AIP Advances,* **8**(11).

OTTER, M., 2012.
Magnetic heat transport in low-dimensional quantum magnets, University of Groningen.

OTTER, M., ATHANASOPOULOS, G., HLUBEK, N., MONTAGNESE, M., LABOIS, M., FISHMAN, D.A., DE HAAN, F., SINGH, S., LAKEHAL, D., GIAPINTZAKIS, J., HESS, C., REVCOLEVSCHI, A. and VAN LOOSDRECHT, P.H.M., 2012. Optical probing of anisotropic heat transport in the quantum spin ladder Ca 9La 5Cu 24O 41. *International Journal of Heat and Mass Transfer,* **55**(9-10), pp. 2531-2538.

OTTER, M., KRASNIKOV, V.V., FISHMAN, D.A., PSHENICHNIKOV, M.S., SAINT-MARTIN, R., REVCOLEVSCHI, A. and VAN LOOSDRECHT, P.H.M., 2009. Heat transport imaging in the spin-ladder compound Ca9La5Cu24O41. *Journal of Magnetism and Magnetic Materials,* **321**(7), pp. 796-799.

OUYANG, J., CHU, C.-., SZMANDA, C.R., MA, L. and YANG, Y., 2004. Programmable polymer thin film and non-volatile memory device. *Nature Materials,* **3**(12), pp. 918-922.

OVSHINSKY, S.R., 1968. Reversible electrical switching phenomena in disordered structures. *Physical Review Letters,* **21**(20), pp. 1450-1453.

PEDRAM, M. and NAZARIAN, S., 2006. Thermal modeling, analysis, and management in VLSI circuits: Principles and methods. *Proceedings of the IEEE,* **94**(8), pp. 1487-1501.

PERVOLARAKI, M., ATHANASOPOULOS, G.I., SAINT-MARTIN, R., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2009. KrF pulsed laser deposition of La5Ca9Cu24O41 thin films on various substrates. *Applied Surface Science,* **255**(10), pp. 5236-5239.

PERVOLARAKI, M., PASUK, I., STAN, G.E. and GIAPINTZAKIS, J., 2012. Pulsed laser deposition of highly textured La 5Ca 9Cu 24O 41 films on SrLaAlO 4 (1 0 0) and Gd 3Ga 5O 12 (1 0 0) substrates. *Applied Surface Science,* **258**(23), pp. 9475-9479.

PERVOLARAKI, M., SINGH, S., ATHANASOPOULOS, G.I., SAINT-MARTIN, R., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2010. Pulsed laser deposition of homo- and hetero-epitaxial thin films of the exotic La5Ca9Cu24O41 compound on oxide and Si substrates. *Journal of Optoelectronics and Advanced Materials,* **12**(3), pp. 641-645.

PIROVANO, A., LACAITA, A.L., BENVENUTI, A., PELLIZZER, F. and BEZ, R., 2004. Electronic Switching in Phase-Change Memories. *IEEE Transactions on Electron Devices,* **51**(3), pp. 452-459.

POP, E., CHUI, C.O., SINHA, S., DUTTON, R. and GOODSON, K., 2004. Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs, *Technical Digest - International Electron Devices Meeting, IEDM*2004, pp. 411-414.

CHARIS ORFANIDOU

POP, E., SINHA, S. and GOODSON, K.E., 2006. Heat generation and transport in nanometer-scale transistors. *Proceedings of the IEEE,* **94**(8), pp. 1587-1601.

POP, E., VARSHNEY, V. and ROY, A.K., 2012. Thermal properties of graphene: Fundamentals and applications. *MRS Bulletin,* **37**(12), pp. 1273-1281.

PUBLIC DOMAIN, October 2016-last update, Sputter deposition.
Available: https://en.wikipedia.org/wiki/Sputter_deposition.

RAOUX, S., BURR, G.W., BREITWISCH, M.J., RETTNER, C.T., CHEN, Y.-., SHELBY, R.M., SALINGA, M., KREBS, D., CHEN, S.-., LUNG, H.-. and LAM, C.H., 2008. Phase-change random access memory: A scalable technology. *IBM Journal of Research and Development,* **52**(4-5), pp. 465-479.

RAOUX, S., WELNIC, W. and LELMINI, D., 2010. Phase change materials and their application to nonvolatile memories. *Chemical reviews,* **110**(1), pp. 240-267.

REIMERS, J.N. and DAHN, J.R., 1993. Effects of Impurities on the Electrochemical Properties of LiCoO2. *Journal of the Electrochemical Society,* **140**(10), pp. 2752-2754.

ROSSEN, E., REIMERS, J.N. and DAHN, J.R., 1993. Synthesis and electrochemistry of spinel LTLiCoO2. *Solid State Ionics,* **62**(1-2), pp. 53-60.

ROZENBERG, M.J., INOUE, I.H. and SÁNCHEZ, M.J., 2004. Nonvolatile memory with multilevel switching: A basic model. *Physical Review Letters,* **92**(17), pp. 178302-1.

SAH, C.-., 1967. The Equivalent Circuit Model in Solid-State Electronics—Part I: The Single Energy Level Defect Centers. *Proceedings of the IEEE,* **55**(5), pp. 654-671.

SAH, C.-., NOYCE, R.N. and SHOCKLEY, W., 1957. Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics. *Proceedings of the IRE,* **45**(9), pp. 1228-1243.

SAMPEDRO, C., GÁMIZ, F. and GODOY, A., 2013. On the extension of ET-FDSOI roadmap for 22 nm node and beyond. *Solid-State Electronics,* **90**, pp. 23-27.

SAWA, A., 2008. Resistive switching in transition metal oxides. *Materials Today,* **11**(6), pp. 28-36.

SCHMIDT, R.R., CRUZ, E.E. and IYENGAR, M.K., 2005. Challenges of data center thermal management. *IBM Journal of Research and Development,* **49**(4-5), pp. 709-723.

SEMENOV, O., VASSIGHI, A. and SACHDEV, M., 2006. Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits. *IEEE Transactions on Device and Materials Reliability,* **6**(1), pp. 17-27.

SHACKELFORD, J.F. and ALEXANDER, W., 2001.
Selecting thermal properties
Materials Science and Engineering Handbook 3rd edn. FL, USA: Boca Raton CRC Press.

SHAHIDI, G.G., 2013. From 2D-planar to 3D-non-planar device architecture: A scalable path forward? *Proceedings of the Custom Integrated Circuits Conference* 2013.

SHAHIDI, G.G., 2006. Are we at the end of CMOS scaling? *International Journal of High Speed Electronics and Systems,* **16**(1), pp. 3-8.

CHARIS ORFANIDOU

SHAHIDI, G.G., 2002. SOI technology for the GHz era. *IBM Journal of Research and Development,* **46**(2-3), pp. 121-131.

SHAHIL, K.M.F. and BALANDIN, A.A., 2012. Thermal properties of graphene and multilayer graphene: Applications in thermal interface materials. *Solid State Communications,* **152**(15), pp. 1331-1340.

SHAMSA, M., SOLOMON, P.M., JENKINS, K.A., BALANDIN, A.A. and HAENSCH, W., 2008. Investigation of thermal crosstalk between SOI FETs by the subthreshold sensing technique. *IEEE Transactions on Electron Devices,* **55**(7), pp. 1733-1740.

SHAO-HORN, Y., CROGUENNEC, L., DELMAS, C., NELSON, E.C. and O'KEEFE, M.A., 2003. Atomic resolution of lithium ions in LiCoO2. *Nature Materials,* **2**(7), pp. 464-467.

SHIBUYA, M., NISHINA, T., MATSUE, T. and UCHIDA, I., 1996. In situ conductivity measurements of LiCoO2film during lithium insertion/extraction by using interdigitated microarray electrodes. *Journal of the Electrochemical Society,* **143**(10), pp. 3157-3160.

SHIN, S.H., WAHAB, M.A., AHN, W., ZIABARI, A., MAIZE, K., SHAKOURI, A. and ALAM, M.A., 2016. Fundamental trade-off between short-channel control and hot carrier degradation in an extremely-thin silicon-on-insulator (ETSOI) technology, *Technical Digest - International Electron Devices Meeting, IEDM* 2016, pp. 20.3.1-20.3.4.

SHOCKLEY, W., 1952. A unipolar “field-effect” transistor*. *Proceedings of the IRE,* **40**(11), pp. 1365-1376.

SHOCKLEY, W., 1952. Transistor electronics: Imperfections, unipolar and analog transistors*. *Proceedings of the IRE,* **40**(11), pp. 1289-1313.

SHOCKLEY, W., 1949. The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors. *Bell System Technical Journal,* **28**(3), pp. 435-489.

SHRIVASTAVA, M., AGRAWAL, M., AGHASSI, J., GOSSNER, H., MOLZER, W., SCHULZ, T. and RAMGOPAL RAO, V., 2011. On the thermal failure in nanoscale devices: Insight towards heat transport including critical BEOL and design guidelines for robust thermal management & EOS/ESD reliability, *IEEE International Reliability Physics Symposium Proceedings* 2011.

SIEGRIST, T., SCHNEEMEYER, L.F., SUNSHINE, S.A., WASZCZAK, J.V. and ROTH, R.S., 1988. A new layered cuprate structure-type, (A1-xA'x)14Cu24O4 1. *Materials Research Bulletin,* **23**(10), pp. 1429-1438.

SIM, H., CHOI, H., LEE, D., CHANG, M., CHOI, D., SON, Y., LEE, E.-., KIM, W., PARK, Y., YOO, I.-. and HWANG, H., 2005. Excellent resistance switching characteristics of Pt/SrTiO3 schottky junction for multi-bit nonvolatile memory application, *Technical Digest - International Electron Devices Meeting, IEDM* 2005, pp. 758-761.

SIMPSON, R.E., KRBAL, M., FONS, P., KOLOBOV, A.V., TOMINAGA, J., URUGA, T. and TANIDA, H., 2010. Toward the ultimate limit of phase change in Ge2Sb 2Te5. *Nano Letters,* **10**(2), pp. 414-419.

SNIDER, G.S., 2008. Spike-timing-dependent learning in memristive nanodevices, *2008 IEEE/ACM International Symposium on Nanoscale Architectures, NANOARCH 2008* 2008, pp. 85-92.

SRIDHAR, A., VIRICENZI, A., RUGGIERO, M., BRUNSCHWILER, T. and ATIENZA, D., 2010. 3D-ICE: Fast compact transient thermal modeling for 3D ICs with inter-tier liquid

CHARIS ORFANIDOU

cooling, *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, ICCAD* 2010, pp. 463-470.

SU, L.T., CHUNG, J.E., DIMITRI, A.A., GOODSON, K.E. and FLIK, M.I., 1994. Measurement and Modeling of Self-Heating in SOI NMOSFET's. *IEEE Transactions on Electron Devices,* **41**(1), pp. 69-75.

SUBRINA, S., 2011.
Thermal Transport in Graphene Multilayers and Nanoribbons, University of California Riverside.

SUBRINA, S., KOTCHETKOV, D. and BALANDIN, A.A., 2009. Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders. *IEEE Electron Device Letters,* **30**(12), pp. 1281-1283.

SVOUKIS, E., ATHANASOPOULOS, G.I., ALTANTZIS, T., LIOUTAS, C., MARTIN, R.S., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2012. Structural and thermal characterization of La5Ca 9Cu24O41 thin films grown by pulsed laser deposition on (1 1 0) SrTiO3 substrates. *Thin Solid Films,* **520**(14), pp. 4613-4616.

SVOUKIS, E., ATHANASOPOULOS, G.I., MORADPOUR, A., SCHNEEGANS, O., REVCOLEVSCHI, A. and GIAPINTZAKIS, J., 2012. Growth and transport properties of HT-Li xCoO 2 thin films deposited by pulsed laser deposition. *Applied Surface Science,* **258**(23), pp. 9366-9369.

SZOT, K., SPEIER, W., BIHLMAYER, G. and WASER, R., 2006. Switching the electrical resistance of individual dislocations in single-crystalline SrTiO3. *Nature Materials,* **5**(4), pp. 312-320.

TAPPERTZHOFEN, S., VALOV, I., TSURUOKA, T., HASEGAWA, T., WASER, R. and AONO, M., 2013. Generic relevance of counter charges for cation-based nanoscale resistive switching memories. *ACS Nano,* **7**(7), pp. 6396-6402.

TERMAN, L.M., 1962. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid State Electronics,* **5**(5), pp. 285-299.

TONG, X.C., 2011. *Advanced Materials for Thermal Management of Electronic Packaging.* 1st edn. New York: Springer Series in Advanced Microelectronics.

VALOV, I., LINN, E., TAPPERTZHOFEN, S., SCHMELZER, S., VAN DEN HURK, J., LENTZ, F. and WASER, R., 2013. Nanobatteries in redox-based resistive switches require extension of memristor theory. *Nature Communications,* **4**.

VALOV, I., SAPEZANSKAIA, I., NAYAK, A., TSURUOKA, T., BREDOW, T., HASEGAWA, T., STAIKOV, G., AONO, M. and WASER, R., 2012. Atomically controlled electrochemical nucleation at superionic solid electrolyte surfaces. *Nature Materials,* **11**(6), pp. 530-535.

VALOV, I., WASER, R., JAMESON, J.R. and KOZICKI, M.N., 2011. Electrochemical metallization memories - Fundamentals, applications, prospects. *Nanotechnology,* **22**(25).

VASSIGHI, A. and SACHDEV, M., 2006. *Thermal and Power Management of Integrated Circuits.* New York: Springer-Verlag.

WANG, K., 2013. Laser Based Fabrication of Graphene. In: M. ALIOFKHAZRAEI, ed, *Advances in Graphene Science.* InTech.

CHARIS ORFANIDOU

WANG, B., BATES, J.B., HART, F.X., SALES, B.C., ZUHR, R.A. and ROBERTSON, J.D., 1996. Characterization of thin-film rechargeable lithium batteries with lithium cobalt oxide cathodes. *Journal of the Electrochemical Society,* **143**(10), pp. 3203-3213.

WANG, S., YIN, Y., HU, C. and REZAI, P., 2018. 3D integrated circuit cooling with microfluidics. *Micromachines,* **9**(6).

WASER, R., 2011. Redox-Based Resistive Switching Memories – the Mystery of Nanoionic Processes, *IEEE Internation Electron Device Meeting (IEDM)* 2011.

WASER, R. and AONO, M., 2007. Nanoionics-based resistive switching memories. *Nature Materials,* **6**(11), pp. 833-840.

WASER, R., DITTMANN, R., STAIKOV, C. and SZOT, K., 2009. Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges. *Advanced Materials,* **21**(25-26), pp. 2632-2663.

WONG, H.-.P., LEE, H.-., YU, S., CHEN, Y.-., WU, Y., CHEN, P.-., LEE, B., CHEN, F.T. and TSAI, M.-., 2012. Metal-oxide RRAM. *Proceedings of the IEEE,* **100**(6), pp. 1951-1970.

WUTTIG, M. and YAMADA, N., 2007. Phase-change materials for rewriteable data storage. *Nature Materials,* **6**(11), pp. 824-832.

XU, P., CHEN, Y., CHEN, Y., MIAO, L., SUN, S., KIM, S.-., BERGER, A., MAO, D., BENCHER, C., HUNG, R. and NGAI, C., 2011. Sidewall spacer quadruple patterning for 15nm half-pitch, *Proceedings of SPIE - The International Society for Optical Engineering* 2011.

YAN, Z., LIU, G., KHAN, J.M. and BALANDIN, A.A., 2012. Graphene quilts for thermal management of high-power GaN transistors. *Nature Communications,* **3**.

YANG, J.J., STRUKOV, D.B. and STEWART, D.R., 2013. Memristive devices for computing. *Nature Nanotechnology,* **8**(1), pp. 13-24.

YANG, Y., PARK, J., SONG, S.C., WANG, J., YEAP, G. and JUNG, S.-., 2015. SRAM Design for 22-nm ETSOI technology: Selective cell current boosting and asymmetric back-gate write-assist circuit. *IEEE Transactions on Circuits and Systems I: Regular Papers,* **62**(6), pp. 1538-1545.

YEH, W., LIN, C., CHOU, T., WU, K. and YUAN, J., 2015. The Impact of Junction Doping Distribution on Device Performance Variability and Reliability for Fully Depleted Silicon on Insulator with Thin Box Layer MOSFETs. *IEEE Transactions on Nanotechnology,* **14**(2), pp. 330-337.

YUEH, W., WAN, Z., JOSHI, Y. and MUKHOPADHYAY, S., 2016. Design, characterization, and application of a field-programmable thermal emulation platform. *IEEE Transactions on Components, Packaging and Manufacturing Technology,* **6**(9), pp. 1330-1339.

ZOTOS, X., NAEF, F. and PRELOVŠEK, P., 1997. Transport and conservation laws. *Physical Review B - Condensed Matter and Materials Physics,* **55**(17), pp. 11029-11032.

ZWERG, M., BAUMANN, A., KUHN, R., ARNOLD, M., NERLICH, R., HERZOG, M., LEDWA, R., SICHERT, C., RZEHAK, V., THANIGAI, P. and EVERSMANN, B.O., 2011. An 82µA/MHz microcontroller with embedded FeRAM for energy-harvesting applications, *Digest of Technical Papers - IEEE International Solid-State Circuits Conference* 2011, pp. 334-335.

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