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METASURFACES ENABLED BY APPLICATION-SPECIFIC INTEGRATED CIRCUITS

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The present Doctorate Dissertation was submitted in partial fulfilment of the requirements for the Degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering, and was approved on June 14, 2023 by the members of the Examination Committee.

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Περίληψη

Τα μεταϋλικά είναι συνθετικά ή τεχνητά υλικά, τα οποία παρουσίασαν ιδιότητες που δεν μπορούν να αναπαραχθούν από συμβατικά υλικά. Αυτά τα υλικά αποτελούνται από δομές πολύ μικρότερες από το μήκος κύματος, οι οποίες ονομάζονται μοναδιαίες κυψέλες και διατεταγμένες στο τρισδιάστατο χώρο. Αυτές οι δομές είναι ιδικά σχεδιασμένες ώστε να μπορούν να αλλάζουν τις ηλεκτρομαγνητικές ιδιότητες τους δηλαδή, την ηλεκτρική επιτρεπτότητα και την μαγνητική διαπερατότητα του υλικού. Μια υποκατηγορία αυτόν τον μεταϋλικών είναι οι μεταεπιφάνειες, οι οποίες είναι παροιμία σχεδιασμένες όπως τα μεταϋλικά με μοναδιαίες κυψέλες, αλλά αντίθετος με τα μεταϋλικά οι μοναδιαίες κυξελες είναι περιοδικά διατεταγμένες σε ένα επίπεδο, σε ένα δισδιάστατο πλέγμα. Όπως τα μεταϋλικά, αυτές οι επιφάνειες επιδείξαν ικανότητες που δεν μπορούν να αναπαραχθούν από κανένα φυσικό υλικό. Αυτές οι ικανότητες τους επιτρέπουν να αλληλοεπιδρούν με το ηλεκτρομαγνητικό περιβάλλον τους με τέτοιο τρόπο ώστε να απορροφούν τελείως ένα προσπίπτον κύμα χωρίς ανάκλασης ή ακόμη να ανακλούν τέλεια ένα προσπίπτον κύμα σε μια γωνία που δεν ακολουθεί τον νόμο του Σνελ χωρίς απώλειες.

Αυτές οι δύο ικανότητες, η τελειά απορρόφηση και η τελειά ανάκλαση, μπορούν να θεωρηθούν ως βασικές ικανότητες των μοναδιαίων κυψελών για τον έλεγχο του πλάτους και της φάσης του ανακλώμενους κύματος. Με αυτό τον ελέγχω, οι μεταεπιφάνειες έχουν χρησιμοποιηθεί για τη δημιουργία πολλαπλών περιπλοκών μετώπων κυμάτων. Αυτά τα μέτωπα έχουν δημιουργηθεί με στατικό και δυναμικό τρόπο. Η δυναμική υλοποίηση τους έχει επιτευχθεί με την ενσωμάτωση ενεργών, μεταβλητών στοιχείων όπως διόδων, σε κάθε μοναδιαία κυψέλη. Όλες οι μοναδιαίες κυψέλες μπορούν να μεταβληθούν ταυτόχρονα, με τη πόλωση τους από μια κεντρική τάση. Επίσης, κάθε κυψέλη μπορεί να πολωθεί μονή της από μια κεντρική μονάδα ελέγχου και να κατορθώσει να μεταβάλει τη φάση ή και το πλάτος σε κάθε κυψέλη ξεχωριστά. Με αυτό το μεμονωμένο έλεγχο έχουν υλοποιείθει πολυλειτουργικες και επαναπρογραμματιζόμενες μεταεπιφάνειες.

Η υλοποιήσεις αυτόν τον επαναπρογραμματιζόμενων μεταεπιφάνειων με κεντρικές

μονάδες ελέγχου είναι δύσκολη καθώς κάθε κυψέλη πρέπει να είναι ηλεκτρικά ενωμένη με την κεντρική μονάδα ελέγχου. Το κόστος, η κατανάλωση ενέργειας, η επεκτασιμότητα και η αξιοπιστία αυτόν τον επαναπρογραμματιζόμενων μεταεπιφάνειων χρήζει βελτίωσης. Στην παρούσα διατριβή αυτό επιτυγχάνετε με την ενσωμάτωση κάθε κυψελης με ιδικά σχεδιασμένα ολοκληρωμένα κυκλωμάτα. Πέραν τούτων, αυτά τα ολοκληρωμένα κυκλώματα παρέχουν επιπλέων λειτουργίες και ευκολία στη σχεδίαση της μεταεπιφάνεια. Τα ολοκληρωμένα κύκλωματα φορτώνουν κάθε κυψέλη μονάδας με συνθέτες εμπέδησεις ώστε να μεταβάλει τόσο το πλάτος όσο και τη φάση του ανακλώμενου κύματος. Με προσεκτικό σχεδιασμό των ολοκληρωμένο κύκλωματων ραδιοσυχνοτήτων και της ηλεκτρομαγνητική μεταεπιφάνεια, η πρώτη οικογένειας ολοκληρωμένων κυκλωμάτων για προγραμματιζόμενες μεταεπιφάνειες παράχθηκε καθώς και η πρώτη πολυλειτουργική και αναδιαμορφώσιμη μεταεπιφάνεια εξοπλισμένη με αυτά τα ολοκληρωμένα κυκλώματα.

Η μεταεπιφάνεια που είναι εξοπλισμένη με αυτά τα ολοκληρωμένα κυκλώματα επέδειξε τον έλεγχο του μεγέθους και της φάσης των συντελεστών ανάκλασης για ευρείες γωνίες πρόσπτωσης τόσο για εγκάρσιες ηλεκτρικές όσο και για εγκάρσιες μαγνητικές πολώσεις. Το ανακλώμενο κύμα μπορεί να μηδενιστεί και οι δύο πολώσεις μπορούν να απορροφηθούν ταυτόχρονα και ανεξάρτητα μέχρι και αμβλείες γωνίες πρόσπτωσης τόσο για την εγκάρσια ηλεκτρική πόλωση όσο και για την εγκάρσια μαγνητική πόλωση. Ο έλεγχος μεγέθους και φάσης αξιοποιείται για να επιδειχθεί προγραμματιζόμενος χειρισμός ηλεκτρομαγνητικού μετώπου κύματος. Η μεταεπιφάνεια απόδειξε πειραματικά ότι μπορεί να παράγει αυθαίρετου σχήματος και πόλωσης μετώπα κύματος. Η αρχιτεκτονική που παρουσιάστηκε και το πρωτότυπο (η μεταεπιφάνεια), βρίσκουν άμεση εφαρμογή σε μείωσης διατομής ραντάρ, έξυπνα προγραμματιζόμενα ασύρματα περιβάλλοντα εσωτερικού και εξωτερικού χώρου, ακόμη μπορεί να τοποθετηθεί σε υφιστάμενους και μελλοντικούς σταθμούς βάσης τηλεπικοινωνιακών συστημάτων.

Abstract

Metamaterials are composite materials which demonstrate properties that can't be reproduced by materials found in nature. These materials consist of sub-wavelength structures, unit cells, which are engineered to alter their electromagnetic medium properties. A subclass of metamaterials, metasurface, are arranged in a two-dimensional lattice. Similar to metamaterials, these surfaces demonstrate abilities that can't be found in any nature material. Their abilities enable them to interact with their electromagnetic environment so as to perfectly absorb or perfectly reflect an incident wave at an angle which doesn't follow Snell's law.

These two metasurface abilities, can be considered as amplitude and phase control abilities by their sub-wavelength structures. These two abilities were exploited to generate complex wave-fronts. Wave-fronts were generated in a static manner first and later in a tunable and dynamic manner. Tunability can be achieved by embedding tunable lumped elements within each unit cell. All the tunable lumped elements can be biased simultaneously. By connecting each tunable lumped element to a central biasing unit like a field-programmable-gate array board individual, or local, control of amplitude and phase can be implemented in a programmable scheme. This implements a multifunctional and reconfigurable programmable metasurface.

These implementations find a bottle-neck, which is inherited by their discrete lumped-element implementation. Cost, power consumption, scalability and reliability need to be addressed while incorporating additional functionality and performance in the metasurface design. This thesis addresses these limitations by incorporating application specific integrated circuits (ASICs), within each unit cell. The integrated circuit loads each unit cell, so as to control both amplitude and phase. Careful co-design of radio-frequency integrated circuits and electromagnetic metasurfaces, have led to the manufacturing of the first family of ASICs for programmable metasurfaces, along with the first multifunctional and reconfigurable

ASIC-equipped metasurface.

The produced metasurface demonstrates control over the reflected magnitude and phase for a wide range of incident angles for both transverse electric and transverse magnetic polarizations. The reflected wave can be set to zero, and both polarizations can be perfectly absorbed simultaneously and independently up to oblique angles of incidence for both transverse electric polarization, and for traverse magnetic polarization. Magnitude and phase control is exploited to demonstrate programmable electromagnetic wavefront manipulation for producing arbitrary shape and polarization wave-fronts. The presented design finds direct application in reduce radar cross-section application, smart indoor/outdoor programmable wireless environments, it can be retrofitted in current and future telecommunication systems.

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To my wife and parents.

Στη σύζυγο και στους γονείς μου.

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2. **K. M. Kossifos**, J. Georgiou, and M. A. Antoniades, "ASIC Enabled Programmable Metasurfaces-Part 1: Design and Characterization," IEEE Trans. Antennas Propag..

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AR axial ratio 206

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BGA ball grid array 144

BRCS bistatic radar cross section 197

CMOS complementary metal-oxide semiconductor 70

COTS commercially-available off-the-shelf 6

CP circular polarization 2

CPW coplanar waveguide 30

CPWG coplanar waveguide with ground 28

CTM capacitor-top-metal 22

DAC digital-to-analog converter 4

DC direct current 6

DFT discrete Fourier transform 188

DUT device under test 28

List of Symbols

Chapter 1

Introduction

Metamaterials (MTMs) are materials that are engineered to exhibit properties that are not found in nature. In 1968, it was theoretically shown that materials with negative refractive index can be achieved by obtaining negative electric permittivity (ε) and magnetic permeability (μ) [1]. The electric field vector, magnetic field vector and wave vector of a propagating wave in negative-refractive-index media will form a left-handed triplet, contrary to positive-refractive-index media where they form a right-handed triplet. Veselago therefore named negative-refractive-index and positive-refractive-index media left-handed and right-handed media, respectively. This ability was experimentally demonstrated at the beginning of the century, in 2001, by employing an array of periodic, electrically small unit cells consisting of copper strips and split ring resonators [2].

By engineering the refractive index of a material, the refracted angle of a travelling wave exiting or entering a material can be directed at an angle which was impossible with conventional materials. An extension of this property was shown in [3] where a gradient of refractive indexes was engineered around a cylindrical object to redirect a wave around the object. By redirecting the wave around an object, the object will neither reflect, absorb nor cast a shadow, in simple terms the object will not interact with the wave, and thus it is effectively cloaked. With MTMs, researchers were able to construct lenses which had the ability to resolve objects beyond the diffraction limit [4]. These lenses, appropriately termed "Veselago-Pedry superlenses" are designed with strict criteria, where the relative electric permittivity and magnetic permeability of the lens medium is equal to -1. Such a lens can find many practical applications in biomedical imaging, lithography and sensing.

Periodically loaded transmission lines with lumped inductors and capacitors have also demonstrated the ability to engineer the refractive index in two-dimensional transmission lines [5] and even one-dimensional transmission lines [6]. Periodically loaded transmission line MTMs take advantage of the engineered refractive index without compromising their size, making them more suitable for radio frequency (RF) and microwave (MW) applications. These periodically loaded transmission lines were adopted in many microwave and antenna designs [7–9], and improved their performance and form factor.

Metasurfaces (MSFs) are the two-dimensional counterparts of MTMs. MSFs consist of by a two-dimensional array of unit cells which are electrically small along their period, but also electrically thin. MSFs are able to alter their electromagnetic properties to perfectly absorb an incident wave [10, 11]. This is implemented by engineering the surface impedance of the MSF to match the impedance of the incident wave. In this scenario, where the surface impedance is matched to the incident wave impedance, all the MSF's unit cells are identical. MSFs have also demonstrated anomalous reflection where the unit cells are arranged in such a way that each unit cell has a progressively different reflection phase than its neighbouring unit cells [12, 13].

Perfect absorption and anomalous reflection are the basis of magnitude and/or phase control for MSF unit cells. By setting either the reflection coefficient amplitude or phase response of each individual unit cell, researches have demonstrated multiple simultaneous functions [14]. This amplitude or phase response manipulation is implemented by altering the geometric parameters of each of the MSF's unit cells. An example can be seen in Fig. 1.1 where the MSF consists of periodically arranged unit cells of size D. The unit cell geometry can be seen in the top left corner of the figure, and this particular geometry is commonly referred to as a Jerusalem cross. Each width (W_x, W_y), length (L_x, L_y) and gap (G_x, G_y) is modified to match a set reflection coefficient for each of its orthogonal x and y component. Doing so, this particular example can collimate or focus a beam and simultaneously convert a linear polarization (LP) to a circular polarization (CP) wavefront. By being able to set both the reflection coefficient magnitude and phase response of each unit cell individually, MSFs have demonstrated even more complex wavefront manipulation capabilities. Complex wavefronts have been demonstrated such as, multiple pencil beams [15, 16], multiple pencil beams with power control of each beam indepen-

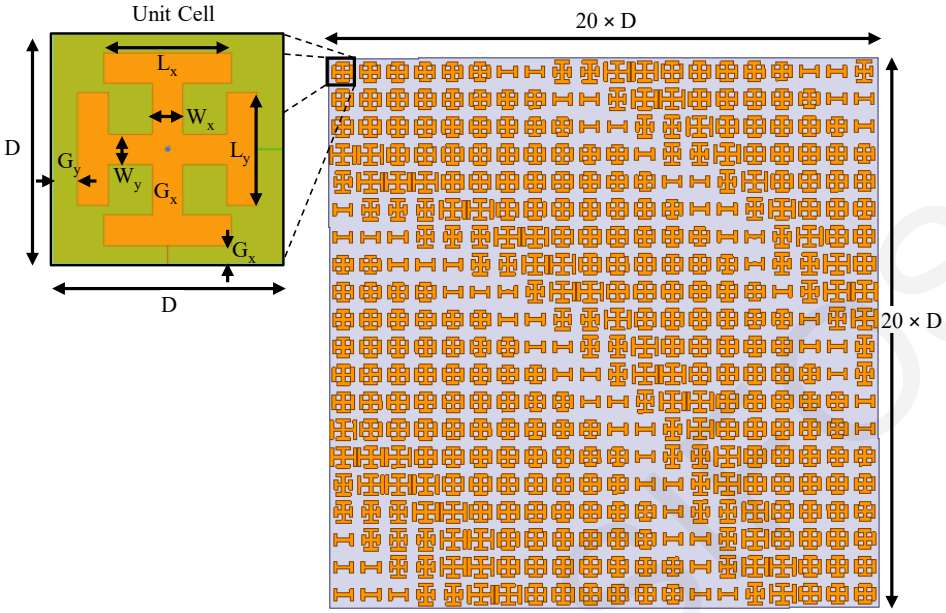


Figure 1.1: Example of a coding MSF. Each unit cell's geometric parameters are set individually through a code before manufacturing.

dently [17], orbital angular momentum (OAM) beams [18] and holographic beams [19]. These types of MSFs are found in the literature as coding MSFs, since they require some sort of coding to calculate each unit cell's response.

Although these MSF capabilities are promising, they are static, meaning that they produce an MSF response that can't be altered after its fabrication. In order to introduce a post fabrication alteration or a tunable response, MSF designs have incorporated tunable elements in their unit cells. By applying a voltage on such tunable elements, the electrical properties of that element could be tuned to alter the resonant behaviour of the unit cell. Numerous electrically-tunable MSFs have been shown, including the use of varactors [20,21], integrated loading elements [22], liquid crystals [23], and more recently utilizing graphene [24–26]. The biasing of the lumped elements within each unit cell is done by grouping rows or columns and connecting them to a biasing voltage. An example of a distribution of one biasing voltage can be seen in Fig. 1.2. This distribution groups all the tunable elements in one biasing voltage. Other devices with more biasing voltages can be found in the literature [27]. Due to this biasing voltage distribution, the abilities of such devices remain limited to this global operation.

Besides electrical tunability, numerous other means of obtaining a tunable MSF behaviour have been shown in [27], magnetic tunability has been shown in [28], and optically tunable behaviour has been shown in [29]. Other chemical materials like

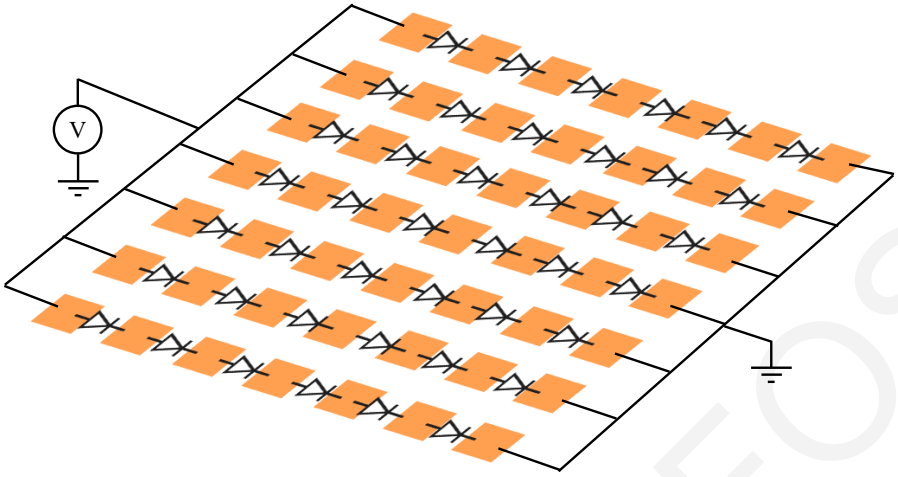


Figure 1.2: Illustration of a tunable MSF. Each unit cell is loaded with a diode.

poly dispersed red 1 acrylate (PDR1A) with optically tunable response have been explored [30]. This particular material has been shown to possess a memory effect [31].

When an MSF is applied in a practical application, it is desirable to avoid human intervention when changing the MSF state via tuning. Such tunability, which typically requires a bias voltage to be changed on the tunable elements without a human to change the dial on a power supply, would require some programmability. A central processing unit or microcontroller or even a field programmable gate array (FPGA) can be used to provide the digital input to digital-to-analog converters (DACs), which will bias the tunable elements embedded within the unit cell. The central processing unit can be connected to a computer which controls the MSF trough software. This software control gives rise to the possibility of programmatically controlling each unit cell independently, which is a tedious process to be implemented manually. These logical steps gave rise to a new type of MSFs. In the literature these types of MSFs can be found as programmable metasurfaces (PMSFs) or even intelligent reflective surfaces (IRSs).

Programmable MSFs with their individual unit cell control have demonstrated multiple reconfigurable functions, such as polarization, scattering and focusing control [32], holography [33, 34], non-linear harmonics control [35], machine learning imaging [36], and frequency recognition for self-adaptivity [37]. Programmable MSFs, and their aforementioned advanced electromagnetic manipulation capabilities, have provided the potential to greatly improve wireless telecommunications through the smart radio environment reconfiguration paradigms [38–42], and have

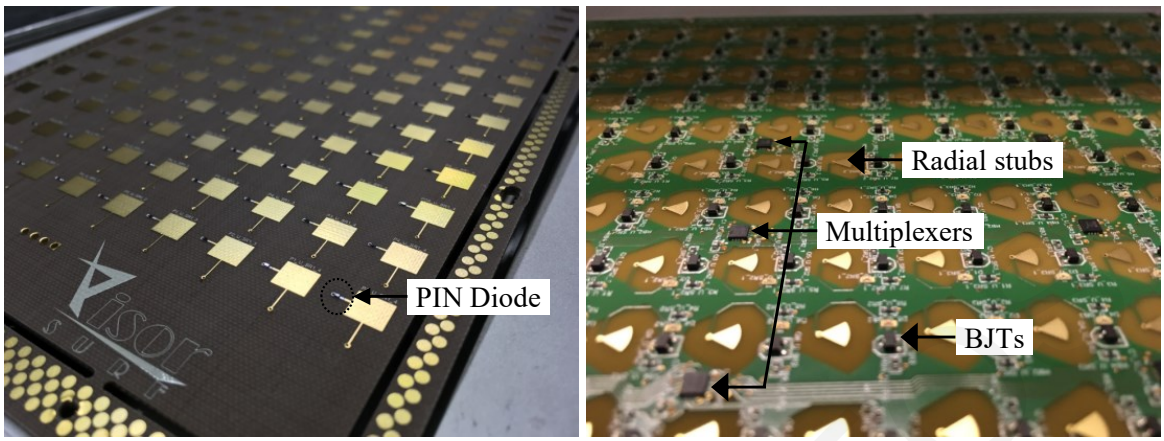
increased the capabilities and agility of antenna applications [43–47].

The use of programmable MSFs in radio environments is in contrast to traditional wireless telecommunications systems, where the effect of the terrain or structural environment is simply accounted for by the transmitter and receiver. By operating a programmable MSF in a radio environment, the parameters of the channel can also be partially controlled. PMSFs operated in this manner have shown promise in improving multiple aspects of wireless telecommunications, such as increased reliability, energy efficiency and security [38–42, 48–50].

A PMSF can be illuminated within the Fraunhofer region by a passive directive antenna such as a rectangular horn antenna, and can programmatically alter the overall radiating pattern [50, 51]. This concept is not new and has been implemented using traditional transmit- and reflect-arrays [52,53]. PMSFs in this scenario, provide greater control over the reflected or transmitted wavefront due to their subwavelength unit cell size.

1.1 Motivation

The goal of this thesis, even though it pre-dates most of the work on programmable MSFs, was to address the limitations and constrictions found in many current programmable MSFs. Currently, PMSFs rely on external, costly and power hungry FPGAs to bias with discrete states each unit cell [32–37]. Within these PMSFs, each unit cell is equipped with a lumped diode, which enables their tunability. An example implementation can be seen in Fig. 1.3, the tunable lumped element in this case a P-intrinsic-N (PIN) diode can be seen in Fig. 1.3(a). In addition, the power to bias all the diodes due to the large number of unit cells is significant. This is not apparent at first; for the example design in Fig. 1.3 which needs 10 mA to forward bias each PIN diode, this will translate into a total of 16 A for a PMSF consisting of 40×40 unit cells. So in retrospect, a different type of diode would have been more appropriate for PMSF applications. Digital-to-analog converters (DACs) are used to provide multiple discrete states to each unit cell, with the compromise of further increased power consumption. The implementation of the feeding networks to each unit cell is a challenging process, which requires additional digital circuits. Since each subwavelength unit cell needs to be addressed, a digital line will need to connect to it. Within this unit cell area, other RF/MW space-consuming components might be



(a) (b)

Figure 1.3: Example implementation of PMSF design. This prototype is based on [32]. (a) The top textured side of the PMSF is shown, where the PIN diodes are populated. On the bottom (b), bipolar junction transistors, multiplexer and radial stubs are used to forward bias each PIN diode.

needed for biasing purposes, to isolate the direct current (DC) from the RF/MW signal. In the example in Fig. 1.3(b) a radial stub is used as part of the biasing network, which occupies a large proportion of the unit cell area. Digital multiplexers and shift registers can be used to reduce the number of DC lines in order to implement a PMSF with a finite area. Eventually, this approach will require additional FPGAs to scale up, and as the operating frequency of the PMSF increases this approach will not be viable even for most applications where the PMSF is required to occupy an area of 5×5 λ^2. Furthermore, the programmable approaches outlined in [32–37] only control the phase response of the unit cell and are for a single polarization. Real life application and adaptation will require far greater control. Controlling the phase and magnitude of each unit cell for both polarizations with commercially-available off-the-shelf (COTS) components like FPGAs, diodes and DACs will only increase further the complexity of the feeding networks, the power consumption and the cost of the MSF [54].

PMSFs, and their aforementioned architecture in their current state, have found a bottleneck that can only be addressed with a new architecture. Furthermore, since MSFs are still relatively new, they do not offer a well-defined way to be used in real-life applications. This makes them unappealing to engineers that work in other professions, for example to engineers working in wireless network deployment or even for engineers working in imaging applications. In order to tackle this bottleneck and make PMSFs easily realised, scalable, low-cost and low power, new hardware

and software components need to be developed. These components need to be available to the public with plug-and-play operation [55].

This new MSF architecture proposed in this work, embeds application-specific integrated circuits (ASICs) within the PMSF's unit cells. The ASICs are controlled through software, which is build on an application programming interface (API). With this software the PMSF is controlled and by extension its electromagnetic environment can also be controlled.

The proposed ASIC-enabled PMSFs architecture, besides being low-cost and low-power, also introduces increased functionalities. The architecture aims to be able to control both the transverse electric (TE) and transverse magnetic (TM) polarization's reflection amplitude and phase for each unit cell. With this ability, the reflection coefficient of each unit cell can be analytically calculated and consequently be easily coded in software as a predefined function. Arbitrary near field and far field wavefronts can be analytically derived and generated, with the press of a button. Analytically generating a wavefront is less time consuming compared to an iterative method approach, thus making the ability to analytically generate a wavefront particularly useful, since there are also time constraints in many applications. All these combined attributes can greatly improve multiple areas of science and applications. Applications like reduced radar cross section (RCS), stealth, imaging, holography, and current and future telecommunication systems.

The developed architecture aims for a plug-and-play incorporation and has a large impact by addressing cost, energy and expandability constrains. Such an architecture will drive the development of many future ASIC and MSF designs that will find even more applications and help humanity in multiple sectors.

1.2 Thesis Overview

In this thesis, two PMSF prototypes were developed. The top-level architecture of the two PMSFs can be seen in Fig. 1.4. The top-level architecture for both designs involve a MSF which is equipped with an ASIC in every unit cell. A graphical user interface (GUI) is used in both designs to choose the desired PMSF functionality. The GUI can be operated on a desk-/lap-top or personal computer. This desired functionality is strongly dependent on the PMSF, therefore the GUI translates the desired functionality into physical input signals to the ASIC. These signals are transmitted

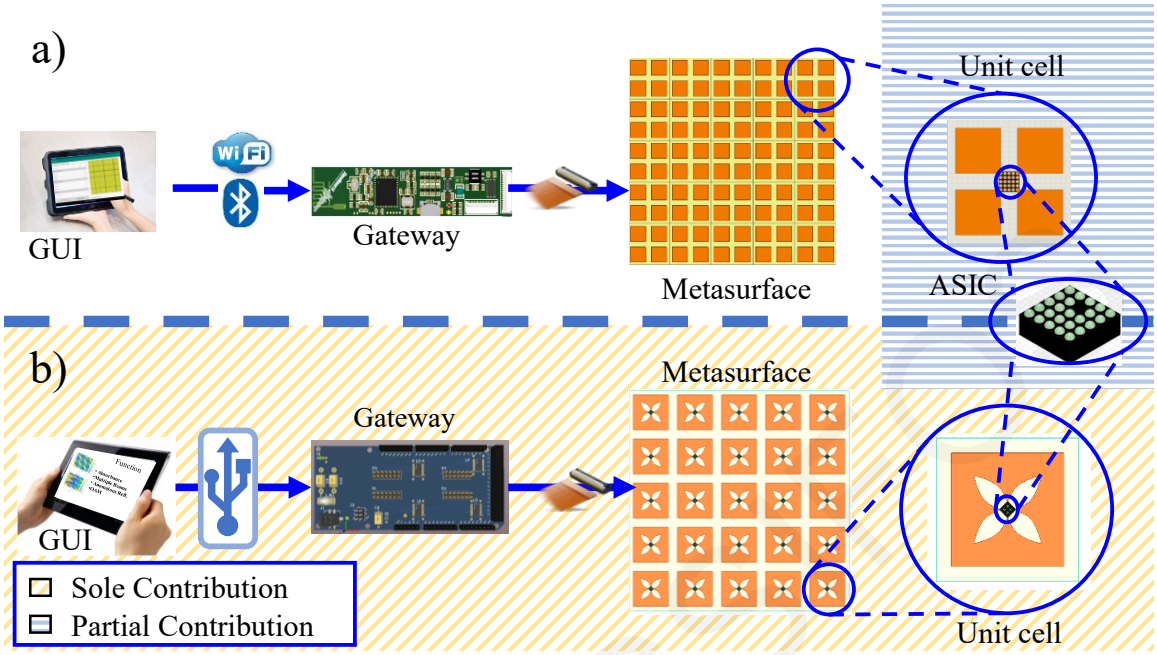


Figure 1.4: Top-level architecture for two electronically PMSF. In (a) the author partially contributed to the development of the unit cell and the RF part of the ASIC. In (b) the author used the ASICs and build the complete system.

to a gateway which is electrically connected to the PMSF and from there propagated within the PMSF.

In the Fig. 1.4(a) the gateway was custom-built which could communicate to the GUI with either a bluetooth or WiFi connection and a wired connection. The unit-cell's design comprised of rectangular patches connected to an ASIC in the middle. The ASIC loads the unit cell with four complex impedance loading elements (LEs). Within the ASIC, an asynchronous control circuits is integrated along with DACs and LEs. For this project, the author contributed with the complete development of the RF part of the ASIC, (the LEs), and partial development of the unit cell design.

In the Fig. 1.4(b) the author utilized the ASIC design he already contributed to, to implement a PMSF with extended capabilities compared to the one in Fig. 1.4(a). Furthermore, the author designed the gateway and GUI. The gateway is a simple microcontroller with a voltage level shifter to ensure the correct compatibility with the integrated circuit (IC) voltage range. The gateway communicates to the GUI with a universal serial bus (USB) wired connection, since during the MSF electromagnetic testing there shouldn't be any electromagnetic radiation interfering with the measurements.

During the development of this PMSF architecture, the author performed RF/MW measurements to verify the operation of the ASIC on-wafer using ground signal

ground (GSG) probes. Once the ASIC was packaged, connectorized measurements were performed on populated printed circuit boards (PCBs). Measurement techniques were developed to accurately de-embed the packaged ASIC. Finally, in order to measure the whole PMSF the author developed his own near field (NF) system to obtain the scattered far field (FF) of the PMSF.

1.3 Thesis Outline

This thesis is divided into six main chapters, excluding the introduction and conclusion. In Chapter 2, background information on the research can be found. Background information for MSF modelling, RF/MW IC components and measurement techniques for all the stages of the design. That is, on-wafer, connectorized or packaged measurement techniques and near field measurement techniques.

The first developed MSF design is presented in Chapter 3, in this chapter the MSF architecture is presented along with an example unit cell design. In this chapter the theoretical LE design analysis is presented along with the top level architecture of the ASIC. The theoretical analysis is validated through simulations and from on-wafer measurements.

A second MSF design is presented in Chapter 4. This MSF design overcomes limitations found with the previous design as it has increased tunability, wider angle range and operates simultaneously for both TE and TM polarizations. Using these functionalities, the design demonstrates not only perfect absorption at a wide angle range but also the generation of arbitrary shaped and polarized wavefronts. Using this MSF design in Section 4.4, the effects of mismatch are studied, and simulated results are presented.

In order to realise the MSF designs presented in Chapter 3 and Chapter 4 the first family of ASICs was realised; and is presented in Chapter 5. A prototype PMSF equipped with an ASIC is presented in Chapter 6, which evolved from the design in Chapter 4. The design's reflection coefficients are measured using a custom measurement set-up in this chapter. This PMSF design's characterization was not a trivial task. PMSF are electrically large, and multiple wavelengths in size. Electrically large antennas are usually measured in near field systems. PMSF unlike electrically large antennas, are not radiating structures but are electromagnetic interacting surfaces. Therefore, adaptation to already existing measurement methods was needed. The

current state of the research concludes with Chapter 7. In this chapter, a synthesis performance of the MSF is evaluated. Finally, this thesis is concluded with Chapter 8, where the conclusion, contributions and possible directions for future work can be found.

Chapter 2

Background Information

Background information required for better comprehension of the work is presented in this chapter. Contributions were made to all the levels of the programmable MSF's design, and therefore this chapter contains background information for all the levels. Information can be found for MSF, RF/MW IC design and measurements. In Section 2.1 the basic modelling of MSFs is presented. The analysis starts with simple periodic structures, and finishes with the analysis of an artificial impedance surface loaded with lumped loads. The artificial impedance surface loaded with lumped loads, strongly resembles the MSF in Chapter 3. It's modelling is presented in order to introduce the basic mechanism and operation of the manufactured MSFs.

The presented MSF uses ICs to programmatically tune the electromagnetic characteristics of each unit cell. This approach is drastically different compared to other programmable MSFs but it is essential to gain more functionality out of the MSF without compromising cost, energy efficiency and expandability. This approach entails that the IC is co-designed with the MSF and therefore the background information in this chapter contains essential information for RF/MW IC components, found in Section 2.2.

The measurement performed in the scope of this work required specialized techniques in all the development stages of the manufactured prototypes. Background information regarding this technique and methods can be found in Section 2.3. Even though this information is not exhaustive, it presents the required information to effectively communicate the techniques used to perform the necessary measurements later on in the next chapters. Information can be found for on-wafer, connectorized (Section 2.3.1) and antenna (Section 2.3.2) measurements techniques.

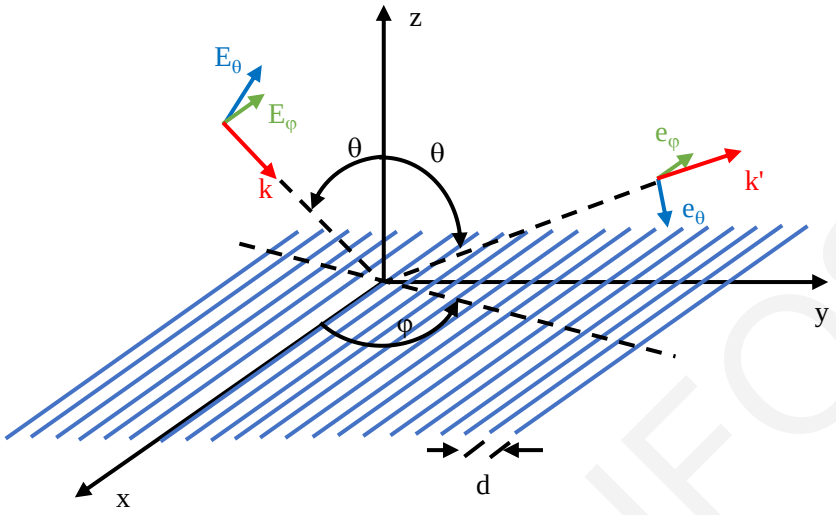


Figure 2.1: The geometry of the planar regular array of wires.

2.1 Metasurfaces

Periodic structures have found application in filters, antennas and more recently in the design of MTMs, and in extension MSFs. Analytical modelling of such structures is important to understand the operating mechanism of such structures. The section provides a brief introduction on the modelling of MSFs by following and summarizing the work of [56], and supplements additional information from other more recent sources.

2.1.1 The Simple, Wire Grid

A periodic array of thin wires can be considered the simplest form of periodic structures. Consider that this array is only periodic only along one axis, the y-axis (see Fig. 2.1).

The analytical formulation of the reflected and transmitted electric field ($\boldsymbol{E}$) and magnetic field ($\boldsymbol{H}$) is a cumbersome procedure and falls outside the scope of this thesis. This analysis is avoided here but without compromising the purpose of this section. Instead, one can introduce a lumped impedance which produces the same response as the wire grid. This lumped impedance is referred to as the surface impedance of the grid (Z_g). This surface impedance is the equivalent impedance in the equivalent transmission line model seen in Fig. 2.2. In [56] the surface impedance

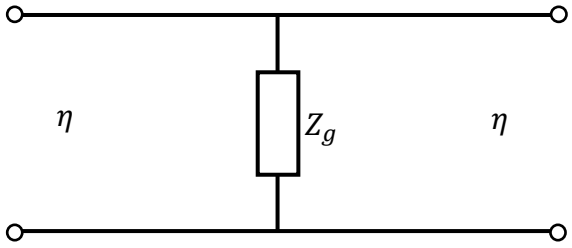


Figure 2.2: Equivalent transition line model for planar array of wires in isotropic space with a wave impedance η (normal incidence).

of a periodic array of parallel wires as shown in Fig. 2.1 is ([56], eq. 4.38):

$$Z_g = Zd + j\frac{\eta}{2}\alpha\left(1 - \sin^2\theta\ \cos^2\varphi\right), \tag{2.1}$$

where Z is the impedance per length, d is the separation between the wires, η is the free space impedance and α is the grid parameter ([56], eq. 4.31):

$$\alpha = \frac{kd}{\pi}\left[\log\left[\frac{d}{2\pi r_0}\right] + \frac{1}{2}\sum_{m=-\infty}^{\infty}\frac{2\pi}{\sqrt{\left(2\pi\eta + k_y d\right)^2 - \left(k^2 - k_x^2\right)d^2}} - \frac{1}{|\eta|}\right] \tag{2.2}$$

For a dense grid where the following conditions are satisfied:

$$k_y d \ll 2\pi,\ \left(k^2 - k_x^2\right)d^2 \ll 2\pi, \tag{2.3}$$

the grid parameter can be simplified to:

$$\alpha = \frac{kd}{\pi}\left[\log\left[\frac{d}{2\pi r_0}\right]\right] \tag{2.4}$$

The reflection (R) and transmission (T) coefficients for normal incidence are:

$$R = -\frac{\frac{\eta}{2}}{\frac{\eta}{2} + Z_g},\ \ T = 1 + R = \frac{Z_g}{\frac{\eta}{2} + Z_g}, \tag{2.5}$$

whereas for oblique angles the reflection coefficients for TM-polarized incident waves are:

$$R_{TM} = \frac{e_\theta}{E_\theta} = \frac{\cos^2\theta\ \cos^2\phi}{AE}, \tag{2.6}$$

$$R_{EM} = \frac{e_\phi}{E_\theta} = \frac{\cos\theta\ \sin\phi\ \cos\phi}{AE}, \tag{2.7}$$

and for TE-polarized incident waves:

$$R_{TE} = \frac{e_\phi}{E_\phi} = \frac{\sin^2\phi}{AE}, \tag{2.8}$$

$$R_{ME} = \frac{e_\theta}{E_\phi} = \frac{\cos\theta \ \sin\phi \ \cos\phi}{AE}, \tag{2.9}$$

where AE is equal to:

$$AE = \left(1 - \sin^2\theta \ \cos^2\phi\right)(1 + j\alpha\cos\theta) + \left(\frac{\eta}{2} Z\, d\cos\theta\right). \tag{2.10}$$

The TE to TM and TM to TE cross-polarization conversion terms are referred to as R_{EM} and R_{ME} in (2.7) and (2.9), respectively. The transmission for oblique incident angles follows the general rule of $T = 1 + R$. From this analysis it is important to understand the dependence of the reflection and transmission coefficients, and in extension the surface impedance, on the angles $\theta\,\varphi$ at which the wave is incident on the surface, the frequency and the geometrical parameters of the grid.

2.1.2 Grid of Metal Strips

The average boundary conditions of a dense wire grid are described by the single scalar parameter α, the grid parameter. This grid parameter is strongly dependent on all the geometric properties of the wire grid (periodicity, radius). The analytical form for the reflection and transmission coefficients found in (2.5)-(2.9) are dependent on the angle of incidence and are universal for dense arrays. In [56], it was shown that it is enough to measure the reflection and transmission coefficients at a single angle to determine the grid parameter of another unit cell geometry. In this case, planar conducting strips of width w and periodicity d were found to have a grid parameter similar to the wire grid. The grid parameter found was:

$$\alpha = \frac{kd}{\pi}\left[\log\left[\frac{d}{\sin\frac{\pi w}{2d}}\right]\right]. \tag{2.11}$$

For an array of thin strips, the argument of the sine is small and expanding it into a Taylor series approximates to:

$$\alpha = \frac{kd}{\pi}\left[\log\left[\frac{2d}{\pi w}\right]\right]. \tag{2.12}$$

Comparing this to the grid parameter of the wire array in (2.4) and ((2.12), one can see that the two grids have the same response if $w = 4r_0$. Therefore, the grid impedance of a conducting strip array is:

$$Z_g = j\frac{\eta}{2}\alpha = j\omega\mu_0\frac{d}{2\pi}\left[\log\left[\frac{d}{\sin\frac{\pi w}{2d}}\right]\right]. \tag{2.13}$$

For an excitation wave with polarization orthogonal to the strip, the grid impedance can be found by applying the Babinet principle to the strip and substituting the width w with the gap *(d-w)*.

$$Z_g \perp = \frac{\eta}{4Z_g} = \pi \left[j\omega\varepsilon_0 2d \log\left[\left[\sin\left(\frac{\pi\,(d-w)}{2d}\right)\right]^{-1}\right]\right]^{-1}. \tag{2.14}$$

It can be seen that the grid impedance is inductive for an excitation plane wave with polarization parallel to the strips (2.13) and capacitive for the orthogonal polarization (see (2.14)). From this, one can imply that for a polarization with both x and y components the sheet will be at resonance and therefore transparent.

2.1.3 Grid of Rectangular Arrays

Until this point only periodic structures in one dimension were presented, like in Fig. 2.1 the y axis. In this section structures which are periodic in both x and y axis, are summarized, thus expanding on the previous subsection. A periodic structure made of patch arrays and a mesh made of rectangular wires, as can be seen in Fig. 2.3, will be presented. According to [56] the grid impedance of a patch array or rectangular wire grid is mainly capacitive or inductive, respectively. For a patch array (Fig. 2.3(a)) the grid impedance is:

$$Z_{patch}^{TE\|TM} = \frac{1}{j\omega\, C_{patch}}, \tag{2.15}$$

where for TE polarization C_{patch} is equal to [57]:

$$C_{patch}^{TE} = D\varepsilon_0 \frac{(\varepsilon_{r1}+\varepsilon_{r2})}{\pi} \ln\left[\frac{1}{\sin\dfrac{\pi w}{2D}}\right]\left[1-\frac{k_0^2}{k_{eff}^2}\frac{\sin^2\theta}{2}\right], \tag{2.16}$$

and for TM polarization:

$$C_{patch}^{TM} = D\varepsilon_0 \frac{(\varepsilon_{r1}+\varepsilon_{r2})}{\pi} \ln\left[\frac{1}{\sin\dfrac{\pi w}{2D}}\right]. \tag{2.17}$$

For the mesh (Fig. 2.3(b)) the impedance is inductive:

$$Z_{grid}^{TE\|TM} = j\omega\, L_{grid}, \tag{2.18}$$

and for TE polarization L_{grid} is equal to:

$$L_{grid}^{TE} = \frac{D\mu_0}{2\pi} \ln\left[\frac{1}{\sin\dfrac{\pi w}{2D}}\right], \tag{2.19}$$

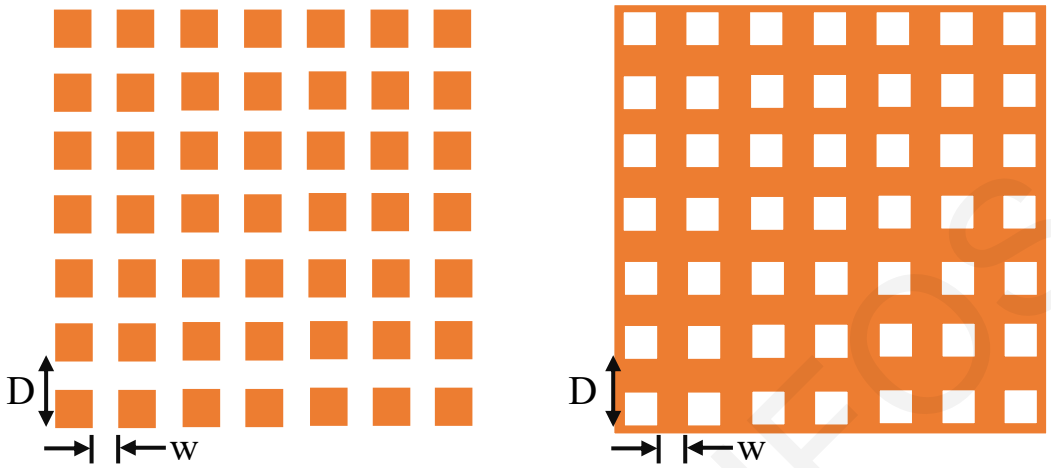


Figure 2.3: Rectangular arrays, (a) capacitive patch array and (b), inductive wire grid.

and for TM polarization:

$$L_{grid}^{TM} = \frac{D\mu_0}{2\pi} \ln\left[\frac{1}{\sin\frac{\pi w}{2D}}\right]\left[1 - \frac{k_0^2}{k_{eff}^2}\frac{\sin^2\theta}{2}\right]. \tag{2.20}$$

The geometric parameters w and D can be seen in Fig. 2.3 k_0 is the free space wave number and k_{eff} is the wave number of the incident wave vector in the effective host medium.

$$k_{eff} = k_0\sqrt{\frac{\varepsilon_{r1} + \varepsilon_{r2}}{2}}. \tag{2.21}$$

The dielectric substrates surrounding the periodic surface on both sides have relative dielectric permittivity ε_{r1} and ε_{r2}. Of course, the inductive or capacitive impedances of the grid can be approximated with the above expressions, but in reality, they are not purely reactive. They also possess a loss component. For the patch array the losses can be added to the calculation using:

$$Z_{patch}^{TE\|TM} = R_{patch} + \frac{1}{j\omega C_{patch}}, \tag{2.22}$$

$$R_{patch} = \rho\frac{D - w}{(D - w)\,T}\,. \tag{2.23}$$

As for the losses for the wire grid, these haven't been yet addressed in the literature.

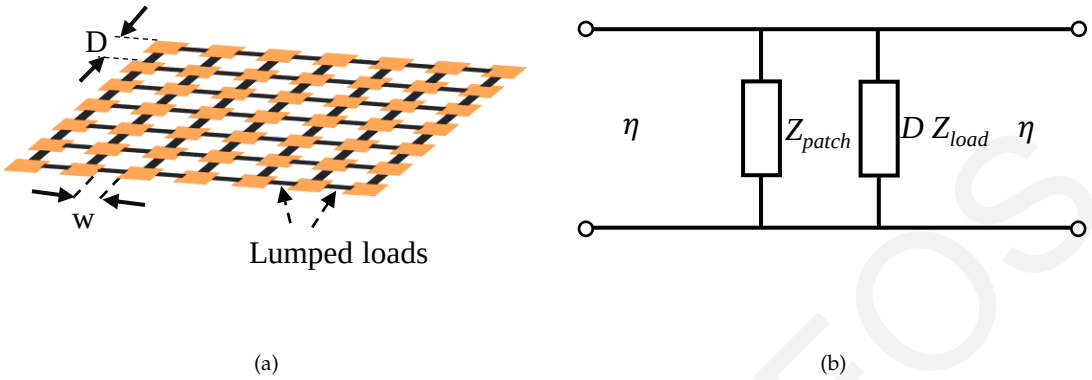


Figure 2.4: (a) Periodic array of patches with lumped loads and (b), equivalent circuit of the loaded patch array.

2.1.4 Grid of Loaded Rectangular Patches

Until this point it was shown that periodic structures possess complex grid impedances. The next logical step would be to try to load this complex impedance with some lumped components to alter this impedance. An example can be seen in Fig. 2.4 where the patch array is loaded with lumped loads. In [56], the author states that the grid impedance of such a periodic array becomes the equivalent circuit of a parallel connection of the grid impedance of the periodic structure, in this case the patch array, and the impedance of the loads (Z_{load}) times the periodicity of the grid (D).

$$Z_g = Z_{patch} \,||\, (D\, Z_{load}) \ . \tag{2.24}$$

2.1.5 Artificial Impedance Surfaces

In many antenna and waveguide applications, it is desirable to have a surface with a specific surface impedance. Imagine an antenna located near a metallic structure, like an antenna on an aircraft. A common dipole in this case will suffer greatly since the reflected power from the metallic surface will cancel out with the radiated power in the FF. Lets look at the reflection coefficient of a normally incident electric field on a surface:

$$R_e = \frac{Z_s - \eta}{Z_s + \eta} \ . \tag{2.25}$$

Here, Z_s is the surface impedance and η is the free space impedance. For a perfect electric conductor, $Z_s = 0$ and $R_e = -1$. For a perfect magnetic wall, $Z_s = \infty$, and the $R_e = 1$. A surface with $R_e = 1$ could solve the problem of the dipole over the metallic structure, since the reflected power will not cancel out in the FF. This was traditionally done with a magnetodielectric layer of thickness d positioned on a metal ground plane, as in Fig. 2.5.

The input impedance seen at the upper surface by normally incident waves is given by [58]:

$$Z_s = Z_0 \frac{Z_m + Z_0 \tanh(\gamma d)}{Z_0 + Z_m \tanh(\gamma d)} \tag{2.26}$$

The load impedance (Z_m) can be calculated using the:

$$Z_m = T\rho, \tag{2.27}$$

where T and ρ are the thickness and the resistivity of the metal used in the ground plane, respectively. The substrate impedance Z_0 can be calculated using:

$$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}. \tag{2.28}$$

Since most cases the electrical properties of the substrate is provided by the manufacturer with two parameters the relative dielectric constant (ε_r) and loss tangent ($\tan\delta$), which can convert to ε using:

$$\varepsilon = \varepsilon' + j\varepsilon'' = \varepsilon_0\varepsilon_r + j\varepsilon_0\varepsilon_r \tan\delta. \tag{2.29}$$

The propagation constant γ can be found using:

$$\gamma = a + j\beta. \tag{2.30}$$

Here, a is the attenuation constant and β is the phase constant:

$$a = \omega \sqrt{\frac{\mu\varepsilon'}{2}\left(\sqrt{1 + \left(\frac{\varepsilon''}{\varepsilon'}\right)^2} - 1\right)} \left(\frac{Np}{m}\right), \tag{2.31}$$

$$\beta = \omega \sqrt{\frac{\mu\varepsilon'}{2}\left(\sqrt{1 + \left(\frac{\varepsilon''}{\varepsilon'}\right)^2} + 1\right)} \left(\frac{rad}{m}\right). \tag{2.32}$$

For a magnetodielectric layer where the attenuation constant (a) is negligible, the surface impedance of the artificial impedance layer can be approximated using:

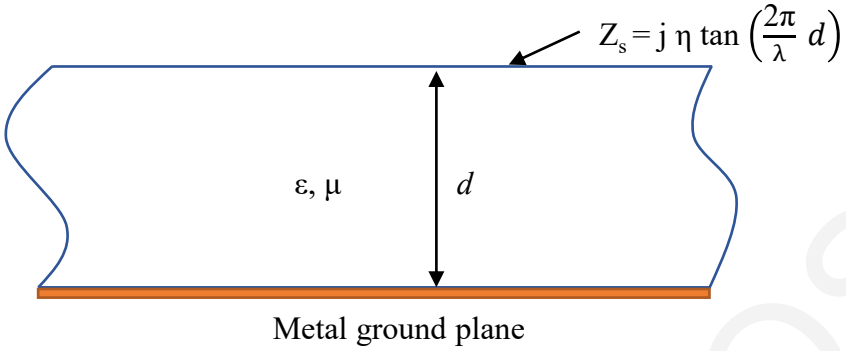


Figure 2.5: Artificial impedance created from with a thick magnetodielectric with parameters ε, μ and d placed over a metal ground plane.

$$Z_s = j\sqrt{\frac{\mu}{\varepsilon}} \tan\left(\omega\sqrt{\mu\varepsilon}d\right) = j\eta \tan\left(\frac{2\pi}{\lambda}d\right). \tag{2.33}$$

At $d = \lambda/4$ the impedance tends to $j\infty$, realizing a magnetic wall. Another way to realize a magnetic wall is shown in [56], where a thin dielectric layer is placed between a capacitive grid and a metal ground plane, as shown in Fig. 2.6(a).

In this case, the dielectric layer is much smaller than the wavelength, and the inductive impedance of the dielectric layer using the ground plane can be approximated with $Z_{ind} = j\omega\mu d$. By this approximation, the inductance of the impedance is equal to:

$$L_{ind} = \mu d. \tag{2.34}$$

This total surface impedance of the artificial impedance structure is then the parallel connection of Z_{ind} and the grid impedance of the top patches (see Fig. 2.6(b)).

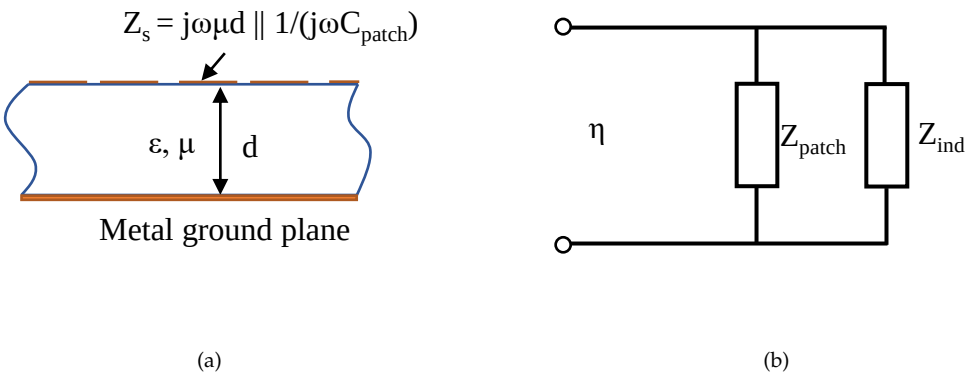


Figure 2.6: Artificial impedance created with a thin dielectric layer (a) structure of metal patches over a dielectric layer with a metal ground plane (b) circuit equivalent.

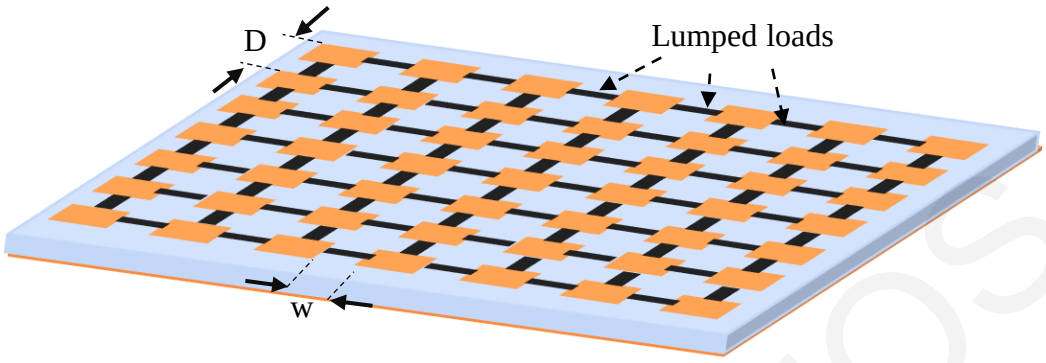


Figure 2.7: Artificial impedance surface loaded with lumped loads.

$$Z_s = \frac{j\omega\mu d}{1 - \omega^2 C_g \mu d}. \tag{2.35}$$

This parallel connection of an inductive impedance with the capacitive impedance of the patches will have a resonant frequency. At the resonant frequency, where $\omega_0 = \sqrt{1/C_g \mu d}$, the imaginary part of the surface impedance tends to infinity. This property is particularly useful, but it is limited to a narrow frequency bandwidth. By loading the artificial impedance surface with lumped loads, as can be seen in Fig. 2.7, one can alter the surface impedance of the surface. The surface impedance in such a loaded artificial impedance surface is approximately calculated by the parallel circuit connection of the grid impedance of the patches (Z_{patch}), the inductive impedance of the substrate (Z_{ind}) and the effect impedance of each load (Z_{load}) times the period of the array (D) :

$$Z_s = Z_{patch} \,||\, Z_{ind} \,||\, (DZ_{load}) \,. \tag{2.36}$$

With this, the derivation of (2.36), the basic understanding of the operation of a loaded unit cell was presented. This principle of operation, is subsequently used to analyze the structures in this work. For a better understanding of the implementation of the load Z_{load} by an integrated circuit, some background information on ICs and their component palette are presented in the next section, Section 2.2.

2.2 Integrated Circuits

The design of integrated RF and MW circuits involves the use of both passive and active components. The operation of such components needs to be understood

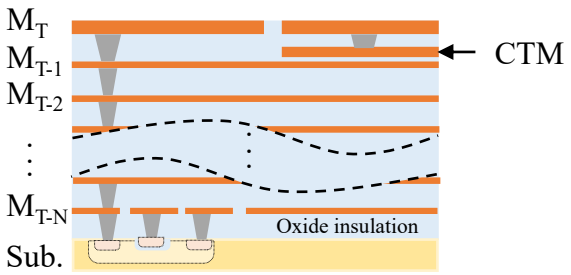


Figure 2.8: Cross-section of a typical integrated circuit technology structure. Multiple metal layers are used (M_T-M_{T-N}) in all integrated circuit semiconductor technologies. Optionally a capacitor-top-metal (CTM) layer is provided.

in detail in order to obtain a functional circuit design. Modelling of such IC components can be found in the literature, and every process design kit (PDK) has adapted these models to accurately describe its own components in a particular foundry's technology. This is because each IC process uses different semiconductors, semiconductor doping, conductor materials etc. This model adaptation, is often done within a specified frequency and voltage range for a small number of component. Their components, which are available to the IC designer, are often referred to as the component palette. Mainstream IC design is implemented on a semiconductor substrate on which the active and some passive components are manufactured. Various semiconductor types are commercially used, but this thesis focuses only on an economically affordable silicon semiconductor process. On this silicon-semiconductor substrate, metal layers are manufactured. Many metal layers are used to accommodate routing of the internal power, digital and RF/MW signals. These metallizations are connected with vertical vias and are separated with isolation layers which are usually implemented with oxides of the semiconductor (for example if the semiconductor is silicon, Si the oxide will be SiO_2). A simplified vertical cross-section of an IC showing the metallization, vias and substrate can be seen in Fig. 2.8. The manufacturing of an IC with such a cross-section involves multiple sequential steps of photolithography and chemical processing.

Historically, the mainstream silicon IC technologies were driven by the digital circuits market and their need for circuit miniaturization and increase in logic complexity. This, left the RF and MW circuit component palette somewhat limited. Small additions have been made recently to this palette by adding specialized RF components in the PDK. Some of these components need additional manufacturing

steps. For example, passive metal insulator metal (MiM) capacitors use a capacitor-top-metal (CTM) layer as their one terminal. This layer is between the top metal layer (M_T) and the metal layer below it (M_{T-1} see Fig. 2.8). This is implemented to provide an even smaller component footprint and increase the capacitor's quality factor. Even so, both passive and active RF/MW components possess limited performance compared to their discrete non-integrated component counterparts. One might ask in this case what is the point to implement RF and MW circuits in silicon technologies. The advantage of having a small form factor and integrating both RF/MW circuits with analog and digital circuits can increase a system's performance and reduce the overall cost. In the next subsection, the models of major passive and active integrated circuit components are examined, to understand where the limitation of these components arises.

2.2.1 Passive Components

Resistors in packaged form can be found with low tolerances and in all sorts of power rating. On the contrary, the integrated resistors are usually implemented with polysilicon or most commonly referred to as "poly". This is the polycrystalline form of silicon which has a fairly high conductivity, but is still less conductive than a metal. This results in the resistance range from this material to be in the moderately low-value range. These resistances are often calculated by knowing the geometry of the resistor and the resistivity of the material. The resistivity depends on the doping (if there is any doping) and composition. Often the resistance tolerance of such a device is approximately 35% and for RF/MW poly resistance the resistance tolerance is very loosely placed in the 50% range. The temperature coefficient of such a resistor is in the neighbourhood of $1000 ppm/^{\circ}C$.

Another aspect of such resistors worth mentioning is that they always have a parasitic capacitance to the silicon substrate. This capacitance is caused by the physical geometry of the device, and it makes the polysilicon resistance essentially a three terminal device. This parasitic capacitance is fairly low, but can cause the resistance to short-circuit to the substrate at higher frequencies.

In the standard IC processes, the lack of good inductors is the most obvious shortcoming. An octagonal-planar-spiral inductor can be seen in Fig. 2.9(a). These are implemented usually on the top metal layer (M_T) where the thickness of the

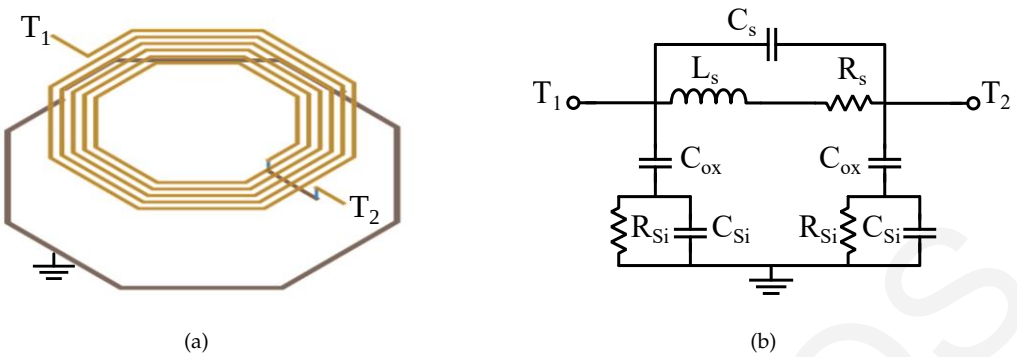


Figure 2.9: Octagonal-planar-spiral inductor. (a) three dimensional view can be seen and in (b), the lumped circuit model [59, 60].

metal is usually thicker. The metal below the top metal layer (M_{T-1}) is also used to wire the second terminal (T_2) to the boundary of the device. A metallic ring is often placed around the inductor on the first metal layer (M_1) to act as a noise isolating shield. In the past, rectangular-planar-spiral inductors were the norm, but since then octagonal-planar-spiral inductor have been adapted since they possess a higher quality factor.

The equivalent lumped circuit model of a planar spiral inductor can be seen in Fig. 2.9(b). The model, contains many parasitic elements and it is far from ideal. Although the calculation for the parasitic elements varies between rectangular and octagonal inductors, the model shown in Fig. 2.9(b) can still be adapted.

In the lumped model in Fig. 2.9(b), the inductance (L_s) is in series with the resistance (R_s) that models the resistive losses from the conductor. A capacitance (C_s) is placed in parallel to the inductive and resistive component. This capacitance is caused by the capacitance between the turns of the inductor. Two capacitances are placed in parallel to model the oxide effect (C_{ox}), which is below the inductor. In series with these capacitances a parallel resistance (R_{Si}) and capacitance (C_{Si}) connection is placed to model the losses and capacitance effect caused by the lossy silicon substrate. This parasitic elements are not negligible since the planar-spiral inductors have a large size and are close in the vicinity to the silicon substrate. With the contribution off all these parasitic elements, the overall quality factor of IC planar spiral inductor is around 20, and their self-resonant frequency is relatively low.

Capacitors in mainstream IC technologies can be made with all the interconnection metal layers. Metal structures in this maner can form parallel-plate capacitors. Although this is straight forward, using these metals will result in a larger compo-

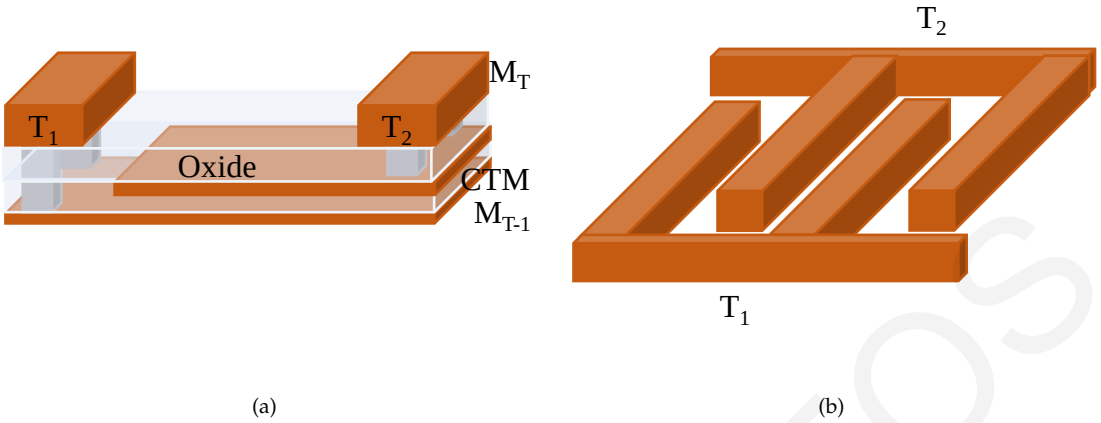


Figure 2.10: Passive capacitor types found in IC technologies. (a) Metal insulator metal (MiM) capacitors and (b), Metal oxide metal (MoM) capacitors [60,61].

nent size for a given capacitance. In order to further reduce the component's size MiM capacitors and metal oxide metal (MoM) capacitors [60,61] are preferred in the mainstream IC technologies. These types of capacitors can be seen in Fig. 2.10.

MiM capacitors (Fig. 2.10(a)) are essentially parallel plate capacitors which use a dedicated CTM layer which is insulated from the bottom plate of the capacitor with a much thinner oxide layer. This oxide layer is 20 times thinner than regular oxide layers. With the oxide layer thickness reduction, these capacitors are much more compact, but with the compromise of having a smaller breakdown voltage. MoM capacitors (Fig. 2.10(b)) are similar to interdigitated capacitors used in MW designs. These capacitors offer a larger capacitance per area due to their increased area with relatively higher break down voltage. Many metal layers can be used in these capacitors to further increase their capacitance. MoM capacitors posses on the other hand higher parasitic inductive components, which makes their self resonant frequency lower compared to MiM capacitors.

The models provided with the PDK are often accurate for passive components, but with an optimistic quality factor. For passive components, like planar inductors and MiM/MoM capacitors, one can simulate their response using full-wave simulators, such as ANSYS HFSS™ software. Information in the PDK can be found on the layer's material and thickness, which make this possible. Unfortunately, in the majority of PDKs the oxide layer's dielectric constant might be provided without any information for the losses in the dielectric. In this case extra design step can be taken to measure the dielectric constant of the oxide layer before simulating these components.

2.2.2 Active Components

A variety of active components can be found in common IC processes. The majority of these components are variations of the classic metal–oxide–semiconductor field-effect transistor (MOSFET). MOSFET implementations of both variable resistors (varistors) and variable capacitors (varactors) can be found in most PDKs.

Implementing a varistor with a MOSFET is straight forward. By applying a gate-to-source voltage the resistance between drain and source (r_{ds}) can be set. One can recall that this resistance for a long channel MOSFET in the triode region can be calculated with [60]:

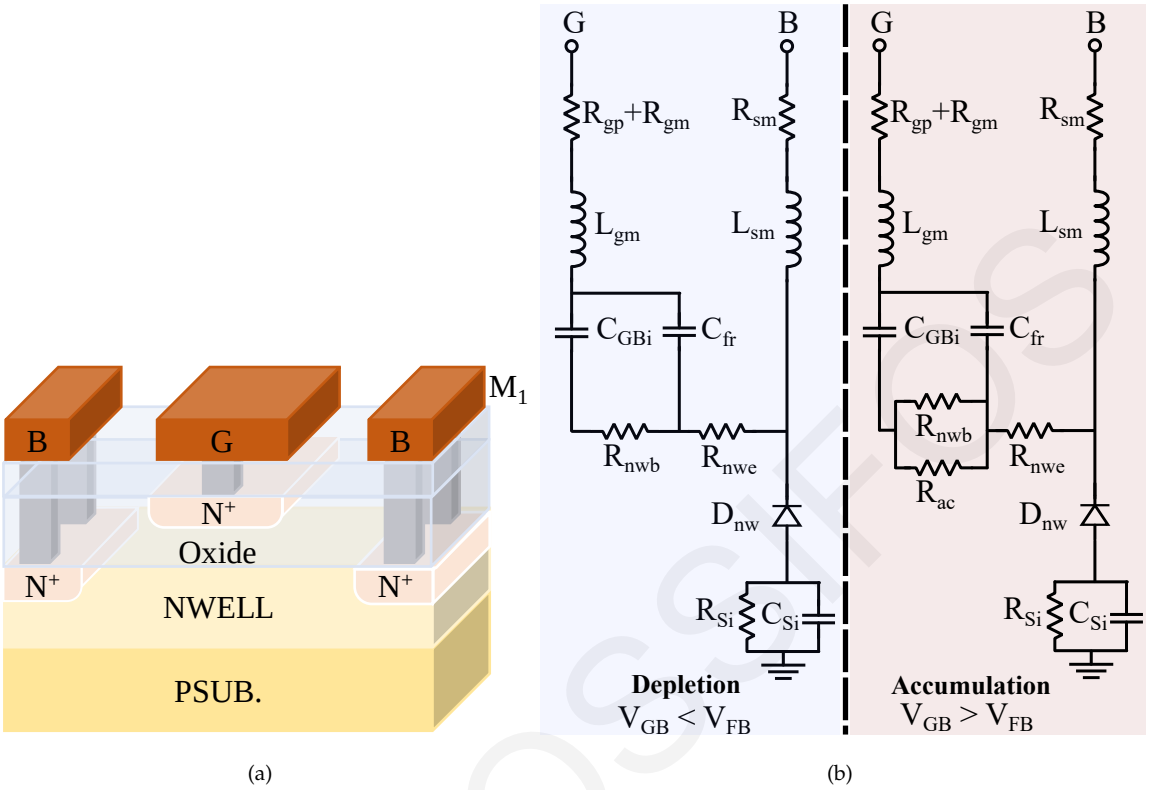
$$r_{ds} \simeq \left(\mu_e C_{ox} \frac{W}{L} \left((V_{GS} - V_T) - V_{DS}\right)\right)^{-1} . \tag{2.37}$$

A MOSFET varistor is relatively small in size and possesses a small parasitic capacitance but it has loose tolerances, because it depends on the mobility (μ_e) and threshold V_T. Similarly, the device is also temperature dependent because of the mobility (μ_e) and threshold voltage V_T are temperature dependent. Furthermore, the device is nonlinear since it is not only dependent on the gate source voltage (V_{GS}), but it is also dependent on the drain source voltage (V_{DS}).

A MOSFET type varactor's cross section can be seen in Fig. 2.11(a) and its lumped element model can be seen in Fig. 2.11(b). The MOSFET type varactor uses a n^+ drain and source diffusion in an n-well, while combining the drain and source to a terminal (the bulk (B)). These types of varactor's tunable operation is granted by the attraction and repulsion of electron carriers in the n-well, which will essentially increase or decrease the bottom part of a parallel plate capacitor's plate below the gate (G). The thin isolating oxide layer below the gate (G) grants MOSFET type varactor devices much larger capacitance for a given area compared MiM and MoM capacitors. This oxide layer has a fairly low break down voltage but the advantage of these types of capacitors is that they are tunable [60, 62].

Two lumped models are used for this device operation. One for the depletion region ($V_{GB} < V_{FB}$), and one in accumulation ($V_{GB} > V_{FB}$) (Fig. 2.11(b)). One can and choose the appropriate lumped element model when calculating the components values [60]. This devices are often stacked together and connected in parallel to create a new components with a much higher capacitance.

In the model there is a silicon resistance(R_{Si}) and capacitance(C_{Si}), and a diode (D_{nw}) that is formed between the n-well and the P-type substrate. Parasitic induc-



(a) (b)

Figure 2.11: MOS varactor. (a) Cross section of MOSFET varactor and (b), lumped circuit model [60, 62].

tance and resistance are used in the lumped circuit model to model the connection losses in both the bulk (R_{sm}, L_{sm}) and gate (R_{gp}, R_{gm}, L_{gm}) terminals. The tunable capacitance (C_{GBi}) is in parallel with a fringing field static capacitance (C_{fr}). In the n-well there are losses which are accounted for by the accumulation (R_{nw}, R_{ac}) and depletion (R_{nw}) operation. These losses are dependent on the geometry and doping of the channel and therefore they can be minimized. One can reduce the distance between the gate and the bulk and reduce these losses and in turn increase the quality factor of the varactor. This distance is often referred to as the gate length and is often set to the minimum resolution for the given technology. A significant portion of the resistance though is attributed to the lightly doped n-well contact region (R_{nwe}), and its not dependent on the gate length and thus provides the limiting factor for the varactor's quality factor.

2.3 Measurement Techniques

For the development of the IC-equipped MSF, multiple RF/MW measurements were needed to be performed. From the validation of the IC's components, to

the measurement of the far field (FF) of the MSF. This section is meant to provide the necessary background information to understand the terminology for on-wafer, connectorized and antenna measurement techniques.

2.3.1 RF and MW Measurement Techniques

RF and MW measurements for an IC design are implemented in all the design stages. On-wafer measurements are initially performed before the IC is packaged. These on-wafer measurements are meant to test the functionality of an IC design with possible probe access to its sub-circuit components. This design step mitigates the risk and catches potential faults early in the design cycle, and subsequently reduces the cost of a product. These on-wafer measurements are also used by the foundries for characterizing the RF and MW components used in the PDK.

The final measurements are implemented when the IC design has been packaged. In order to perform these measurements the IC is soldered to a PCB from where a coaxial interface is also soldered. An example of a two-terminal surface mount device (SMD) measurement can be seen in Fig. 2.12(a). Any waveguide structure can be used to connect the SMD to a coaxial interfaces from which the vector network analyser (VNA)'s cables can be connected. This particular example uses a coplanar waveguide with ground (CPWG).

A measurement from the VNA will be a measurement of all the components connected to it, a cascade of the cables, coaxial connectors, on-PCB waveguide and the device under test (DUT), in this case the SMD. The response of the cables can be calibrated out with the use of coaxial standards. This will bring the reference plane up to the coaxial connectors. The remaining effect of the connectors and waveguides will remains in the measurement and their affect is not negligible. In order to remove this effect and move the measurement plane to the device plane, one can design and use PCB standards and perform a calibration to obtain DUT response. Calibration standards can be manufactured for short-open-load-through (SOLT), line-reflect-reflect-match (LRRM), line-reflect-match (LRM) and thru-reflect-line (TRL) calibrations. The mathematical calculations of such a calibration is often implemented in the VNA software. Such calibration procedures are susceptible to the variations between standards and the precise load value. Although these procedures might be simple, special cases exist where a two-tier methods are used.

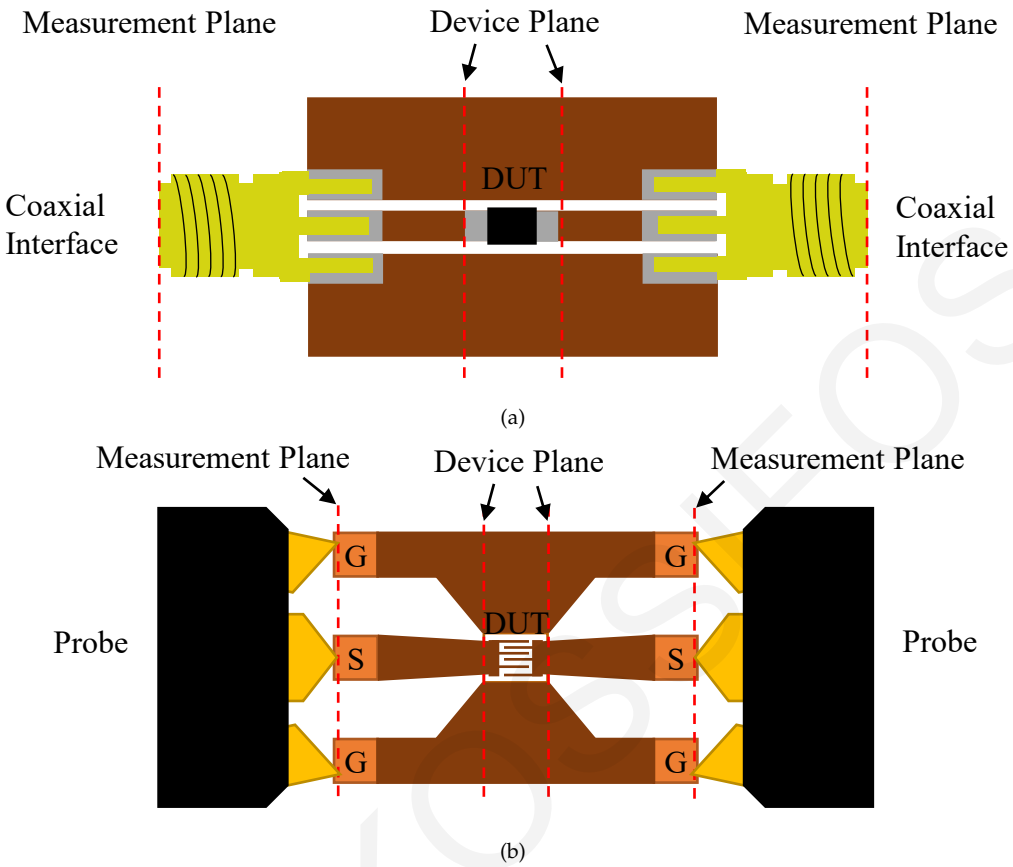


Figure 2.12: A device under test in its measurement structure for (a) connectorized measurement, and (b) on-wafer measurement. The measurement and device plane is shown in both structures.

In these methods the first step involves a calibration to remove the cable effect and then extra structures are used to move the measurement plane to the DUT plane. This extra step is often called de-embedding.

Specific techniques have been developed for on-wafer measurements, like any other RF and MW measurement technology. Often the techniques used in one technology can be transferable to other technologies (for example from on-wafer to packaged PCB measurements) with some adaptation. The methodology in both cases requires a priori knowledge of the device under test (DUT) and its operation. Special structures are designed for the measurement of a device. These structures are used to connect the DUT to the measurement apparatus.

The apparatus involves a VNA, special needle like probes, and coaxial cables to connect the VNA to the probes. When an active device needs to be measured, bias-Tee components are needed, which are often built-in to the VNA.

The probes and cables can be calibrated out from the VNA measurement, just like any other RF and MW measurement. The calibration even follows the same mathematical formulation, but differs in the calibration standards, which are pla-

nar and needs an additional alignment procedure compared to its coaxial counter parts. Planar standards often provide standards for SOLT, LRRM, LRM and TRL calibration.

A measurement at this point will include the connectors' response, and its measurement plane is at the tips of the needle like probe (see Fig. 2.12(b)). This measurement is often termed a RAW measurement. The metallization used to connect the DUT to the probe will effect the measurement, and its response is not negligible, even though these structures are electrically small. In order to move the measurement plane to the device plane or in short de-embed these structures on the left and right of the DUT from the measurement, special structures, or de-embedding structures are used. One might ask why not use the same mathematical formulation used in the calibration procedure. The answer is that the calibration procedures (except TRL [63]) involve precise loads which are hard to obtain in the mainstream IC technologies. This difficulty in obtaining precise load standards was the drive to develop new procedures, as outline below.

2.3.1.1 Open-Short De-embedding

The open-short (OS) de-embedding procedure is the simplest procedure [64, 65]. The mathematical formulation for this procedure is identical for on-wafer and packaged measurements. An example measurement structure used to measure the RAW S-parameter data for a two-port on-wafer measurement can be seen in Fig. 2.13(a). The measurement structure contains two GSG pads. The grounds in this structure are connected to enclose the DUT (in this example the MoM capacitor). The signal pads are connected to the terminals of the MoM capacitor. Often this connection is implemented with tapered lines to increase the measurement frequency bandwidth. These capacitors often have a guard ring, which is the implemented in lower layers, this ring is again connected to the ground pads.

An example structure to measure the RAW S-parameter can be seen in Fig. 2.13(b). The structure is very similar to the on-wafer case. Here the DUT is a simple SMD and it is connected to a coplanar waveguide (CPW). The CPWs extend to the edge of the PCB, where they connect to the RF connectors. Other types of PCB transmission lines (TLs) can be used for this purpose, like microstrip and coplanar stripline and many types of connectors and they will all go through the same mathematical

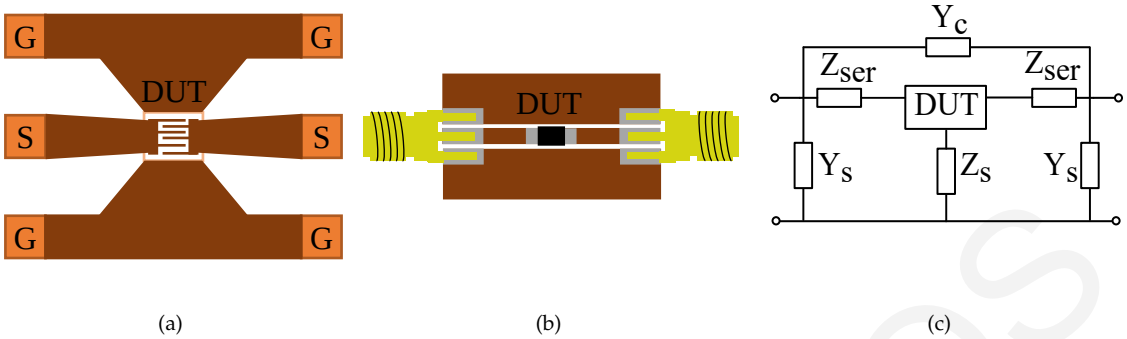


Figure 2.13: RAW examples structures used for, (a) on-wafer, (b) packaged measurements, and (c) their equivalent lumped circuit model. In (a) a MoM capacitor is used as the DUT and in (b) an SMD component.

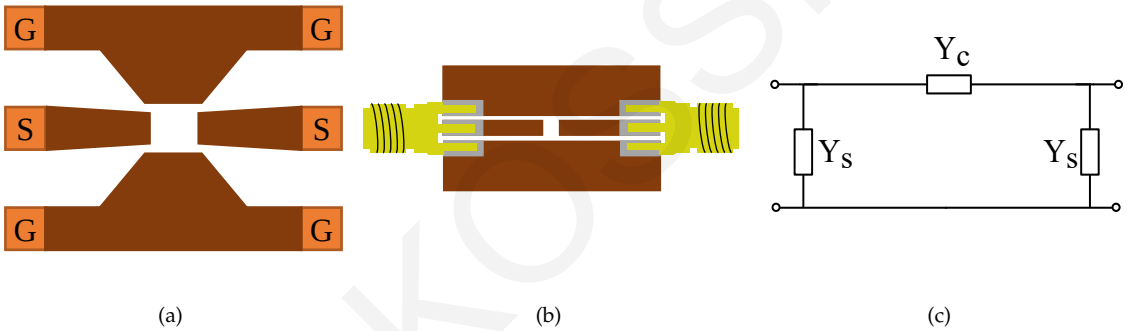


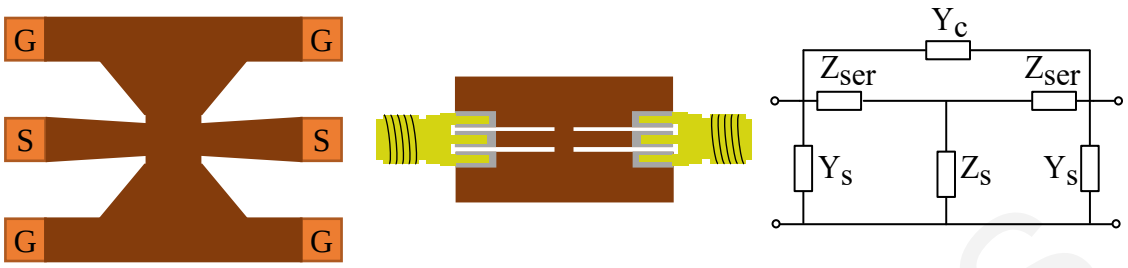
Figure 2.14: OPEN device examples for (a) on-wafer, and (b) package measurement. (c) The equivalent lumped circuit model of the OPEN devices.

analysis show in this section.

A lumped element equivalent of the measurement structures shown in Fig. 2.13(a) and Fig. 2.13(b) can be seen in Fig. 2.13(c). The DUT in the middle is connected to a network of complex impedances (Z) and admittances (Y). These impedance and admittance values are dependent to the overall structure used to connect the DUT.

These impedances and admittances are measured with the use of two de-embedding structures. The admittances are obtained from an OPEN device shown in Fig. 2.14(a) for on-wafer measurement, and an OPEN device shown in Fig. 2.14(b) for packaged measurements. These devices are basically the structure in Fig. 2.13(a) and Fig. 2.13(b) but without the DUT. The equivalent lumped circuit model of the OPEN device can be seen in Fig. 2.14(c).

The impedances are obtained from a SHORT device, shown in Fig. 2.15. In Fig. 2.15(a) a SHORT device is shown for on-wafer measurements and in Fig. 2.15(b) a SHORT device is shown for packaged measurements. These devices are identical to the structures in Fig. 2.13(a) and Fig. 2.13(b) but with a metal where the DUTs



(a) (b) (c)

Figure 2.15: SHORT device examples for (a) on-wafer, and (b) package measurement. (c) The equivalent lumped circuit model of the SHORT devices.

used to be. This effectively shorts the signal pads to the ground. The equivalent lumped circuit model of the short device can be seen in Fig. 2.15(c), and it contains both the admittances and the impedances.

These three structures (RAW, OPEN and SHORT) are measured and the obtained S-parameter have the following format:

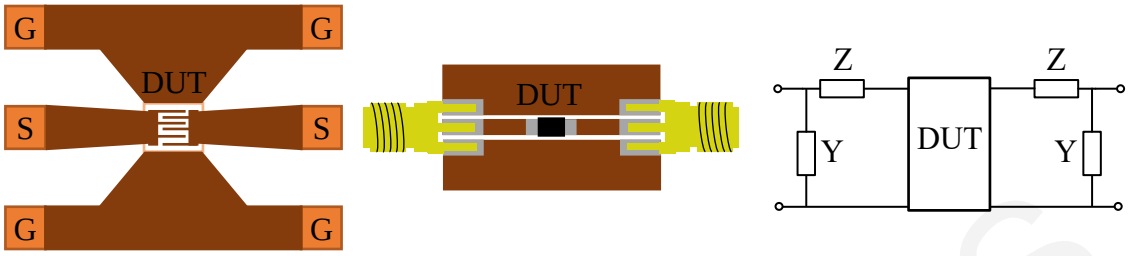
$$S = \begin{bmatrix} S_{11}(f) & S_{12}(f) \\ S_{21}(f) & S_{22}(f) \end{bmatrix}, \tag{2.38}$$

where the dependency in frequency (f) is discrete. These S-parameters can be transformed into Z-, Y-, T- and ABCD-parameter matrices [58,66] and these matrices properties can be exploited for the sake of the de-embedding procedure. The first step to the open-short (OS) de-embedding is to remove the admittances. This is done by converting the RAW's S-parameter to Y-parameters. A simple subtraction of these two Y-parameter will remove the admittances and a new Y-parameter with open de-embedded is obtained, Y_{DO}. Since the same shunt admittance is also present on the SHORT equivalent circuit, the SHORT device is also converted to Y-parameters to perform the same subtraction and obtain Y_{SO}:

$$Y_{DO} = Y_{RAW} - Y_{OPEN}\,,\; Y_{SO} = Y_{SHORT} - Y_{OPEN} \tag{2.39}$$

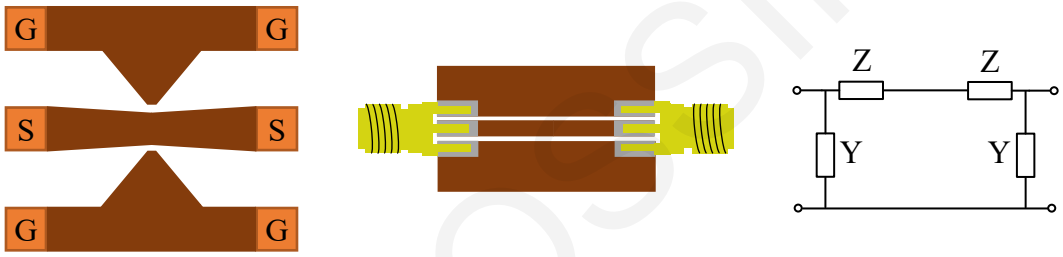
The final step involves converting the Y-parameters to Z-parameters obtained from (2.39) to obtain Z_{DO} and Z_{SO}. The subtraction of these two, will result in the Z-parameter of the DUT (Z_{DUT}).

$$Z_{DUT} = Z_{DO} - Z_{SO} \tag{2.40}$$



(a) (b) (c)

Figure 2.16: RAW examples structures used in the through de-embedding for (a), on-wafer and (b) packaged measurements. (c) Their equivalent lumped circuit model.



(a) (b) (c)

Figure 2.17: THRU examples structures used in the through de-embedding for (a), on-wafer and (b) packaged measurements. (c) Their equivalent lumped circuit model.

This Z-parameters can be converted now into any other parameter to be processed. This procedure can be easily converted to one-port de-embedding procedure [67], and even improved [68].

2.3.1.2 Through De-embedding

Through de-embedding needs only one de-embedding structure, and it is conceptually a simple procedure [64, 69]. For this procedure, the DUT is embedded in two connectors that have complete symmetry. An example structure of on-wafer measurements can be seen in Fig. 2.16(a) and for packaged measurements in Fig. 2.16(b). The connectors are modelled with a shunt admittance (Y) and series impedance (Z) on both sides of the DUT, as can be seen in Fig. 2.16(c).

The de-embedding structure in this procedure, the THRU, (Fig. 2.17(a) and Fig. 2.17(b)) is the RAW structure with the DUT removed while directly connecting the two signal traces in the middle and without changing the trace length. In the same way the THRU equivalent lumped circuit model (Fig. 2.17(c)) is the same as

the RAW equivalent circuit model with the DUT shorted in the center.

The RAW in the procedure is treated as a cascade of three components, the left branch (LEFT), the DUT and the right (RIGHT). This cascade can be mathematically expressed using either ABCD- or T-parameter matrices and subsequently takes the following form:

$$T_{RAW} = T_{LEFT} \times T_{DUT} \times T_{RIGHT}, \tag{2.41}$$

while the THRU structure is only the cascade of the left and right branch will take the following form:

$$T_{THRU} = T_{LEFT} \times T_{RIGHT}. \tag{2.42}$$

One can imagine that the easier way to obtain the T_{LEFT} or the T_{RIGHT} would be $T_{LEFT} = T_{RIGHT} = \sqrt{T_{THRU}}$, but this would enforce that both are equal and symmetrical. A better approach involves the conversion to Y-parameters. The Y-parameters of the THRU are:

$$Y_{THRU} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}, \tag{2.43}$$

which can be easily converted to the Y parameters of the left and right branch with:

$$Y_{LEFT} = \begin{bmatrix} Y_{11} - Y_{12} & 2Y_{12} \\ 2Y_{12} & -Y_{12} \end{bmatrix}, \tag{2.44}$$

$$Y_{RIGHT} = \begin{bmatrix} -2Y_{12} & 2Y_{12} \\ 2Y_{12} & Y_{11} - Y_{12} \end{bmatrix}. \tag{2.45}$$

The Y_{LEFT} and Y_{RIGHT} can be now converted to the T-parameters and the DUT T-parameters can be obtained with the following equations:

$$T_{DUT} = T_{LEFT}^{-1} \times T_{RAW} \times T_{RIGHT}^{-1}. \tag{2.46}$$

The through de-embedding procedure can be easily calculated, and only needs one de-embedding structure which saves space. Its simplicity though comes with its shortcoming of not having a way to adjust the reference plane, and therefore it relies heavily on the design of the THRU structure.

2.3.1.3 Open-Short-Through De-embedding

A combination of the aforementioned de-embedding techniques (OS and Through) is the open-short-through (OST) de-embedding technique [64, 70]. In this procedure, the connectors,which are represented with a shunt admittance and a series

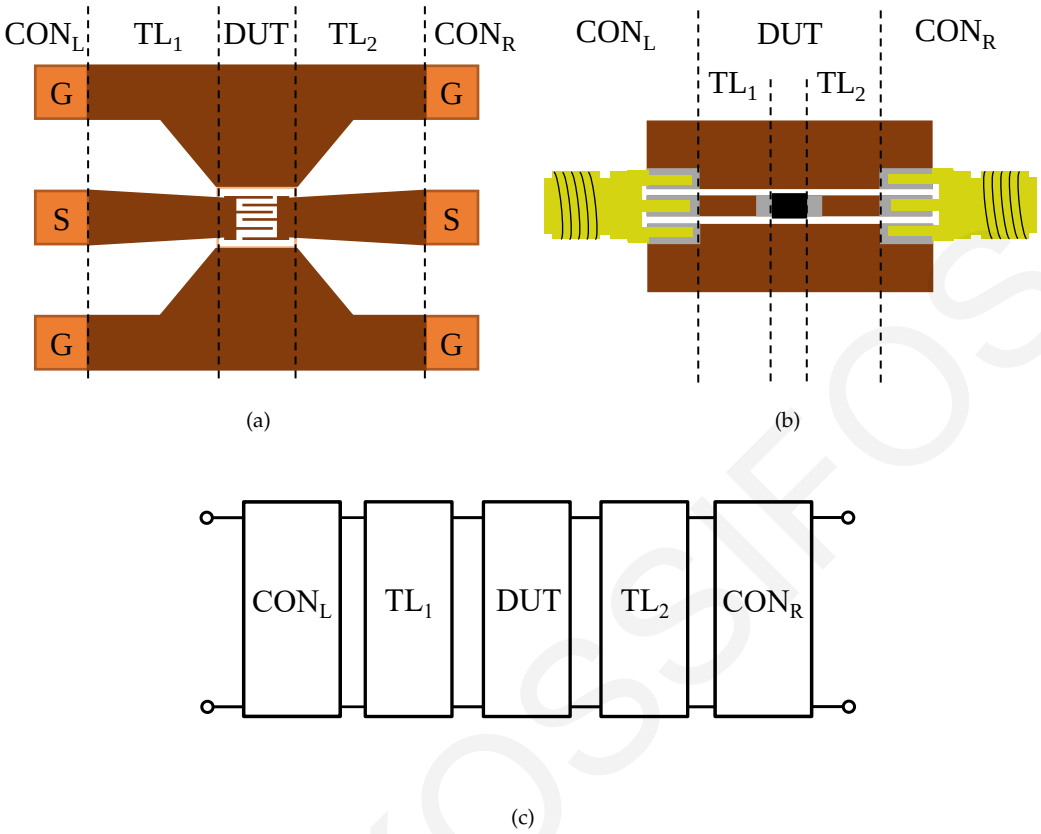


Figure 2.18: Raw devices for OST de-embedding for (a) on-wafer, and (b) for packaged measurements. (a) and (b) show individually all the components, the connectors (CON_L and CON_R) , the transmission lines leading to the DUT (TL_1 and TL_2) and the DUT.(c) Cascade representation T or ABCD matrices of the RAW device.

impedance, are de-embedded first. The next step is to de-embed the transmission line that connects the on-wafer pads or connectors (*CON.*) to the DUT.

The RAW devices for an OST de-embedding can be seen in Fig. 2.18(a) and Fig. 2.18(b) for on-wafer and packaged measurements. The device is considered to consist of a cascade of connectors (CONs) and transmission lines (TLs) to connect to the DUT, which will be de-embedded using their corresponding de-embedding device. A network representation of this device can be seen in Fig. 2.18(c). This network can be expressed mathematically using ABCD parameters matrices with:

$$RAW = CON_L \times TL_1 \times DUT \times TL_2 \times CON_R. \tag{2.47}$$

The CONs T-parameters are formulated by measuring the OPEN (Fig. 2.19(a) & Fig. 2.19(b)) and SHORT (Fig. 2.20(a) & Fig. 2.20(b)) devices. Similarly to the OS procedure, the S-parameters are transformed to Y- and Z-parameters. The equivalent lumped element circuit model of the OPEN and SHORT devices can be found in

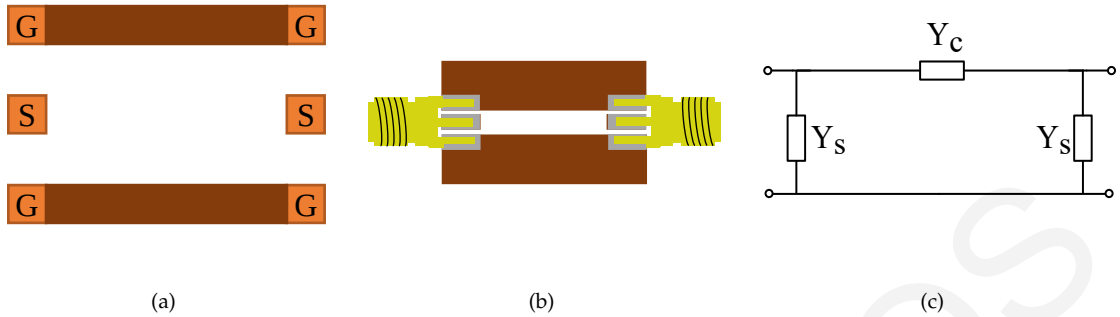


Figure 2.19: Example for OPEN device used in the OST measurement procedure for (a) on-wafer and (b) packaged measurement. In (c) their equivalent lumped circuit model is shown.

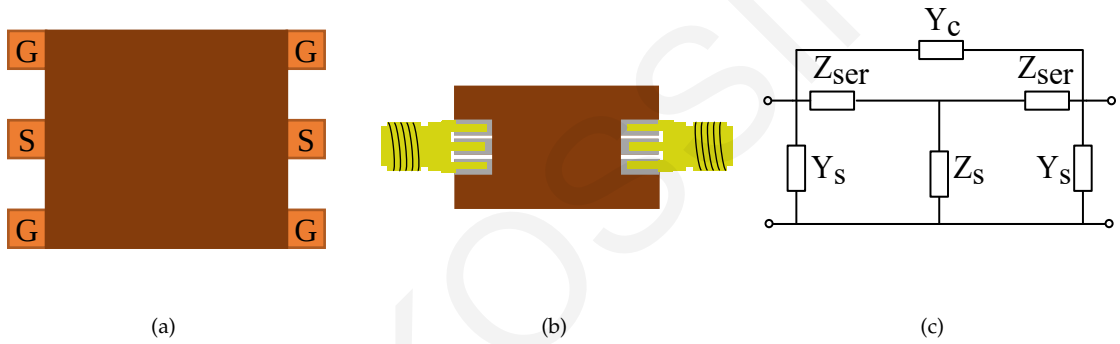


Figure 2.20: Example of SHORT device used in OST procedure for (a) on-wafer and (b) packaged measurements. (c) SHORT's equivalent lumped circuit mode.

Fig. 2.19(c) and Fig. 2.20(c) respectively.

The shunt admittance (Y_s) of the CONs can be extracted from the OPEN device's Y-parameters using :

$$Y_s = Y_{11OPEN} + Y_{12OPEN}. \tag{2.48}$$

In order to obtain the series impedance (Z_{ser}) of the CONs, the intermediate Z_D matrix is calculated from the OPEN and SHORT Y-Parameters using:

$$Z_D = (Y_{SHORT} - Y_{OPEN})^{-1}. \tag{2.49}$$

Then the series components is isolated by :

$$Z_{ser} = Z_{11D} - Z_{12D}. \tag{2.50}$$

The CONs ABCD matrices can be formulated using:

$$CON_L = \begin{bmatrix} 1 & Z_{ser} \\ Y_s & 1 + Z_{ser}Y_s \end{bmatrix}, \tag{2.51}$$

$$CON_R = \begin{bmatrix} 1 + Z_{ser}Y_s & Z_{ser} \\ Y_s & 1 \end{bmatrix}. \tag{2.52}$$

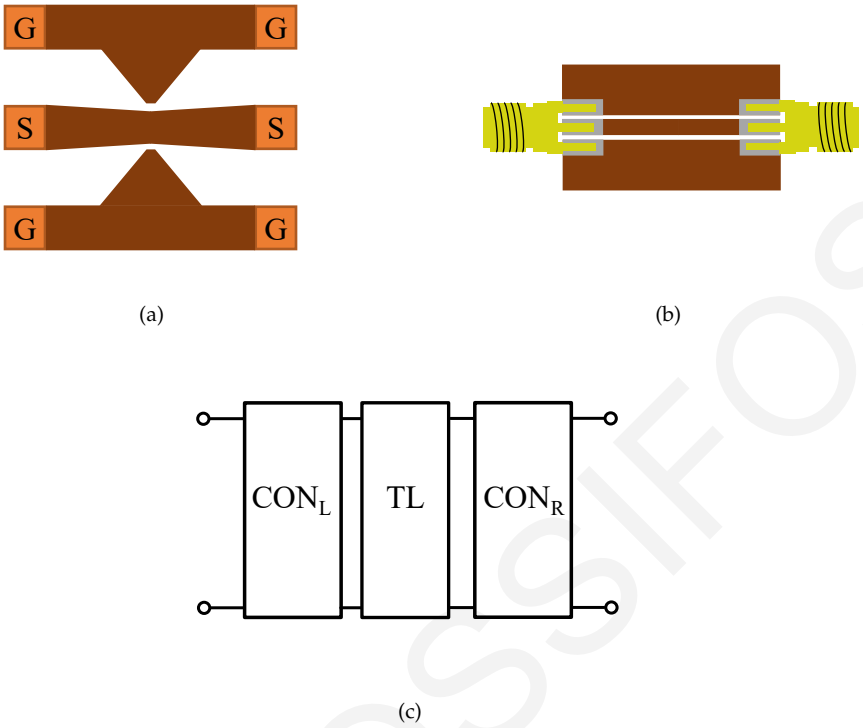


Figure 2.21: THRU device used in OST procedure for (a) on-wafer and (b) packaged measurements. (c) THRU's equivalent cascade of ABCD matrices.

The THRU devices as shown in Fig. 2.21(a)and Fig. 2.21(b) are conciser to be a cascade of the CONs and a transmission line (TL) as shown in Fig. 2.21(c). This can be represented with a cascade of ABCD matrices:

$$THRU = CON_L \times TL \times CON_R. \tag{2.53}$$

With the CON parameters already known, one can solve for the ABCD parameter of the TL using:

$$TL = CON_L^{-1} \times THRU \times CON_R^{-1}. \tag{2.54}$$

The characteristic impedance (Z_c) and the propagation constant (γ) of the TL can be found from the S-parameters of the TL (S_{TL}) using:

$$Z_c = \pm Z_0 \sqrt{\frac{(1+S_{11TL})^2 - S_{21TL}^2}{(1-S_{11TL})^2 - S_{21TL}^2}}, \tag{2.55}$$

$$\gamma = -\frac{1}{l} \ln\left[\left(\frac{1 - S_{11TL}^2 + S_{21TL}^2}{2S_{21TL}} \pm K\right)^{-1}\right], \tag{2.56}$$

where K can be found from:

$$K = \sqrt{\frac{\left(1 - S_{21TL}^2 + S_{11TL}^2\right) - (2S_{11TL})^2}{(2S_{21TL})^2}} \tag{2.57}$$

Then the ABCD matrices of a TL of any physical length (l) can be formulated using:

$$TL = \begin{bmatrix} \cosh(\gamma l) & Z_c \sinh(\gamma l) \\ \frac{1}{Z_c}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix}. \tag{2.58}$$

TL_1 and TL_2 can be formulated by replacing the physical length (l) with their corresponding physical length. Finally, with the obtained the TLs and CONs ABCD parameters, now can be removed from the RAWs ABCD parameters to obtain the DUT response using:

$$DUT = TL_1^{-1} \times CON_L^{-1} \times RAW \times CON_R^{-1} \times TL_2^{-1} \tag{2.59}$$

One can infer from this analysis that the CONs are considered as lumped elements while the TL are distributed elements. This assumption enforces in the design of the de-embedding structures that the OPEN and SHORT device should be electrically small, while the THRU device should be relatively large. This makes the occupied on-wafer area required for this de-embedding procedure to become large and relatively costly. That being said, the size might not be an issue when this technique is used for packaged component measurements. Furthermore, the admittance term Y_c in Fig. 2.19(c) and the impedance Zs in Fig. 2.20(c) are omitted in the OST procedure, so great care should be taken in the de-embedding structure to minimize these components.

2.3.1.4 L-2L De-embedding

The length - 2 length (L-2L) is a distributed de-embedding technique involving two transmission-line-based de-embedding structures [64, 71–73]. An on-wafer measurements example RAW, and de-embedding structures for L-2L can be found in Fig. 2.22. The RAW (Fig. 2.22(a)) is symmetrically embedded in two transmission lines (TLs) and two connectors (CONs). Subsequently, this cascade of the RAW structure can be expressed with T-matrices and has the following form:

$$RAW = CON \times TL \times DUT \times TL \times CON. \tag{2.60}$$

The two transmission-line de-embedding structures used in this procedure are also a cascade of CONs and TLs. The 2L (Fig. 2.22(b)) structure consist of by CONs and two TL sections, while the L (Fig. 2.21(c)) consist of CONs and only one TL. The 2L and L structures can be expressed with T-matrices with:

$$2L = CON \times TL \times TL \times CON, \tag{2.61}$$

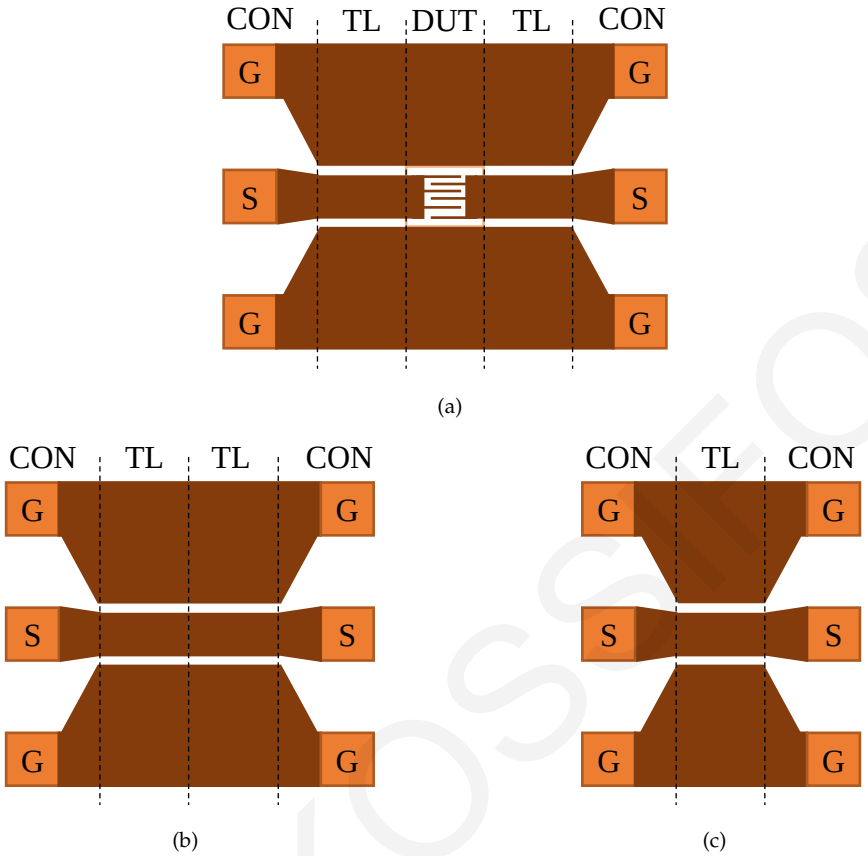


Figure 2.22: Example structures for L-2L characterization of a MoM capacitor (a) RAW device for L-2L, (b) 2L and (c) L.

$$L = CON \times TL \times CON. \tag{2.62}$$

Similarly one can design the electrically equivalent structures with a PCB technology for packaged component measurements. Example structures for RAW, 2L and L can be found in Fig. 2.23. In contrast with the OS and OST methods the L-2L method considers that the CONs are distributed elements. The CONs in this case can be extracted from the L and 2L T-parameters using:

$$CON = \sqrt{L \times 2L^{-1} \times L}. \tag{2.63}$$

After obtaining the T parameters of the CONs, one can remove them from the L structure's T-parameter to get the TL's T-parameters using:

$$TL = CON^{-1} \times L \times CON^{-1} \tag{2.64}$$

Finally, with the CON and TL's T-parameters obtained, now the DUT's response can be calculated using:

$$DUT = TL^{-1} \times CON^{-1} \times RAW \times CON^{-1} \times TL^{-1} \tag{2.65}$$

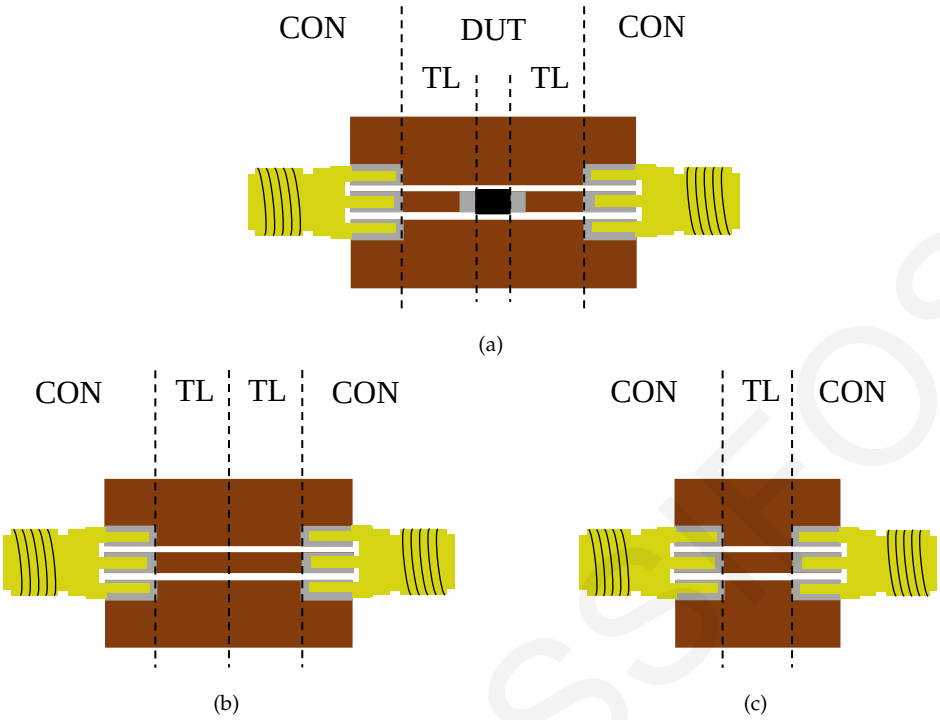


Figure 2.23: Example structures for L-2L characterization of a two port SMD, (a) RAW device for L-2L, (b) 2L and (c) L.

2.3.1.5 TRL Calibration

The measurement methods described prior in this section were a two-step process which required that a calibration would be performed to move the measurement reference plane to the probe tips or the end of the coaxial cables. From there, the DUT response would be extracted from the RAW measurement with the use of de-embedding structures and mathematical manipulation of all the measurements.

The TRL method doesn't require any prior knowledge of the calibration standards and doesn't need any precise load. This make this method desirable for on-wafer and packaged measurements. The method's disadvantage is that it relies on the LINE standard to sets the characteristic impedance of the measurement.

Example structures for TRL calibration can be seen in Fig. 2.24. Three calibration standards which are used are the THRU (Fig. 2.24(b)), the REFLECT (Fig. 2.24(c)) and the LINE (Fig. 2.24(d)). Depending of the physical length of the calibration standards and namely the lengths l_1 and l_2 the reference plane will be moved by this distance in the RAW measurement (Fig. 2.24(a)) .

When the TRL procedure was first presented in 1979 [63], it involved manipulations of R-parameters which are not commonly used today. R-parameters are essentially T-parameters where the individual matrix entries are interchanged (see

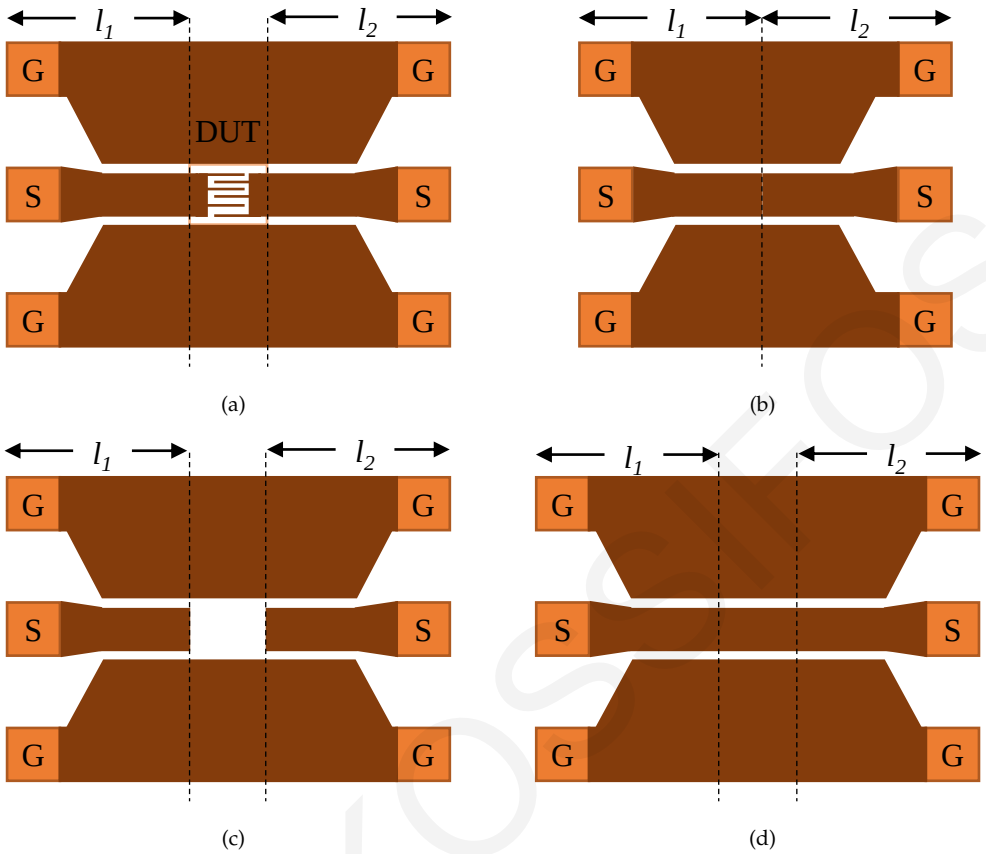


Figure 2.24: On-wafer structures for TRL calibration (a) RAW device, (b) THRU,(c) REFLECT and (d) LINE.

(2.66)). Furthermore, the algorithm relies on choosing the correct solution from quadratic equations depending on the type of reflection standard used. This makes the implementation of this algorithm particularly difficult.

$$R = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix}, \qquad T = \begin{bmatrix} R_{22} & R_{21} \\ R_{12} & R_{11} \end{bmatrix}. \tag{2.66}$$

For the sake of completion, the TRL calibration algorithm with the use of T-parameters is described in this section. Furthermore, the criteria used to choose the unknown terms for an open reflect standard are presented in a pseudo-code manner. The RAW measurement (Fig. 2.24(a)) can be mathematically expressed as a cascade of T-parameters:

$$T_{RAW} = T_{Left} \times T_{DUT} \times T_{Right}, \tag{2.67}$$

where T_{Left} and T_{Right} are the T-parameters of the left and right connectors to the

DUT. In this case the connectors are a contribution of CONs and TLs. Similar to the Through de-embedding procedure, the DUT can be expressed with inverse multiplications of the T-parameters :

$$T_{DUT} = T_{Left}^{-1} \times T_{RAW} \times T_{Right}^{-1}. \tag{2.68}$$

The solution begins by writing the T_{Left} and T_{Right} as:

$$\begin{aligned} T_{Left} &= \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} = t_{11} \begin{bmatrix} 1 & c \\ b & a \end{bmatrix}, \\ T_{Right} &= \begin{bmatrix} \tau_{11} & \tau_{12} \\ \tau_{21} & \tau_{22} \end{bmatrix} = \tau_{11} \begin{bmatrix} 1 & \gamma \\ \beta & \alpha \end{bmatrix}. \end{aligned} \tag{2.69}$$

Where the parameters in (2.69) are unknown (t_{11}, a, b, c, τ_{11}, α, β, γ). Their inverse matrices can be expressed as:

$$\begin{aligned} T_{Left}^{-1} &= \frac{1}{t_{11}} \frac{1}{a - b\,c} \begin{bmatrix} a & -c \\ -b & 1 \end{bmatrix}, \\ T_{Right}^{-1} &= \frac{1}{\tau_{11}} \frac{1}{\alpha - \beta\,\gamma} \begin{bmatrix} \alpha & -\gamma \\ -\beta & 1 \end{bmatrix}. \end{aligned} \tag{2.70}$$

The DUT's T-parameters can be found by substituting (2.70) into (2.68). There are eight unknown terms (2.71), nevertheless, it is only necessary to find seven quantities b, $\frac{c}{a}$, $\frac{\beta}{\alpha}$, $\gamma, t_{11}\tau_{11}$, $a\alpha$ *and* $e^{2\gamma l}$)

$$T_{DUT} = \frac{1}{t_{11}\tau_{11}} \frac{1}{a\,\alpha} \frac{1}{1 - b\frac{c}{a}} \frac{1}{1 - \gamma\frac{\beta}{\alpha}} \begin{bmatrix} a & -c \\ -b & 1 \end{bmatrix} T_{RAW} \begin{bmatrix} \alpha & -\gamma \\ -\beta & 1 \end{bmatrix} \tag{2.71}$$

The THRU and the LINE standard can be expressed with T-parameters similarly to the DUT:

$$\begin{aligned} T_{THRU} &= T_{Left} \times T_{Right}, \\ T_{LINE} &= T_{Left} \times T_{TL} \times T_{Right}. \end{aligned} \tag{2.72}$$

An intermediate matrix T_i is calculated by:

$$T_i = T_{LINE} \times T_{THRU}^{-1} = T_{Left} \times T_{TL}. \tag{2.73}$$

The transmission line matrix T_{TL} is considered to be non-reflecting which helps form a quadratic equation to solve for b and $\frac{c}{a}$. The quadratic equation takes the form of:

$$\begin{aligned} A = T_i(1,2), B = T_i(1,1) - T_i(2,2),\ C = -T_i(2,1) \\ K_{\pm} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \end{aligned} \tag{2.74}$$

Up on analysis, it can be identified that for any well designed transition between coaxial transmission line, to any planar transmission line there will be small reflections in the transition ($|S22| \ll 1, |S11| \ll 1$). This will produce $|b| \ll 1$ and $\frac{c}{a} \gg 1$. Therefore, the correct root is selected by:

$$\begin{aligned} &if\ (|K_+| < |K_-|) \\ &\quad \left\{ b = K_+,\ \frac{c}{a} = \frac{1}{K_-} \right\} \\ &else \\ &\quad \left\{ b = K_-,\ \frac{c}{a} = \frac{1}{K_+} \right\} \end{aligned} \tag{2.75}$$

By rearranging now the T_{THRU} matrix and knowing b and $\frac{c}{a}$ one can solve to find γ and $\frac{\beta}{\alpha}$:

$$\begin{aligned} \gamma &= \frac{S_{22THRU} + det(S_{THRU})\,\frac{c}{a}}{1 - S_{11THRU}\,\frac{c}{a}}, \\ \frac{\beta}{\alpha} &= \frac{S_{11THRU} - b}{(b\,S_{22THRU} - det(S_{THRU})}. \end{aligned} \tag{2.76}$$

Here, the term $det(S_{THRU})$ is the determinant of the S-parameter matrtix of the THRU calibration standard. Having calculated γ and $\frac{\beta}{\alpha}$, the term a can be calculated using the quadratic equation:

$$a = \pm \sqrt{\frac{(S_{11REF} - b)(1 + S_{22REF}\,\frac{\beta}{\alpha})(b\,S_{22THRU} - det(S_{THRU}))}{((S_{22REF} + \gamma)(1 - (S_{11REF}\,\frac{c}{a})(1 - S_{11THRU}\,\frac{c}{a})}}. \tag{2.77}$$

In order to choose the correct sign for a, the reflection coefficients at each port are calculated using:

$$\begin{aligned} R_{1A} &= \frac{S_{11REF} - b}{a - S_{11REF}\,a\,\frac{c}{a}}, \\ R_{1B} &= \frac{S_{11REF} - b}{a\,S_{11REF}\,\frac{c}{a} - a}. \end{aligned} \tag{2.78}$$

For an open ended REFLECT standard one can choose the correct sigh of a using:

$$\begin{aligned} &if\left(|\angle R_{1A}| < \frac{\pi}{2}\right) \\ &\{a = a\} \\ &if\left(|\angle R_{1B}| < \frac{\pi}{2}\right) \\ &\{a = -a\} \end{aligned} \tag{2.79}$$

With b, a and $\frac{c}{a}$ solved, the term α can be now calculated using:

$$\alpha = \frac{bS_{22THRU} - det(S_{THRU})}{a(1 - S_{11THRU}\frac{c}{a})}. \tag{2.80}$$

This leaves the final term $t_{11}\tau_{11}$ to be solved using (2.81):

$$t_{11}\tau_{11} = \frac{T_{22THRU}}{a\alpha + b\gamma}. \tag{2.81}$$

Finally, all the terms can be substituted into (2.71) to finalise the calibration.

2.3.2 Antenna Measurements

Antenna measurements are used to measure different characteristics of an antenna, such as radiation patterns, efficiency, bandwidth, directivity, gain and polarization just to mention a few [74]. These measurements are often conducted in anechoic chambers by measuring the transmission between two antennas. One reference antenna's parameters are known, while the second antenna's parameters are extracted from the measurement. The antenna is measured at multiple angles on a stage that can rotate.

The antenna's measured parameters are typically required at the far field (FF). The FF of an antenna is at a distance greater than the Fraunhofer distance (d_F):

$$d_F = \frac{2D^2}{\lambda}, \tag{2.82}$$

where D is the largest geometrical dimension of the antenna and λ is the wavelength where the measurement is carried out. Therefore, the measurement distance should be greater than d_F. For electrically small antennas, a smaller wavelength would make the Fraunhofer distance relatively small, but in the case where the radiating element is electrically large, like in the case where the radiating element is a MSF, the Fraunhofer distance becomes larger, which is impractical and even infeasible to be accommodated in a FF anechoic chamber.

Compact-range anechoic chambers are facilities that utilize multiple parabolic reflectors to measure the FF of an antenna in a more compact range, and so they can measure even larger antennas [75].

NF measurement systems are used to measure the near field of an antenna, and then using analytical methods to transform it to the FF. Analytical solutions to compute the FF can be found in the literature for planar [76,77], cylindrical [78] and spherical [79] measurements.

2.3.2.1 Far Vs Near Field Measurements

Although NF measurements can characterize an antenna that would need a very large anechoic chamber to be measured, they have inherent drawbacks. They require the precise measurement over an area to compute the FF antenna characteristics, which makes them significantly slower than FF measurements. The computational time needed to compute the FF from the NF measurement is not negligible. Both FF and NF measurement systems are prone to positioning errors and misalignment errors, as they are both implemented with mechanical positioners and actuators. For NF measurements, due to the more complex movements and larger number of measurement one can argue that they are more susceptible to these types of errors.

In terms of complexity, NF measurement systems are far more complex than FF systems, with the majority of the complexity located inside the implementation of the NF to FF transformation. In the next subsections, the analytical formulation for the NF to FF transformation is presented. It should be noted that the formulation presented is without any probe compensation.

2.3.2.2 Planar Near Field to Far Field Transformation

Assuming that a source of an electromagnetic wave, e.g a horn antenna as shown in Fig. 2.25 , is positioned at the axis origin, the radiated electric field ($\boldsymbol{E}$) observed at a distance $z_{obs.}$ can be expressed as a function of the plane wave spectrum (PWS) (F), [76,77]:

$$E(x, y, z_{obs.}) = \frac{1}{4\pi^2} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} F(k_x, k_y) e^{-j(k_x x + k_y y + k_z z_{obs.})} dk_x dk_y, \tag{2.83}$$

$$F(k_x, k_y) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E(x, y, z_{obs.}) e^{j(k_x x + k_y y + k_z z_{obs.})} dx\, dy. \tag{2.84}$$

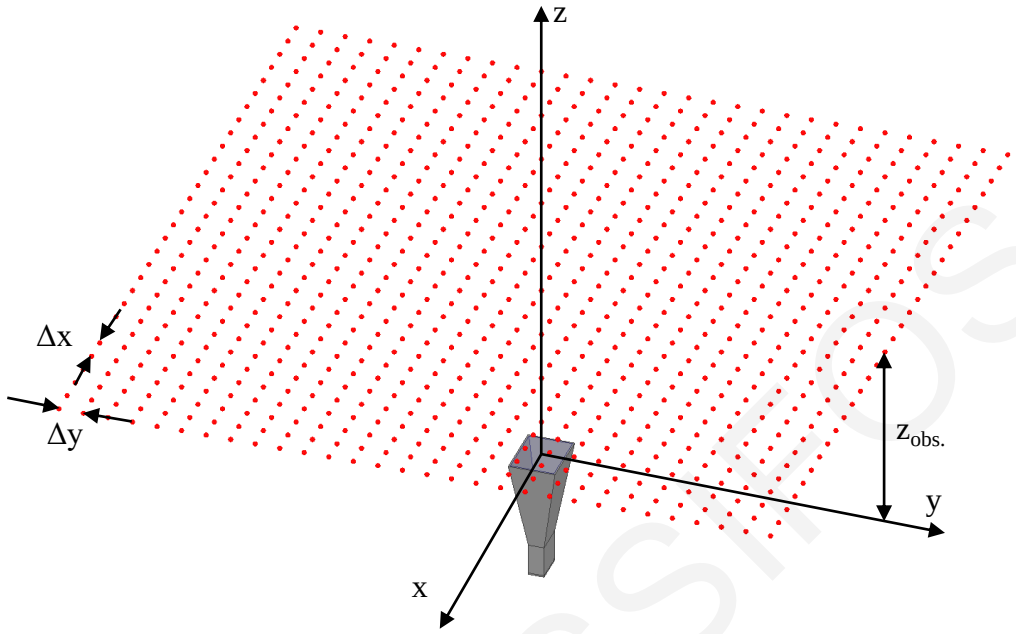


Figure 2.25: Planar near field measurement of a horn antenna. Measurement points are shown with red marker points.

In practice, the observation plane can't extend to infinity, therefore it is truncated to a finite surface, where $x_{min} < x < x_{max}$ and $y_{min} < y < y_{max}$ is observed. Furthermore, this finite surface now needs to be discretized using sampling steps Δx and Δy. After the truncation and discretization of (2.83) and (2.84), they take the following form:

$$E(x_p, y_q, z_{obs.}) \approx \frac{1}{4\pi^2} \sum_{n=1}^{N} \sum_{m=1}^{M} F(k_x^n, k_y^m) e^{-j(k_x^n x_p + k_y^m y_q + k_z^{n,m} z_{obs.})} \Delta k_x \Delta k_y, \tag{2.85}$$

$$F(k_x^n, k_y^m) \approx \sum_{p=1}^{P} \sum_{q=1}^{Q} E(x_p, y_q, z_{obs.}) e^{-j(k_x^n x_p + k_y^m y_q + k_z^{n,m} z_{obs.})} \Delta x \Delta y. \tag{2.86}$$

where, $k_z^{n,m} = \sqrt{k - k_x^n - k_y^m}$, k is the wavenumber in free space. $\Delta k_x = {}^{2\pi}/_{(x_{max} - x_{min})}$, $\Delta k_y = {}^{2\pi}/_{(y_{max} - y_{min})}$. Q and P are integer numbers calculated by $P = {}^{(x_{max} - x_{min})}/_{\Delta x} + 1$, $Q = {}^{(y_{max} - y_{min})}/_{\Delta y} + 1$. N and M are also integer numbers and are calculated by $N = {}^{(k_{xmax} - k_{xmin})}/_{\Delta k_x} + 1$ and $M = {}^{(k_{ymax} - k_{ymin})}/_{\Delta k_y} + 1$. The sampling steps Δx and Δy are set to be ${}^{\lambda}/_{2}$ to avoid discretization errors. The electric far field (E_{ff}) can then be calculated with the approximated formula:

$$\begin{aligned} E_{ff}(r, \theta, \phi) &\approx jk_z \frac{e^{jkr}}{r} F(k_x, k_y), \\ &= jk \cos\theta \, \frac{e^{jkr}}{r} F(k \sin\theta \cos\phi, k \sin\theta \sin\phi). \end{aligned} \tag{2.87}$$

2.3.2.3 Cylindrical Near Field to Far Field Transformation

The mathematical formulation for a cylindrical near-field measurement was first reported in [78]. The grid for this measurement can be seen in Fig. 2.26, where the measurement points are marked with red dots. These points surround a source, in this case a horn antenna. These measurement points are located at a radius ($r_{obs.}$), while the z-axis similarly to the planar measurement is truncated. It was shown that the tangential electric components E_ϕ and E_z on these measurement points can be represented as a truncated summation of cylindrical waves [75, 78, 80]:

$$E_\phi(r_{obs.}, \phi_p, z_q) \approx \sum_{n=-N/2}^{N/2-1} \sum_{m=1}^{M} \left[b_n(k_z^m) \frac{nk_z^m}{kr_{obs.}} H_n^{(2)}(a^m r_{obs.}) - a_n k_z^m \frac{\partial H_n^{(2)}}{\partial r}(a^m r_{obs.}) \right] e^{jn\phi_p} e^{-jk_z^m z_q} \Delta k_z, \tag{2.88}$$

$$E_z(r_{obs.}, \phi_p, z_q) \approx \sum_{n=-N/2}^{N/2-1} \sum_{m=1}^{M} \left[b_n(k_z^m) \frac{a^m}{k} H_n^{(2)}(a^m r_{obs.}) \right] e^{jn\phi_p} e^{-jk_z^m z_q} \Delta k_z. \tag{2.89}$$

The truncated cylinder is quantized in $\Delta_\phi = \pi/kr_0$ and $\Delta_z = \lambda/2$ steps [78], where r_0 is the minimum radius that can enclose the antenna under test (AUT) and λ is the wavelength. N is the number of calculated cylindrical modes, which is also truncated to a finite number to reduce the computation time. The number of modes is proportional to r_0 and it is calculated by $N = kr_0 + n_1$. n_1 is set to an integer value between 5 and 10. k_z^m is $-\pi/\Delta z \leq k_z^m \leq \pi/\Delta z$. M is the number of measurement points in the z-axis direction ($M = k_{zmax} - k_{zmin}/\Delta k_z + 1$). $H_n^{(2)}$ is the Hankel function of the second kind and order n with $a^m = \sqrt{k^2 - (k_z^m)^2}$. $b_n(k_z^m)$ and $a_n(k_z^m)$ are the cylindrical wave coefficients and can be calculated using:

$$b_n(k_z^m) = \frac{k}{a^m H_n^{(2)}(a^m r_{obs.}) \Delta k_z} \sum_{p=0}^{P-1} \sum_{q=0}^{Q-1} E_z(r_{obs.}, \phi_p, Z_p) e^{-jn\phi_p} e^{jk_z^m z_q}, \tag{2.90}$$

$$a_n(k_z^m) = \frac{1}{\frac{\partial H_n^{(2)}}{\partial r}(a^m r_{obs.}) \Delta k_z} \left[b_n(k_z^m) \frac{nk_z^m}{kr_{obs.}} H_n^{(2)}(a^m r_{obs.}) \Delta k_z - \sum_{p=0}^{P-1} \sum_{q=0}^{Q-1} E_\phi(r_{obs.}, \phi_p, Z_p) e^{-jn\phi_p} e^{jk_z^m z_q} \right]. \tag{2.91}$$

The cylindrical wave coefficients ((2.90) and (2.91)) can be calculated using a two dimensional discrete Fourier transform [78] or the matrix method [80]. Once the cylindrical wave coefficients are obtained, the far field can be computed in spherical

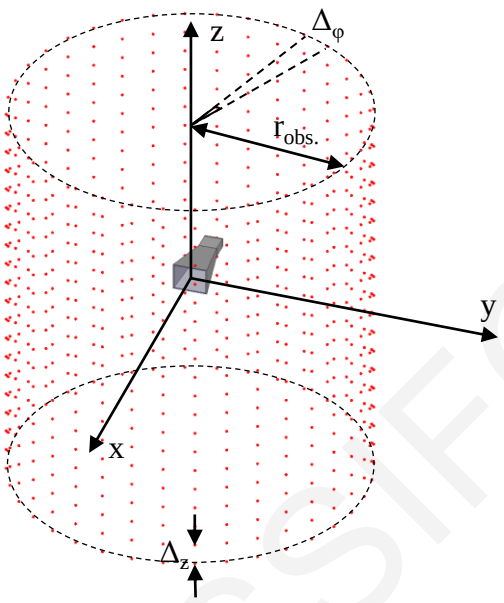


Figure 2.26: Cylindrical near field measurement of a horn antenna. Measurement points are shown with red marker points.

coordinates using:

$$E_\theta(r,\theta,\phi) = -j2k\sin\theta\frac{e^{-jkr}}{r}\sum_{n=-N/2}^{N/2-1} j^n b_n(k\cos\theta)e^{jn\phi}, \tag{2.92}$$

$$E_\phi(r,\theta,\phi) = -2k\sin\theta\frac{e^{-jkr}}{r}\sum_{n=-N/2}^{N/2-1} j^n a_n(k\cos\theta)e^{jn\phi}. \tag{2.93}$$

2.3.2.4 Spherical Near Field to Far Field Transformation

Spherical near field measurements of a radiating source, in this case a horn antenna, can be seen in Fig. 2.27. The measured electric field at a radius $r_{obs.}$ can be expressed as a truncated series of spherical vector wave functions [79,81]:

$$\hat{E}(r_{obs.},\theta,\phi) \approx k\sqrt{\eta}\sum_{s=1}^{2}\sum_{n=1}^{N}\sum_{m=-n}^{n} Q_{smn}F_{smn}^{(c)}(r_{obs.},\theta,\phi), \tag{2.94}$$

where $\eta = \sqrt{\mu_0/\varepsilon_0}$ is the free space impedance or the impedance of the medium. Q_{smn} is the spherical wave coefficient, and $F_{smn}^{(c)}$ are the normalized spherical wave functions.

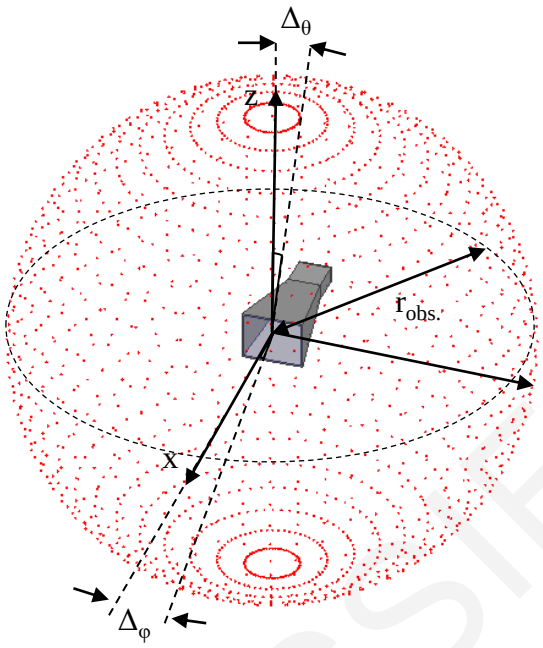


Figure 2.27: Spherical near field measurement of a horn antenna. Measurement points are shown with a red marker point.

The normalized spherical wave function is calculated using:

$$\begin{aligned} F^{(c)}_{smn}(r_{obs.},\theta,\phi) =& \delta_{s2}\frac{n(n+1)}{k_0 r_{obs.}} z^c_n(k_0 r_{obs.}) P^{|m|}_n(\cos(\theta)) e^{jm\phi}\hat{e}_r \\ &+ R^{(c)}_{sn}(r_{obs.})\Theta_{smn}(\theta) e^{jm\phi}\hat{e_\theta} \\ &+ (-1)^s R^{(c)}_{sn}(r_{obs.})\Theta_{s+1mn}(\theta) e^{jm\phi}\hat{e_\phi}, \end{aligned} \tag{2.95}$$

where $R^{(c)}_{sn}$ and $\Theta_{smn}(\theta)$ can be computed using:

$$R^{(c)}_{sn} = \delta_{s1} z^{(c)}_n(k_0 r_{obs.}) + \delta_{s2}\frac{1}{k_0 r_{obs.}}\frac{\partial}{\partial(k_0 r_{obs.})} k_0 r_{obs.} z^{(c)}_n(k_0 r_{obs.}), \tag{2.96}$$

$$\Theta_{smn}(\theta) = \delta_{s1}\frac{jm}{\sin\theta} P^{|m|}_n(\cos\theta) + \delta_{s2}\frac{\partial}{\partial\theta} P^{|m|}_n(\cos\theta), \tag{2.97}$$

and $\delta_{s\sigma}$ is the modified Kronecker delta which is used to accommodate for parity,

$$\delta_{s\sigma} = \frac{1}{2}(1 + (-1)^{s+\sigma}). \tag{2.98}$$

The radial function $z^{(c)}_n$ is specified by an upper index c to select which solution of the Bessel differential equation is used:

$$\begin{aligned} z^{(1)}_n &= j_n(kr) && (spherical\ Bessel\ function) \\ z^{(2)}_n &= n_n(kr) && (spherical\ Neumann\ function) \\ z^{(3)}_n &= H^{(1)}_n(kr) = j_n(kr) + jn_n(kr) && (spherical\ Hankel\ function\ of\ the\ first\ kind) \\ z^{(4)}_n &= H^{(2)}_n(kr) = j_n(kr) - jn_n(kr) && (spherical\ Hankel\ function\ of\ the\ second\ kind) \end{aligned} \tag{2.99}$$

Furthermore, $P_n^{|m|}$ is the associated Legendre polynomial of order m and degree n. The spherical wave coefficient can be calculated using:

$$Q_{smn} = \frac{1}{\bar{P}_{smn}(r_{obs.})} \sum_l \sum_t \left(E_\theta(r_{obs.}, \theta_l, \phi_t)\hat{\epsilon_\theta} + E_\phi(r_{obs.}, \theta_l, \phi_t)\hat{\epsilon_\phi} \right) F^*_{smn}(r_{obs.}, \theta_l, \phi_t) \sin\theta_l \Delta_\theta \Delta_\phi, \tag{2.100}$$

where $\bar{P}_{smn}(r_{obs.})$ can be calculated using:

$$\bar{P}_{smn}(r) = n(n+1)\frac{4\pi}{2n+1}\frac{(n+|m|)!}{(n-|m|)!}(R_{sn}(r))^2. \tag{2.101}$$

The spherical wave coefficients can be used to compute the orthogonal electric fields at any radial distance (r) greater than the minimum sphere (r_{min}) radius that can enclose the source by substituting them into (2.94). In order to avoid discretization errors, the sampling steps should be $\Delta_\theta = \Delta_\phi = {}^{2\pi}/_{kr_{min}}$.

2.4 Conclusion

Information in this chapter is used throughout this thesis. With the basic operation of each MSF unit cell the reader will be able to understand the operation of the unit cells in Chapters 3, 4 and 6.In Chapter 3, the loading element (LE) design is presented, where the understanding of the difference between integrated and lumped components is needed (Section 2.2). Similarly, the information of Section 2.2 is used in Section 4.4 and Chapter 5. The information about measurements (Section 2.3) is used throughout the thesis, in Chapter 3 and Chapter 4 for on-wafer measurements, in Chapter 5 and Chapter 6 for connectorized measurements. The information for antenna measurements (Section 2.3.2) is used in Chapter 6 and Chapter 7 for a bistatic measurement and for a planar NF-FF transformation, respectively.

Chapter 3

Toward an ASIC-Enabled Programmable Metasurface Absorber

In this chapter the steps towards the implementation of a programmable metasurface (PMSF), enabled by a custom application-specific integrated circuit (ASIC), are presented in detail. The ASIC is used to provide an adaptive and complex impedance load to each of the PMSF unit cells. Various semiconductor technologies are analysed for the implementation of tunable complex impedance loading elements (LEs) before one is selected for the final implementation, in which four complex loads are placed within each ASIC, and each load is controlled by two digital-to-analog converters (DACs). The LE is fabricated in the selected technology using a multi-project wafer (MPW) run before a more costly full wafer prototype attempt. The MPW produced forty dies which were used to experimentally validate the LE operation. Furthermore, the ASICs populate the back of the PMSF to form a mesh network to enable programmability. The chapter includes practical limitations that affect the realization, in addition an example adaptive PMSF absorber that builds upon the practical tuning range of the ASICs. Perfect absorption for both transverse electric (TE) and transverse magnetic (TM) polarization is demonstrated.

3.1 Introduction

Metamaterials (MTMs) are composite materials that exhibit properties that are not found in nature. A negative refractive index is one of the many exotic properties that MTMs possess. It was initially speculated in [1] and experimentally

demonstrated in [2] that a negative refractive index can be realized when the electric permittivity and magnetic permeability are both negative. MTMs have also demonstrated the ability to resolve beyond the diffraction limit in free space [4] by designing the refractive index to be equal to -1, and cloaking by manipulating the electromagnetic waves around an object [3]. These are just some of highlights of the MTM properties. MTMs have since also been used to improve the performance of countless components in RF/microwave and antenna design [6,7,9,82].

Metasurfaces (MSFs), the two-dimensional versions of MTMs have gained interest by researchers in the past decade. Like their three-dimensional counterparts, they have demonstrated many exotic properties, such as anomalous reflection [12,13,83,84], perfect absorption [85] and non-linear reflection [35]. By loading the MSFs with lumped elements, the MSF response can be altered [86]. These lumped elements can be replaced with tunable varactors or varistors and create electronically tunable MSF reflectors [21,87] and absorbers [88]. Other means of obtaining tunable MSFs have been shown, like magnetic tunability [28], optical tunability [29] and even by exploiting the optomechanical properties of poly disperse red 1 acrylate to optically tune MSFs with a memory effect [30,31].

MSFs have demonstrated the ability to synthesize wavefronts through the individual design of their constituent unit cells. In [89], multi-beam reflection and simultaneous polarization conversion was demonstrated. Isoflux patterns with circular polarization were demonstrated in [90] and local multipoint distribution service patterns were demonstrated in [91].

Dynamic wavefront manipulation was also demonstrated by PMSFs. Dynamic scattering, focusing and polarization rotation was implemented in [32]. Dynamic control of the modulation of the reflection phase resulted in accurate control of the harmonic level of a non-linear reflecting PMSF [35]. PMSFs were utilized to implement reflective [34] and transmissive [33] holograms in the microwave regime.

The conceptual design of this work was presented in [92], where individual electronically tunable complex impedance MSF LEs, consisting of resistive and capacitive (*RC*) elements, were embedded in each unit cell to obtain a reconfigurable multifunctional MSF. It was shown that by using this approach, continuous control over the real and imaginary parts of the complex surface impedance can be obtained, thus enabling the shaping of the spatial profile of both the reflection amplitude and phase, leading to maximum versatility in the achievable functions. In this chapter,

the design methodology is presented, including the steps taken to implement the PMSF concept by taking into account manufacturing and cost limitations. The PMSF consists of a top textured layer, exposed to the electromagnetic (EM) waves, an intermediate ground plane layer, and two routing layers on the bottom, to provide control and power to the application-specific integrated circuits (ASICs) that are used to program the MSF. The ASICs are populated on the bottom side in an array structure. In order to reduce the cost and to conform to tight space constraints, a single ASIC design must operate without the need for any further components. As will be subsequently elaborated upon, the ASIC contains both low-power, MSF LEs, as well as asynchronous circuits implementing a grid communication algorithm, as presented in [93]. This chapter includes realistic LE tunability ranges, extracted from three candidate semiconductor technology PDKs. Furthermore, the chapter outlines various MSF PCB manufacturability issues. Finally, the chapter shows that the ASIC can be used to create a PMSF, also known as a hypersurface [94], which demonstrates programmed perfect absorption, for a range of incident angles for both TE and TM polarizations.

3.2 Programmable Metasurface Unit Cell

Fig. 3.1 shows an array of unit cells that form an example PMSF. The top view in Fig. 3.1 is showing the textured square patch, while the bottom view, shows the PMSF loading ASIC that is placed in every unit cell.

The general topology resembles greatly the MSF presented in Section 2.1.5, but has a significantly different response, since the ASIC is positioned at the bottom of the unit cell below a ground plane, and it is connected to every four rectangular patches. This general topology was chosen after carefully considering other alternative options, e.g. the ASIC could lie on the top layer (which would make the topology resemble more the one in Section 2.1.5) or even be embedded within the PCB. The first option was discarded, since having metallic tracks that carry power and communication signals on the top layer will adversely affect the EM behaviour of the PMSF. Secondly, if the ASIC were to be embedded in the PMSF PCB, it would not only need a specialized, high-cost PCB process, but would also render the hypersurface irreparable in case of ASIC faults. Given the large number of ASICs needed to create a hypersurface, the probability of one ASIC failing or having a dry solder

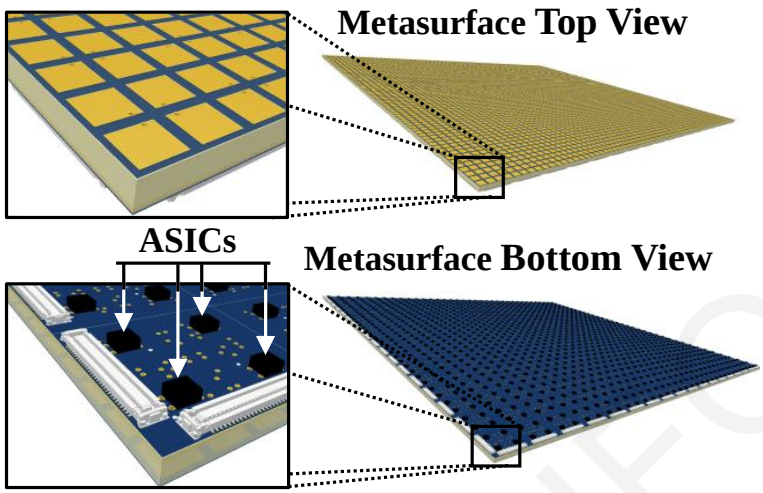


Figure 3.1: Illustration of a PMSF covering a 5×5 λ^2 area. The top and bottom views of the PMSF are shown. The loading ASICs are located on the bottom side of the PMSF.

joint is increased. Thus, serviceability is of paramount importance in the selection of the topology.

3.2.1 Unit Cell Geometry

An example unit cell topology can be seen in Fig. 3.2. It consists of a textured MSF pattern on the top layer (L_1), a ground plane in the middle layer (L_2), communication and power distribution layers (L_3 and L_4), with the ASIC bonded to the bottom layer (L_4). The ASIC on the bottom layer, containing the MSF LEs, has four direct vias that route the RF signals between the bottom layer (L_4) and the top layer (L_1). The example unit cell topology in Fig. 3.2, which has a subwavelength size of $\lambda/7$, is periodically repeated to form the complete MSF (Fig. 3.1) that occupies a total area of 5×5 λ^2, at the design frequency (5 GHz).

The design cycle of a PMSF such as the one shown in Fig. 3.1 requires a careful design balancing act, taking into account multiple practical constraints. The PMSF presented is designed to perform as an absorber at normal and oblique incident angles. As it will be shown in this section, this entails that the loading ASIC will need to cover a specified RC range to achieve this operation. In the current example, the range required for the resistance is relatively low, and hence works at the limits of the practical range found in ASIC implementations, as it will be shown in Section 3.3.1. This constraint can be relaxed by implementing the hypersurface on a thicker substrate (H_1) and by employing a substrate with lower dielectric losses,

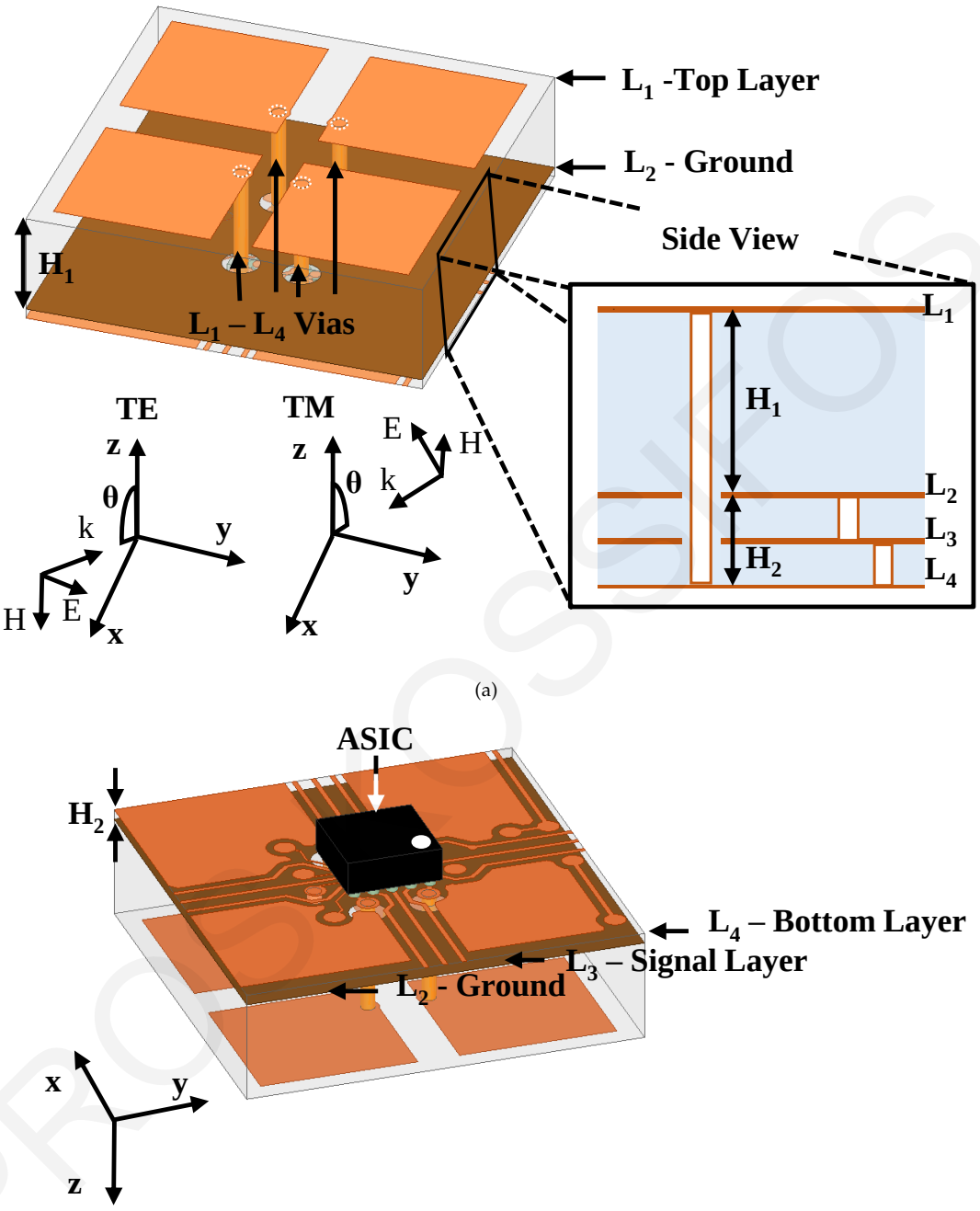


Figure 3.2: MSF unit cell geometry. (a) Top side of the unit cell and (b) bottom side of the unit cell showing the location of the MSF loading application specific integrated circuit (ASIC).

resulting in higher resistance value requirements.

The example unit cell design is elaborated in Fig. 3.3. The details of the geometric parameters are listed in Table 3.1. An optimized parameter that is sensitive to the performance of the PMSF absorber is the position of the $L_1 - L_4$ vias connecting the patches in L_1 to the ASIC terminals in L_4. As described in [95], the optimal position for an isotropic cell would be at the corner of the patches, where the surface

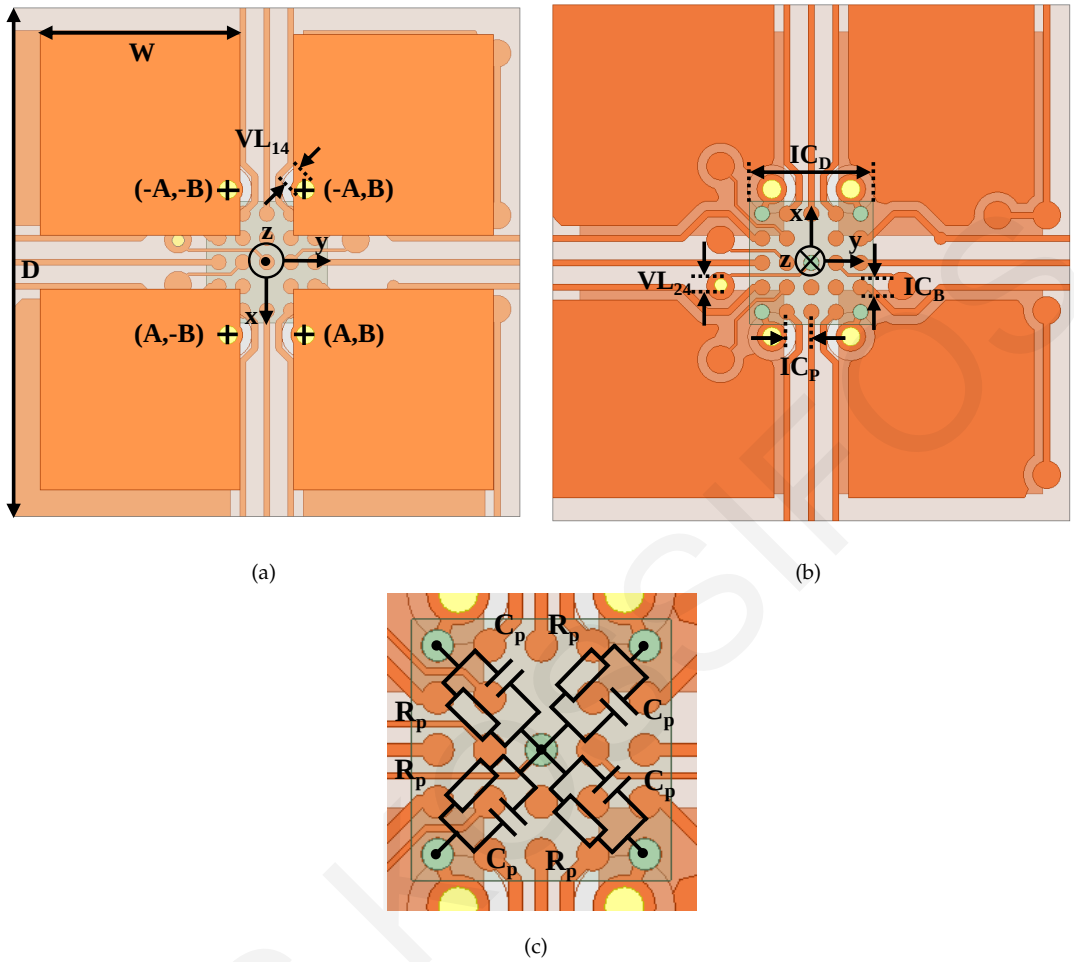


Figure 3.3: MSF unit cell geometry. (a) Top side of the unit cell, (b) bottom side of the unit cell, and (c) close-up of the bottom side, showing the location of the MSF loading ASIC, implementing four parallel-connection *RC* loads.

current density is larger. Unfortunately, due to various fabrication limitations this option was not available, so the vias were placed near the inner edge of patches along one direction, as shown in Fig. 3.3, so that at least one polarization would be optimally covered. The methodology for the optimization of the absorber unit-cell parameters, namely the width of the patches and the period of the cell, is described in [95], under the constraints of: operating frequency, manufacturing (through via position), dielectric thicknesses, ASIC size and available *RC* range.

In Fig. 3.3(a) and Fig. 3.3(b) a top and bottom view of the unit cell are shown. Fig. 3.3(c) depicts the connectivity of the ASIC to the MSF from the edge pins. The ASIC in this design loads the MSF with four parallel-connected *RC* loads, as shown in Fig. 3.3(c). The design of the MSF loads, along with their control circuit will be discussed in Section 3.3.1. The ASIC uses a wafer-level-chip-scale package (WLCSP). The solder balls are also included in the simulations, and are each modelled as a

Table 3.1: Rectangular patch unit cell's geometry parameters.

Geometric Parameter	Dimension (mm)	Description
H_1	2.137	Top Substrate Thickness
H_2	0.255	Bottom Substrate Thickness
D	8.4	Period of the Unit Cell
W	3.32	Width of the Patch
A	1.2	x-Coordinate of $L_1 - L_4$ Via
B	0.641	y-Coordinate of $L_1 - L_4$ Via
VL_{14}	0.30	Diameter of $L_1 - L_4$ Via
VL_{24}	0.15	Diameter of $L_2 - L_4$ Via
IC_D	2.00	ASIC Dimensions
IC_P	0.40	ASIC Pitch
IC_B	0.25	ASIC Pad Diameter

cylinder of height 0.15 mm and diameter 0.25 mm. The solder ball used was alloy SAC405 in order to accurately take into account its effect on the design. The realizable unit cell was designed by taking into account practical limitations of the ASIC and the PCB technology. These limitations include *R* and *C* ranges, cost of the semiconductor process, maximum PCB thickness, via and track sizes, and substrate losses.

As can be seen in Table 3.1, H_1 is much larger than H_2, in order to relax the ASIC's constraint on the realization of the resistance values, and H_2 should be small, so that the power and ground supplied to the ASIC is of good quality. The asymmetric layer stack of the PCB improves the RF performance of the MSF, however care must be taken with an increased number of layers as they introduce additional variations in the PCB thickness. The PMSF unit cell was co-simulated using an electromagnetic model that was combined with the lumped *RC* loads. The absorption performance, shown in Fig. 3.4, was obtained through the use of circuit and electromagnetic co-simulations in ANSYS HFSS.

In Fig. 3.4(a) and Fig. 3.4(b) the reflection coefficient for normal incidence (θ = 0°) is plotted for TE and TM polarization respectively. In these plots, perfect

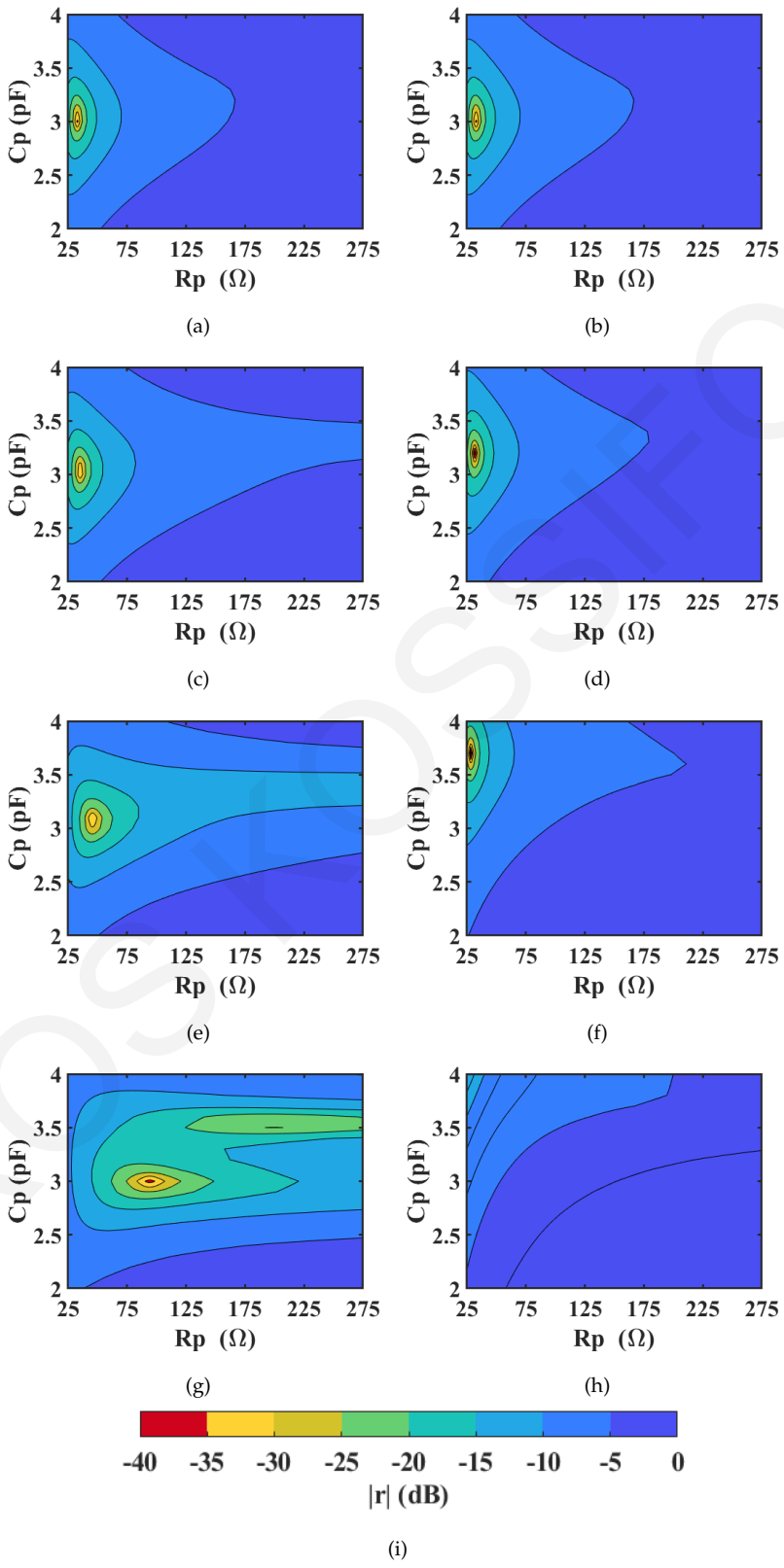


Figure 3.4: Reflection coefficient magnitude $|r|$ in dB at 5 GHz for (a) TE $\theta = 0°$ normal incidence, (b) TM $\theta = 0°$ normal incidence, (c) TE $\theta = 15°$, (d) TM $\theta = 15°$, (e) TE $\theta = 30°$, (f) TM $\theta = 30°$, (g) TE $\theta = 45°$, (h) TM $\theta = 45°$ and (i) the color scale .

absorption (|r|<-30 dB) is indicated with a yellow colour in the plot. Note that the results are almost indistinguishable for TM polarization, but not identical due to the

asymmetric placement (in the x- and y-axes) of the through vias (L_1-L_4) with respect to the MSF patches on the top layer (Fig. 3.3(a)). This asymmetric placement was implemented to obtain good performance for large oblique incidence angles for at least one polarization, the TE [95]. This can be seen in Fig. 3.4(c), Fig. 3.4(e) and Fig. 3.4(g), where the reflection coefficient for TE polarization is shown for $\theta = 15°$, 30°, and 45°, respectively. It can be seen that the required resistance and capacitance for perfect absorption increase for larger oblique angles of incidence, but a very low reflection amplitude can be obtained inside the considered RC range. Note that two absorption peaks appear for larger angles and can be both exploited [95]. In Fig. 3.4(d), Fig. 3.4(f) and Fig. 3.4(h) the reflection coefficient for TM polarization is shown for $\theta = 15°, 30°$, and 45°, respectively. It can be seen that the required RC combination shifts towards higher capacitances for larger oblique angles of incidence. For this polarization, the reflection dip moves outside the considered RC range for angles exceeding 45°, which could prove to be a limitation in the realization of the LE RC range.

3.3 Metasurface ASIC

Numerous semiconductor technologies are commercially available for the implementation of the MSF loading ASICs. The selection of a semiconductor technology offers new challenges in the design of a suitable integrated circuit for MSF applications. Programmable MSF designs shown in the literature thus far, use commercially-available off-the-shelf (COTS) components as LEs, and programmable modules such as field programmable gate arrays (FPGAs), to individually address each unit cell [32, 35]. This type of architecture separates the high-frequency RF electronic component of the design (the unit cell LE) from the low-frequency analog and digital component (the FPGA). Typically, the RF LEs operate at a higher frequency and are manufactured from high-performance and costly technologies, like silicon-germanium (SiGe) and even gallium-arsenide (GaAs), while the analog and digital control circuits are manufactured on cheaper silicon technologies.

This chapter aims towards the realization of a PMSF architecture that addresses individually each unit cell, and is capable of providing a complex loading impedance. This functionality necessitates that the high-frequency LEs are integrated together with the analog and digital control circuits on the same chip. Ideally, in order to

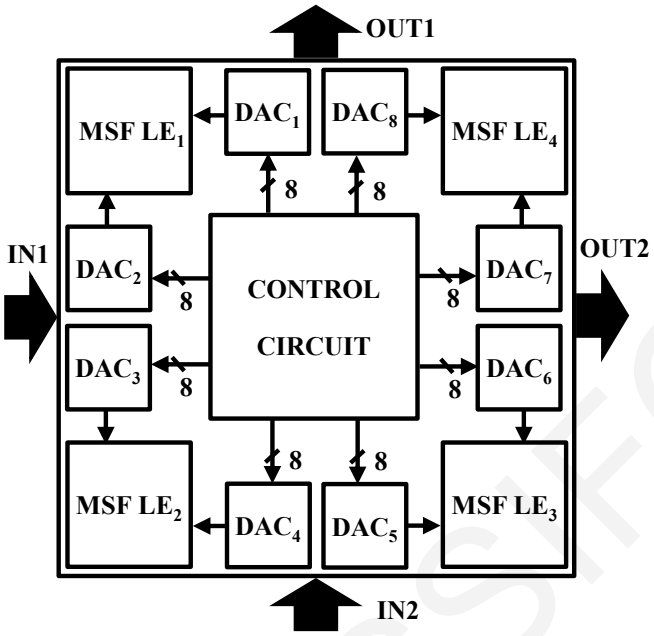


Figure 3.5: Top-level diagram of the PMSF loading ASIC showing the input/output (IN1, IN2, OUT1, OUT2), the four MSF LEs, eight DACs, and the communication control circuit. The ASIC uses serial and unidirectional input/output communication.

realize high-quality RF LEs, the whole integrated circuit would be designed in a high-frequency SiGe or GaAs process, however the large number of ICs necessary to implement a large hypersurface would render the cost prohibitively high. Therefore, a technology should be selected that can provide a sufficient range for the tunable complex impedance LEs at the design frequency of 5 GHz, while also being economically feasible.

With the envisaged large number of ASICs needed for the hypersurface implementation, the power consumption of each IC needs to be carefully considered. In [32], each individual MSF LE required 10 mA of current in its ON state. This might appear small, but the MSF consists of 40×40 unit cells, which translates to a total current consumption of 16 A when all 1600 LEs are ON. In order to reduce the overall current consumption, each MSF LE should be implemented with a negligible current draw, and since each unit cell is locally controlled, the digital and analog part should also be designed with minimum power requirements. In [96], the importance of using asynchronous control circuits for enabling programmable and scalable MSFs is argued. Asynchronous circuits offer a low power consumption for controllers that are idling most of the time, as in the case of controllable MSFs. Additionally, and more importantly for RF applications, EM emissions from this ASIC are inherently

reduced, due to the data-driven clocking, as well the fact that a location setting can be changed without clocking the entire surface. Finally, by using asynchronous clocking there is no need for a power hungry clock distribution network on the entire MSF.

The packaging of the MSF loading ASIC also needs to be taken into account. The package will introduce additional parasitic effects that will reduce the overall range of the obtainable complex impedances, and can also increase the cost of the ASIC. For the chosen MSF application, WLCSP was chosen since it offers the cheapest packaging solution and introduces the least amount of parasitic effects [97,98].

The top-level architecture of the PMSF loading ASIC is shown in Fig. 3.5. It consists of four MSF LEs that each consist of a voltage-controlled capacitor (varactor) in parallel with a voltage-controlled resistor (varistor). These LEs are connected between the outer pins of the chip and the center ground pin. The biasing for the MSF LEs is provided by eight on-chip DACs, that are set by data passed through four serial, asynchronous, unidirectional communication ports of the ASIC. These communication ports form a larger grid, within the MSF, arranged in a Manhattan style network, as described in Section 3.3.5.

3.3.1 Metasurface Loading Element Design

The MSF LE will need to provide a complex impedance to adjust the surface impedance of the MSF to be equal to the incident wave's impedance (η) in order to achieve perfect absorption. The complex impedance values are dependent on the direction or angle of incidence (θ), the polarization of the propagating wave (TE or TM) and the frequency.

The ASIC is connected to the MSF at the four corner pins and with the center ground via pin, as shown in the close up shown in Fig. 3.3(c) forming a double T' five-terminal network shown in Fig. 3.6. Five complex impedances (Z_A, Z_B, Z_C, Z_D and Z_E) compose the theoretical circuit.

The network in Fig. 3.6 can be described with the Z-parameter matrix:

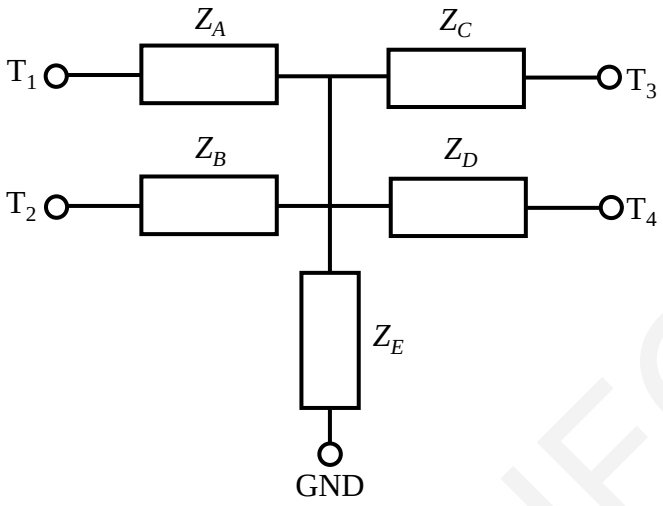


Figure 3.6: ASIC's equivalent double T' network.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}. \tag{3.1}$$

This Z-parameter matrix can be expressed in terns of the five complex impedances (Z_A, Z_B, Z_C, Z_D and Z_E) by using the well known equation from [58] (page 175, eq. (4.28)):

$$Z_{ij} = \frac{V_i}{I_j}, I_k = 0 \; for \; k \neq j. \tag{3.2}$$

This would re-write the Z-parameters as:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} Z_A + Z_E & Z_E & Z_E & Z_E \\ Z_E & Z_B + Z_E & Z_E & Z_E \\ Z_E & Z_E & Z_C + Z_E & Z_E \\ Z_E & Z_E & Z_E & Z_D + Z_E \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}. \tag{3.3}$$

Therefore, one can say that:

$$Z_A = Z_{11} - Z_{ij}, \; for \; i \neq j. \tag{3.4}$$

The complex impedances Z_A, Z_B, Z_C and Z_D are the tunable load impedances. If these impedances are tuned to be $Z_A = Z_B = Z_C = Z_D$, the Z matrix takes the following

form:

$$Z_{ASIC} = \begin{bmatrix} Z_A + Z_E & Z_E & Z_E & Z_E \\ Z_E & Z_A + Z_E & Z_E & Z_E \\ Z_E & Z_E & Z_A + Z_E & Z_E \\ Z_E & Z_E & Z_E & Z_A + Z_E \end{bmatrix}. \tag{3.5}$$

To convert the above Z matrix to S parameters, the following equation can be used:

$$S = G_{ref}(Z - Z_{ref})(Z + Z_{ref})^{-1}G_{ref}^{-1}. \tag{3.6}$$

Where G_{ref} is equal to :

$$G_{ref} = \begin{bmatrix} G & 0 & 0 & 0 \\ 0 & G & 0 & 0 \\ 0 & 0 & G & 0 \\ 0 & 0 & 0 & G \end{bmatrix}, \tag{3.7}$$

and $G = \sqrt{\Re(Z_0)}^{-1}$ and Z_0 is the port impedance. This will result in the following S-parameter matrix:

$$S_{ASIC} = \begin{bmatrix} S_A & S_B & S_B & S_B \\ S_B & S_A & S_B & S_B \\ S_B & S_B & S_A & S_B \\ S_B & S_B & S_B & S_A \end{bmatrix}. \tag{3.8}$$

S_A and S_B are calculated using:

$$\begin{aligned} S_A = S_{ii} &= \frac{Z_A^2 + 4Z_AZ_E - Z_0(2Z_E + Z_0)}{(Z_A + Z_0) + (Z_A + 4Z_E + Z_0)}, \\ S_B = S_{ij} &= \frac{2Z_E + Z_0}{(Z_A + Z_0) + (Z_A + 4Z_E + Z_0)}, for\ i \neq j. \end{aligned} \tag{3.9}$$

If the center ground pin of the ASIC is connected directly to ground, then $Z_E \simeq 0$ and (3.9) can be simplified to:

$$\begin{aligned} S_A = S_{ii} &= \frac{Z_A - Z_0}{Z_A + Z_0}, \\ S_B = S_{ij} &= 0, for\ i \neq j. \end{aligned} \tag{3.10}$$

In simulation, one can place a terminal directly on the center pin so the analysis of the four-port network can be simplified to a single port, since $Z_E \simeq 0$ and the four ports are isolated. This might not be the case in the physical implementation, since vias in pad might not be available in the PCB technology, and traces will be needed to rout the center pin from L_4 to L_2.

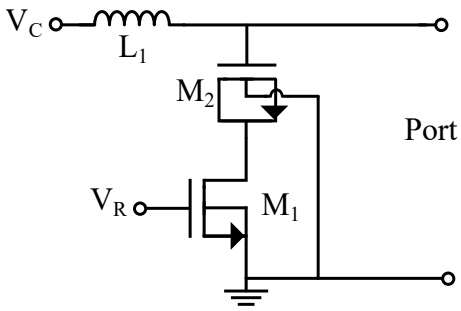


Figure 3.7: Simplified LE circuit series configuration.

3.3.1.1 Circuit Topology Selection

The LE can be realised in various circuit topologies and their realization will need to be implemented though the use of the devices available in an affordable, commercially available foundry process. Models for their simulation in this case are supplied with the PDKs and the complete process of modelling the device can be omitted.

The variable resistance (varistor) is most easily integrated in an IC technology by using a simple MOSFET device, and the variable reactance or variable capacitor (varactor) can be realized using a MOSFET varactor, as described in the background information for IC components in Chapter 2.

A simplified schematic for a series configuration can be seen in Fig. 3.7. M_2 is the varactor and M_1 is the varistor. L_1 is an RF choke inductor used to bias the varactor without affecting the total impedance. V_C is the analog biasing voltage used to bias the varactor, and V_R is the analog bias voltage used to bias M_1. M_1 in this configuration will need to have a resistance value equal to the optimum values shown in Fig. 3.4. In theory, this can be achieved by increasing the size of the MOSFET. Increasing the size will also increase the substrate capacitance, effectively shorting the MOSFET to the substrate.

A simplified schematic of the parallel circuit topology LE circuit can be seen in Fig. 3.8. The varactor (M_2) is placed in parallel with the varistor (M_1), and an on-chip metal-insulator-metal (MiM) DC blocking capacitor (C_1) is placed in series with M_1 to prevent V_C shorting out through M_1. The varactor's (M_2) capacitance, is tuned by a biasing voltage V_C, through an on-chip inductor, L_1. L_1 is used as an RF choke to prevent the low impedance biasing node V_C from effectively shorting the load. Given that a MSF requires a large number of unit cells, it is essential that each LE has a low static power consumption. The varistor is tuned by a biasing voltage V_R. Both

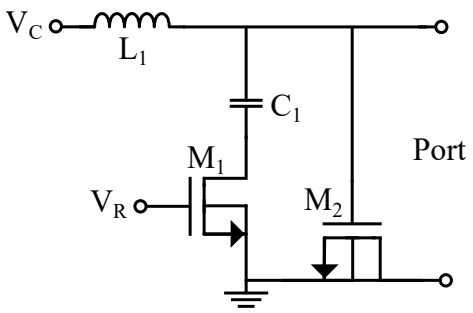


Figure 3.8: Simplified LE circuit parallel configuration.

V_C and V_R draw negligible current, in the order of pico Amperes, into the MOSFET gates.

This parallel model can achieve lower resistance values compared to the series configuration. Its limitation and design process will be discussed next.

3.3.1.2 Parallel Circuit Topology

The impedance of the varactor (M_2) in Fig. 3.8, will ideally only have a reactive component, but in reality, it also possesses a resistive component, and the same applies for the inductor. Similarly, the varistor possesses a parasitic reactive component in addition to the desired resistance. The on-chip DC block capacitor does not have ideal behaviour, primarily due to the capacitance of the bottom plate to the substrate ground. For this reason, each element in the schematic will affect the total impedance that is seen by the one-port network. One can think of each element as a complex impedance, which is predominantly resistive, capacitive or inductive. The LE can then be simplified to an equivalent parallel *RC* circuit that loads the MSF unit cells, shown in Fig. 3.3(c).

3.3.2 Design of the On-Chip Loading Element Components

3.3.2.1 Varistor Implementation

The combined components M_1 and C_1 are easily tuned in this design without needing a very large size. The DC block capacitance should be set to at least double the capacitance of the metal-oxide semiconductor (MOS)-varactor in order not to affect the total capacitance.

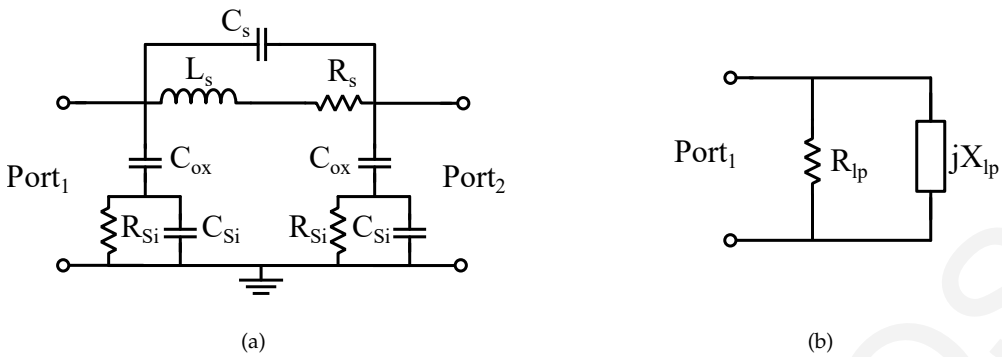


Figure 3.9: (a) Inductor lumped-element model [59,60], and (b) equivalent parallel circuit.

3.3.2.2 Inductor Implementation

A planar on-silicon inductor model is derived and experimentally validated in [59,60]. For L_1 in the LE circuit, the aforementioned inductor model is used and can be seen in Fig. 3.9. In the circuit, the inductor is connected to V_C on one side (Port_2) and Port $_1$ on the other side. V_C can be considered a very low impedance node, therefore the model in Fig. 3.9(a) can be considered a one-port network by shorting Port_2. The complex model can then be converted into a simplified parallel circuit shown in Fig. 3.9(b). This is done by solving for the total admittance (Y_{Ltot}) and then converting this to a parallel resistance ($R_{lp} = 1/\Re(Y_{Ltot})$) and a parallel reactance ($X_{lp} = 1/\Im(Y_{Ltot})$). The parallel resistance and reactance are equal to:

$$R_{lp} = \frac{\left(\left(\frac{R_s}{\omega}\right)^2 + L_s^2\right) K_1}{C_{ox}^2 \left(R_{Si}\left(R_s^2 + L_s^2\omega^2\right)\right) + R_s K_1}, \tag{3.11}$$

$$X_{lp} = -\frac{\omega(L_s^2\omega^2 K_4 + R_s^2 K_3 - L_s K_2)}{\left(L_s^2\omega^2 + R_s^2\right) K_2}. \tag{3.12}$$

Here K_1, K_2, K_3 and K_4 are given by:

$$\begin{aligned}
K_1 =& \frac{1}{\omega^2} + (C_{ox} + C_{Si})^2 R_{Si}^2, \\
K_2 =& R_{Si}^2\omega^2(C_{ox} + C_{Si})^2 + 1, \\
K_3 =& (C_{ox}^2 R_{Si}^2\omega^2 (C_s + C_{Si}) \\
&+ C_{ox}\left(R_{Si}^2\omega^2\left(2C_sC_{Si} + C_{Si}^2\right) + 1\right) \\
&+ C_s\left(C_{Si}^2 R_{Si}^2\omega^2 + 1\right), \\
K_4 =& R_{Si}^2\omega^2\left(C_{ox}^2 (C_s + C_{Si}) + C_sCsi^2\right) \\
&+ C_{ox}(R_{Si}^2\omega^2(2C_sC_{Si} + C_{Si}^2) + 1) + C_s.
\end{aligned} \tag{3.13}$$

The self-inductance of the inductor can be calculated using: [59]

$$L_{self} = 2l\left(\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{w+t}{3l}\right). \tag{3.14}$$

Where L_{self} is the inductance in nH, l is the wire length, w is the width and t the thickness all the geometric units are in cm. The mutual inductance between two wires can be calculated using:

$$M = 2lQ_m. \tag{3.15}$$

Where M is the in inductance in nH. Q_m is the mutual inductance parameter and can be calculated with:

$$Q_m = \ln\left(\frac{l}{GMD} + \sqrt{1+\left(\frac{l}{GMD}\right)}\right) - \sqrt{1+\left(\frac{l}{GMD}\right)} + \frac{GMD}{l}. \tag{3.16}$$

The term GMD is related to the geometry mean distance of the wires. It can be approximated with the pitch of the wires, and a more accurate expression can be found in [59] (eq. (4)).The series resistance can be expressed as:

$$R_s = \frac{\rho l}{w t_{eff}} \tag{3.17}$$

Where the ρ is the resistivity of the wire, l and w are the length and the width of the wire respectively. The term t_{eff} is the effective thickness of the wire and is relates to the skin depth δ:

$$t_{eff} = \delta\left(1 - e^{-\frac{t}{d}}\right), \tag{3.18}$$

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}}. \tag{3.19}$$

Where μ is the permeability and f is the frequency. The shunt capacitance C_s can be calculated using:

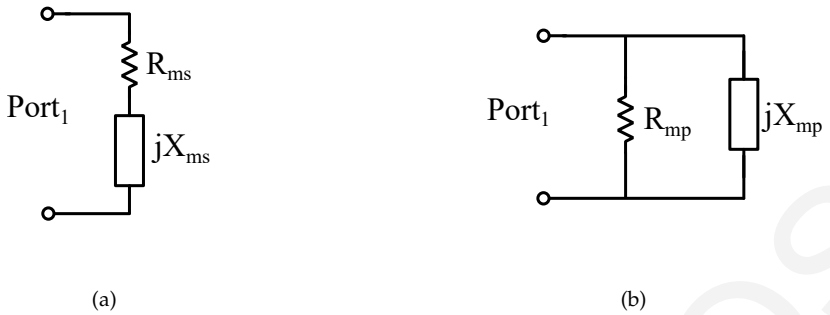
$$C_s = nw^2\frac{\varepsilon_0\varepsilon_r}{t_{oxM_{n-1}-M_n}}. \tag{3.20}$$

The permeability in vacuum is denoted with ε_0 and ε_r is the oxide relative permeability. The number of the inductor turns is n and $t_{oxM_{n-1}-M_n}$ is the oxide thickness between the spiral and the underpass.

The parasitic substrate capacitances C_{Si} and resistance R_{Si} can be calculated using:

$$C_{Si} = \frac{1}{2}lwC_{sub}, \tag{3.21}$$

$$R_{Si} = \frac{2}{lwG_{sub}}, \tag{3.22}$$



(a) (b)

Figure 3.10: Simplified circuit for the MOSFET-varactor lumped-element model which was presented in Section 2.2, Fig. 2.11(b) ([60, 62]). (a) Simplified series circuit, and (b) simplified parallel circuit.

where the C_{sub} and G_{sub} are capacitance and conductance per unit area for the silicon substrate. The oxide capacitance G_{ox} can be calculated using:

$$C_{ox} = \frac{1}{2} lw \frac{\varepsilon_{ox}}{t_{ox}}. \tag{3.23}$$

The dielectric constant and the thickness of the oxide are denoted as ε_{ox} and t_{ox}.

From (3.11) one can observe that, in order to increase the parallel equivalent resistance of the inductor, R_{lp}, the parasitic oxide capacitance (C_{ox}) and the series resistance (R_s), need to be minimized which will in turn effectively minimize the denominator. The dominant factor is C_{ox}, which is raised to the second power in (3.11), therefore the oxide capacitance should be reduced. This is commonly achieved by placing the inductor on the top metal layer and by reducing the width of the inductor lines. Reducing the width of the lines will also increase the series resistance R_s, which is undesirable, so a thick metal is preferable since it reduces R_s without affecting C_{ox}. The length of the inductor lines can be reduced in order to reduce the series resistance R_s until a point where the inductance is sufficient to block most of the RF signal to V_C, and the inductance will not affect the loading capacitance.

An on-chip inductor was designed so as to maximize the parallel resistance, whilst obtaining the correct value of inductance. On the chip, apart from the width of the metal, one can also choose on which metal layers to implement the inductor as well as what is in the vicinity of the inductor.

3.3.2.3 Varactor Implementation

A MOSFET varactor model is presented in [60, 62] for multiple finger devices. This model can be found in Section 2.2, Fig. 2.11(b). For a particular frequency range,

the complex MOSFET varactor can be simplified to a single-port device with a series resistance $R_{ms} = \Re(Z_{mtot})$ and a series reactance $X_{ms} = \Im(Z_{mtot})$ (see Fig. 3.10(a)), where Z_{mtot} is the total complex impedance of the device. This simplified series circuit, can then be transformed into a parallel circuit (see Fig. 3.10(b)), for which the parallel resistance (R_{mp}) is equal to:

$$R_{mp} = \frac{R_{ms}^2 + X_{ms}^2}{R_{ms}} = R_{ms} + X_{ms}Q, \tag{3.24}$$

and the parallel reactance (X_{mp}) is equal to:

$$X_{mp} = \frac{R_{ms}^2 + X_{ms}^2}{X_{ms}} = \frac{R_{ms}}{Q} + X_{ms}, \tag{3.25}$$

where, Q is the quality factor and is given by:

$$Q = \frac{X_{ms}}{R_{ms}}. \tag{3.26}$$

3.3.3 Technology Selection

In this section, an investigation is presented for three commercially-available candidate technologies. This is done using simulated results from CADENCE VIRTUOSO®, revealing the achievable complex impedance ranges for the MSF LEs. These are complementary metal-oxide semiconductor (CMOS) processes at the 350 nm, 180 nm and 65 nm technology nodes. Specialized SiGe and GaAs technologies are not investigated in this thesis, since they are costly and not widely available.

The supplied voltages V_R and V_C in Fig. 3.8, are progressively increased from zero to the maximum allowed operating voltage of the technology or to a large enough voltage that does not provide any further impedance tuning. For each set of V_R and V_C voltages, this corresponds to a specific *RC* combination. Thus, by varying both V_R and V_C, an area of *RC* combinations can be created within an *RC* map, which defines the achievable *RC* values for that technology.

The *RC* area of each LE needs to cover the optimum *RC* combinations required by the MSF unit cell to achieve perfect absorption, (see Fig. 3.22). This has proven difficult to achieve in simulations with the series configuration (in all three of the evaluated technologies), since the varistor (M_1) needs to have a large number of fingers to achieve the required low resistance. The large number of fingers also

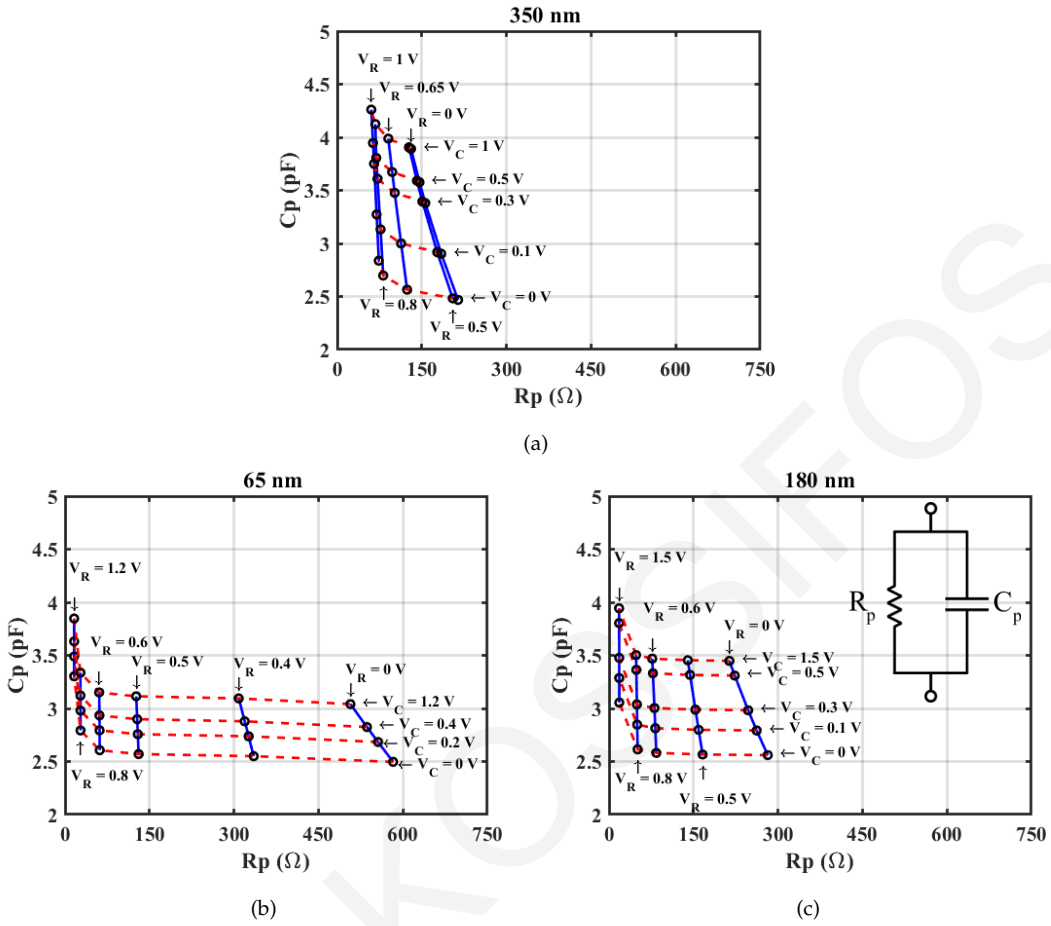


Figure 3.11: Equivalent parallel resistance and capacitance range at 5 GHz, for (a) 350 nm, (b) 65 nm and (c) 180 nm semiconductor technologies.

means that its parasitic capacitance to the substrate is also moderately large, thus effectively short-circuiting it at the design frequency.

The parallel configuration showed more promise in achieving the required low resistance. In order to evaluate the performance of each technology, each device (M_1, M_2, L_1, C_1) was adjusted to increase the parallel RC range and satisfy the optimum RC combinations.

The adjusted parallel configuration RC ranges can be seen in Fig. 3.11(a), Fig. 3.11(b) and Fig. 3.11(c) for the 350 nm, 65 nm and 180 nm technologies, respectively. The results of Fig. 3.11 were obtained using data from S-parameter simulations and converting the reflection coefficient at the Port on the right-hand side of the parallel LE circuit of Fig. 3.8 to a parallel configuration RC map. Constant V_R lines are shown in solid blue lines in the Fig. 3.11, and constant V_C lines are shown in dashed red lines.

It can be seen in Fig. 3.11 that for larger feature technologies the capacitance

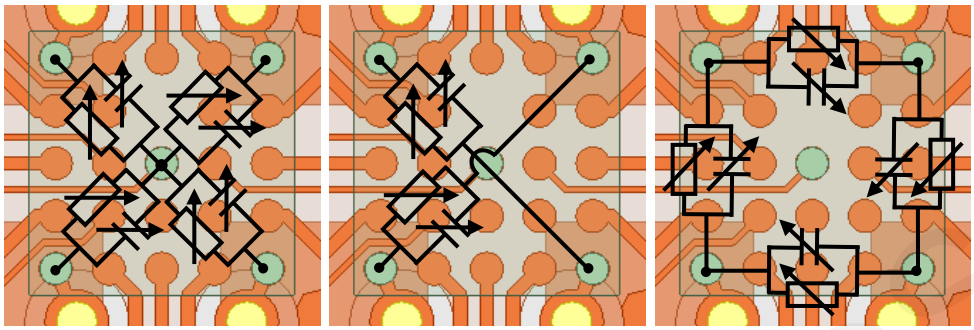
range increases, while the resistance range decreases. The reduction of the resistance range in the larger feature technologies is caused by a reduction of the quality factor of M_2 due to the larger gate length [62]. The gate width also increases the capacitance range proportionally [62]. It is obvious that there is a compromise to be made when choosing the technology. The 180 nm technology offers a compromise between the achievable capacitance and resistance ranges, and was therefore chosen as a viable technology.

3.3.4 Loading Element Connectivity

As described in Section 3.2.1, there are four MSF LEs in each ASIC, connected as shown in Fig. 3.12(a). The ASIC uses 19 pins for the controller and the remaining 5 for the LEs. An alternative solution considered, had two MSF LEs as shown in Fig. 3.12(b), however the one shown in Fig. 3.12(a) was chosen, in order to increase the equivalent parallel resistance of the circuit. The parallel resistance of Fig. 3.12(a) is essentially double that of Fig. 3.12(b). Additionally, two of the pins of Fig. 3.12(b) would have to be converted to a DC ground, using two additional inductors (RF chokes). Note that on-chip inductors occupy an area comparable to the WLCSP pads, which would have made the LEs occupy a larger on-chip area. This increased LE area would increase the ASIC's size as well as its cost. Furthermore, the layout implementation of Fig. 3.12(b) would suffer from additional parasitics, arising from metal lines running across the entire IC. In order to maintain the rotational symmetry required, and to allow the chip to be rotated for communication purposes (see Fig. 3.13), the center pin was selected as the RF ground. A further alternative considered is shown in Fig. 3.12(c). Although this option needs one fewer pins, it was also abandoned because it would be impossible to independently control the varactors/varistors without additional space-hungry on-chip inductors and DC-block capacitors.

3.3.5 ASIC Control Circuit and Digital to Analog Converters

The integrated MSF LE control circuit is presented in this section along with the DACs. The control circuit operation involves the routing of data packages in a grid network where the payload of the package is the eight single-byte inputs for the eight DACs, which in turn connect to the four analog V_R and four V_C voltages of



(a) (b) (c)

Figure 3.12: (a) Selected MSF LE pin location and configuration. Configuration (b) and (c) are alternative pin locations options that were not pursued.

the four LEs.

Therefore, the control circuit has two main operations. First, to provide the digital input to the DAC and in turn tune the complex impedance of the unit cell. Second, to send or receive data packets to / from neighbouring nodes in order to deliver the payload to the appropriate node of the network.

The ASIC control circuitry takes into account constraints arising both in the application and the manufacturability of the ASIC. Also, asynchronous communication is necessary because using a crystal oscillator and clock signal for synchronization (synchronous communication), can contribute to high power consumption, high EM noise generation, and prevent the scalability of the MSF. Given the large number of dies required to populate the MSF, a relatively low-cost technology is needed and the die size needs to be minimized, to maximise the number of ICs per wafer. Also, the size must be large enough to be handled by automated pick-and-place machinery. A 2 mm $\times$ 2 mm size was selected, and therefore the maximum number of WLCSP solder bumps that could be accommodated in this area was 25. To accommodate these restrictions, the control circuit has two serial input channels and two serial output channels, as shown in Fig. 3.5. Also, the current implementation is fully asynchronous, and the communication is carried out by handshaking between the transmitter node and the receiver node [96, 99].

Each control circuit is part of a grid that intelligently moves packets to the destination node and configures the complex impedance values that are used as inputs to the varistors and varactors. In Fig. 3.13, a 4 $\times$ 4 grid network of MSF loading ASICs is shown. The nodes have four orientations (a, b, c and d). This way, the network can be formed by designing only one control circuit. The corner nodes

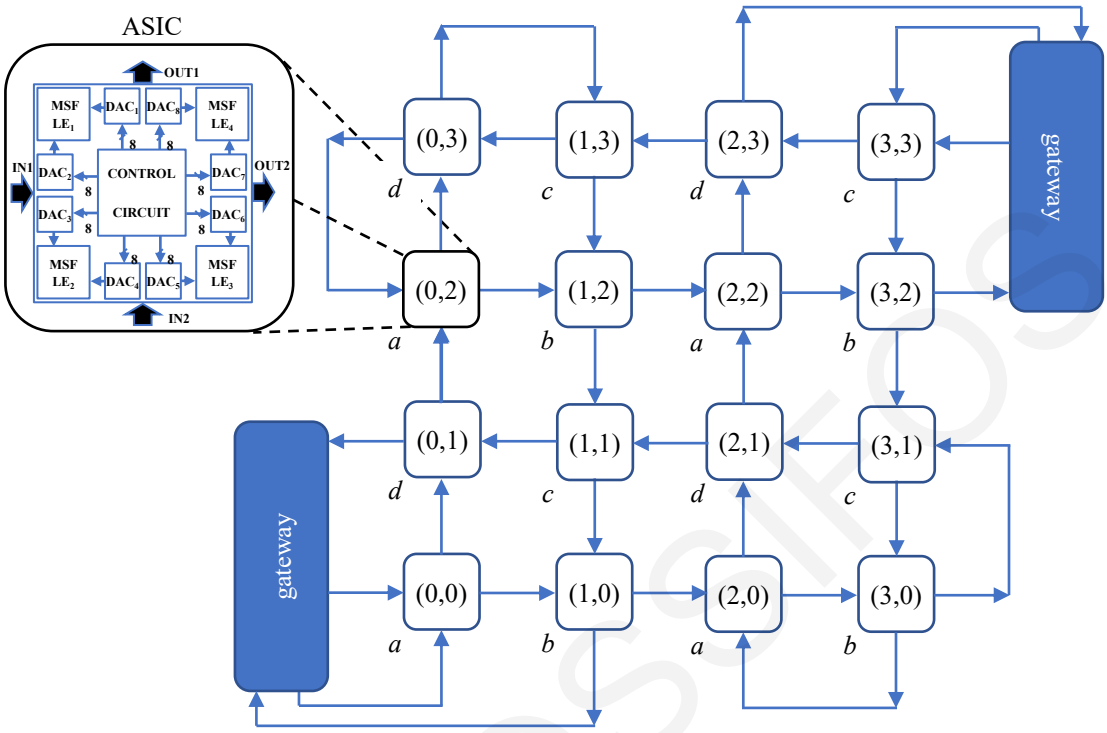


Figure 3.13: A 4 × 4 grid with two gateways and wraparounds forming a network. Letters a, b, c and d correspond to the orientation of each node.

are connected using wraparounds to ensure that there is more than just one path to reach every node in the grid. Therefore, even when a node is faulty, the network will not collapse. The gateways are the means to convey packets to the grid and they have full computing capabilities and resources. They are responsible for feeding the packets into the network, receive packets, apply fault detection mechanisms or even act as intermediate nodes in the network. The network can adopt intelligent routing algorithms, so that the configuration of all the unit cells is done fast and reliably. In [93], the authors present two routing algorithms with fault tolerance mechanisms that can be adopted by the control circuits used in this design.

The data packet, once received by the destination node, is temporarily stored in the node's buffer until verification confirms that the entire packet has been received with no errors. Then, the configuration bits are copied to the memory.

The stored bits directly drive the 8-bit DAC, producing the analog voltages needed to bias and configure the LEs. A two-stage resistor string DAC architecture was adopted for the eight DACs [100]. The DAC's output needed to be monotonic, accurate and it needed to occupy a small area in the ASIC. The current required by the MSF LE is negligible, therefore the DAC had no need of an output buffer.

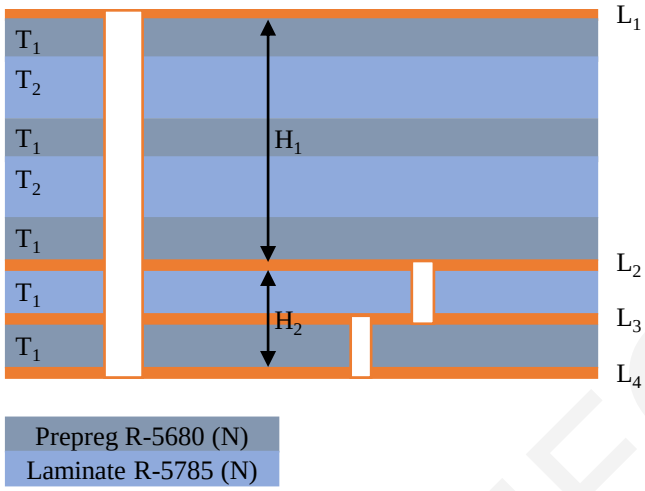


Figure 3.14: The 4-layer PCB stack adopted for the example MSF design.

This requirement and its simplistic design made the two-stage resistor string DAC an attractive solution. The analogue voltages produced by the DACs are inputs to the MSF LEs (V_R and V_C biases). These biases will change the MSF LE impedance, which will in turn alter the MSF surface impedance.

3.3.6 Manufacturability of Metasurface PCB

This section describes the production processes toward manufacturing the actual MSF in a large industrial PCB format. The MSF sub-wavelength periodic structure and its anisotropic PCB stack are demanding, and push the capabilities of the manufacturing process. Asymmetric PCB layer stacks are commonly avoided, since the different thermal expansion coefficients of the PCB materials and or the metallization will produce a warped PCB. The asymmetric PCB layer stack demanded from the correct unit cell operation, was the drive to adapt a homogeneous material layers shown in the Fig. 3.14. The PCB stack consists of Megtron 7N materials (Fig. 3.14), R-5785(N) laminate and prepreg R-5680(N) with a thicknesses of T_1:100 μm and T_2:750 μm. The laminate R-5785(N) and the prepreg R5680(N) have the same electrical properties, dielectric constant of 3.35 (ε_r) and a dissipation factor of 0.002 (tan(δ)). This makes the layering across the thickness H_1 and H_2 act as an electrically homogeneous material.

The four-layer PCB presented consists of four metal layers, as shown in Fig. 3.14. In terms of electrical connectivity, L_3 and L_4 serve for routing, while also a plane is positioned on L_3 that is connected to V_{dd} and on L_4 a metal fill is placed that is

connected to the ground (L_2). L_4 includes the chip's footprints with the routing of the tracks for the asynchronous communications and global signals. The remaining area of L_4 is covered with copper fillers that are connected to the ground. In addition, the three global tracks are distributed to the whole tile.

The dimensions of the PCB are 302.4 mm × 302.4 mm which translate to approximately 5×5 λ^2, at the design frequency (5 GHz). A top and bottom view of the PCB can be seen in Fig. 3.15(a) and Fig. 3.15(b), respectively.In Fig. 3.15(c), the routing of the chip's pads is shown. An array of 5×5 pads is used as a the footprint of the WLCSP dies. The diameter of the pads is 0.25 mm, with a pitch of 0.4 mm (center to center). One of the pads is not used to indicate the correct orientation of the chip. The track width within the chip's footprint is 0.045 mm to enable proper distribution of the tracks. The four corner pads are connected to L_1 through L_1-L_4 vias. Three pads on each side are used for the asynchronous communication with the neighbouring chips. Another two pads are dedicated to the global signals. An additional two pads are used for digital V_{dd} and Gnd, and two pads for the analog V_{dd} and Gnd. The orientation of each chip is hardwired by two pads to V_{dd} or Gnd. When populating the board, the chip's actual orientation can be distinguished by the asymmetry of the pads, where one ball of the 25 is intentionally omitted. Asynchronous tracks are symmetrically routed to match the delays between lines.

Four unit cells were arranged in a scalable design with the appropriate orientation of the chips. Starting from the *a* orientation, the chips were rotated 90° clockwise from the *a* to *d* orientation. At the edges of the PCB, multiple low-insertion-force (LIF) connectors are placed to enable its connection to neighbouring PCBs. Thus, scalability can be achieved. These connectors can also be used for the connection of the gateway. In addition, pads dedicated to power tracks are distributed all over the edges of the PCB for better distribution of the power.

The PCB shown in Fig. 3.15 was manufactured. Even though the metallization layers were not symmetric in the PCB stack the PCB showed very little warpage, and the warpage was less than 100 μm. A post fabrication cross-section of the PCB is shown in Fig. 3.16. The PCB stack thickness deviated from the nominal PCB thickness, by approximately 0.4 mm. H_1 thickness was measured at 2137 μm instead of 1800 μm and H_2 thickness was measured at 265 μm instead of 200 μm as can be seen in in Fig. 3.16(a). This 18% increase in H_1 thickness is mainly attributed to a deviation in prepreg and lamination thicknesses in the stack compared to the

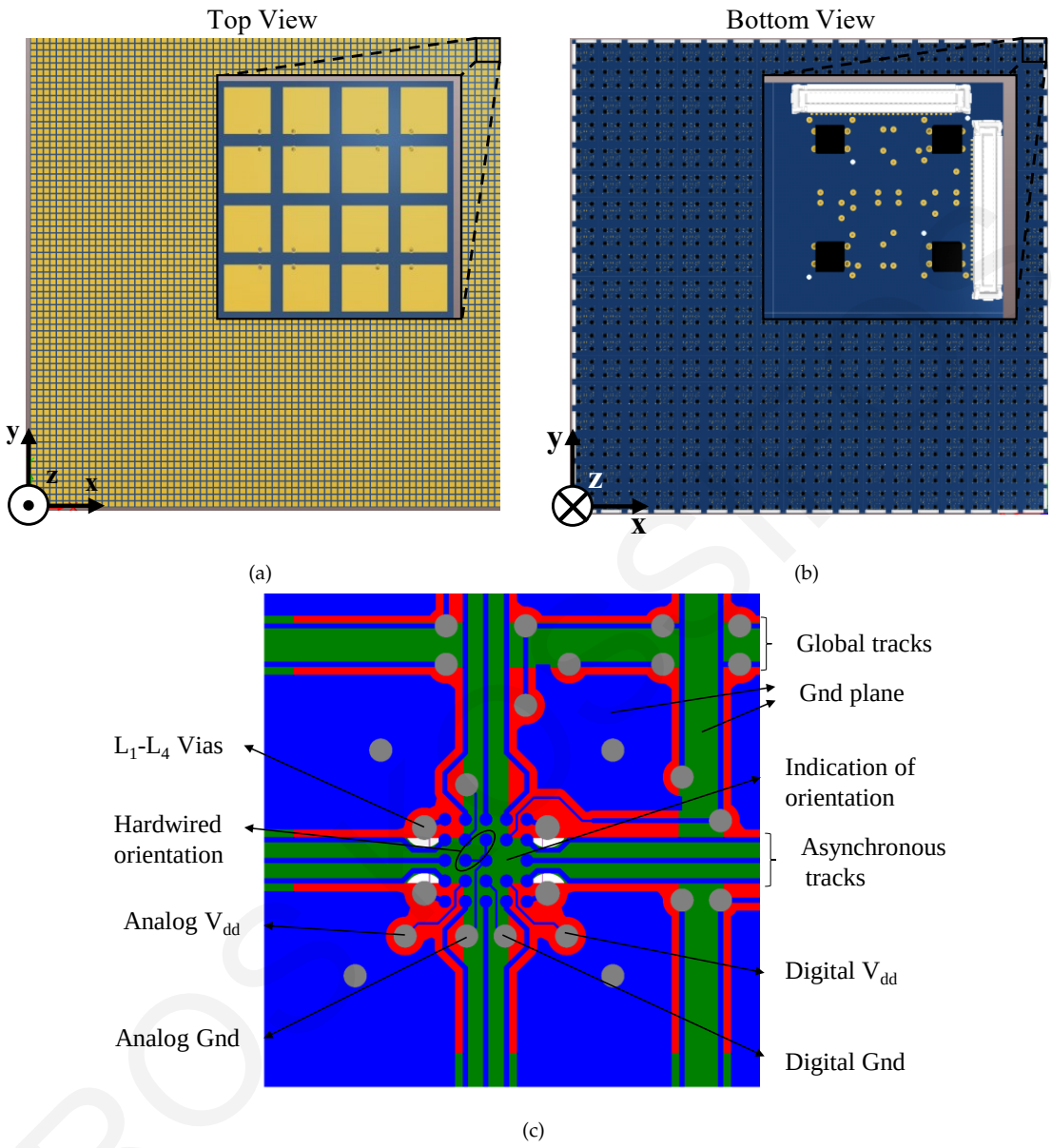
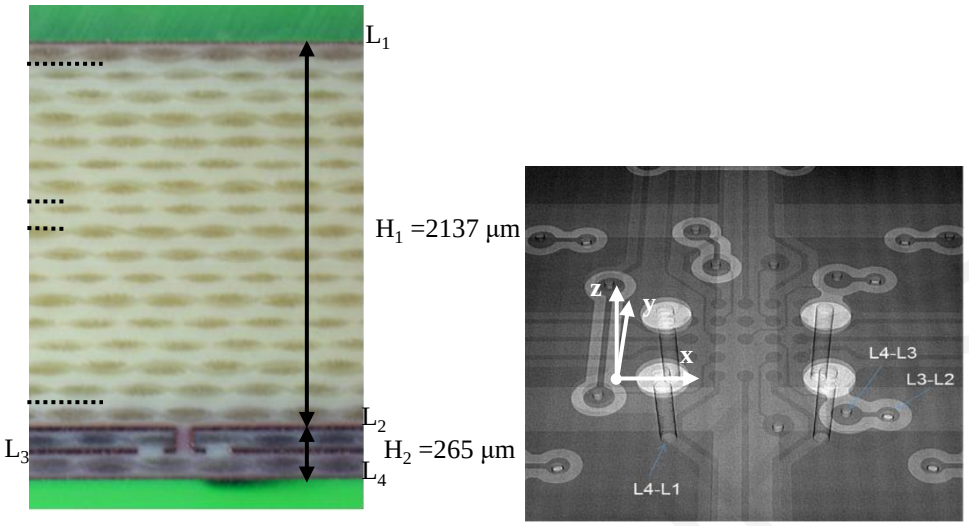


Figure 3.15: MSF PCB, (a) top view, (b) bottom view, and (c) routing of chip's pads.

nominal ones, and from slightly higher copper thicknesses after electroplating on the copper layers. The measured H_1 and H_2 thicknesses show in Fig. 3.16(a) were subsequently used in electromagnetic simulations.

3.3.7 Selected Technology Validation

The MSF LE circuit was fabricated in a commercially available 180 nm CMOS technology using a MPW provided by Europractice [101]. The 180 nm technology's nominal supply voltage was 1.8 V. This MPW step was intended to catch any variations in the circuit performance or even in its operation before a full wafer fabrication. Along with the LE, individual circuit elements were also included for



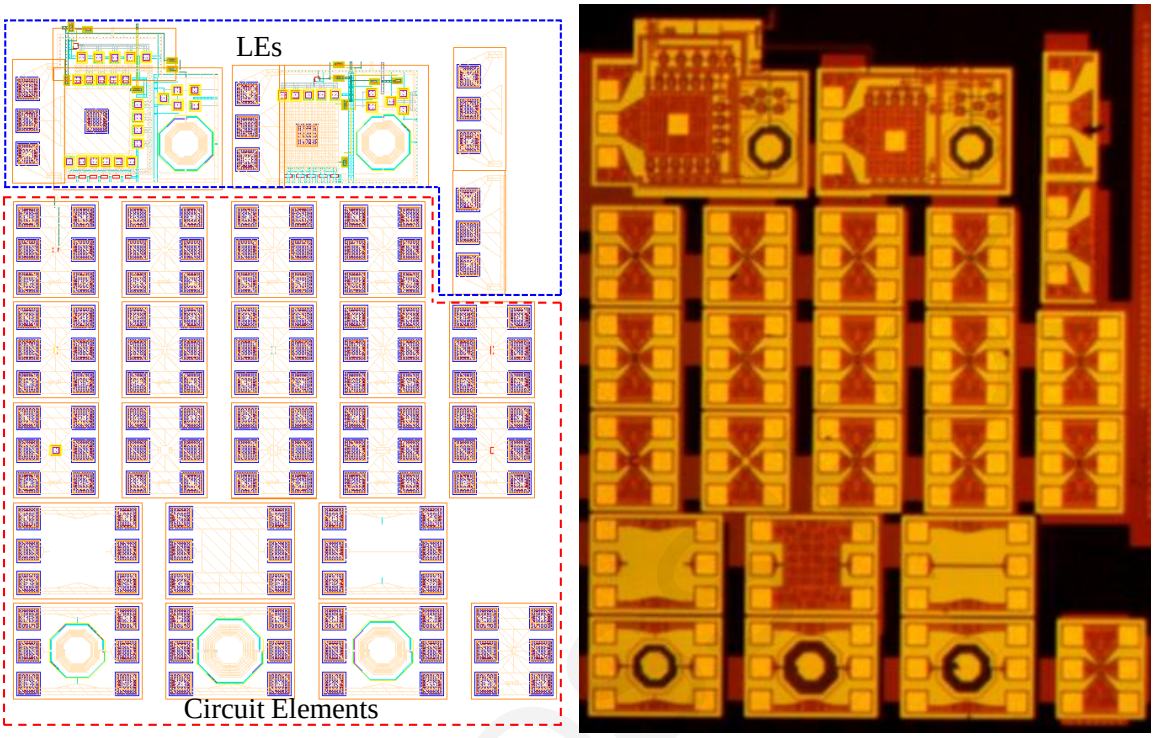
(a) (b)

Figure 3.16: (a) Cross section of the 4-layer stack, and (b) X-ray photograph of the manufactured PCB.

Table 3.2: List of individual circuit element structures.

No.	Circuit Element Description
1	Three inductors of different sizes with two-port de-embedding structures
2	A MiM capacitor and two-port de-embedding structures
3	Three MOS-varactors of different capacitance and two-port de-embedding structures
4	A varistor with its two-port de-embedding structures

technology validation, as shown at the bottom of Fig. 3.17(a) and listed in Table 3.2. These circuit elements (inductors, MiM capacitor, MOS-varactors, varistor) were placed within GSG-boxes to be measured separately for troubleshooting purposes. The provided models (with the PDK) of the circuit elements were used in combination with the GSG-box and open, short and through de-embedding structures were designed in Keysight advance design system (ADS). With these de-embedding structures, OS and OST de-embedding [64] were performed for all the circuit elements in simulation and measurements as described in Section 2.3.1.1 and Section 2.3.1.3, respectively.

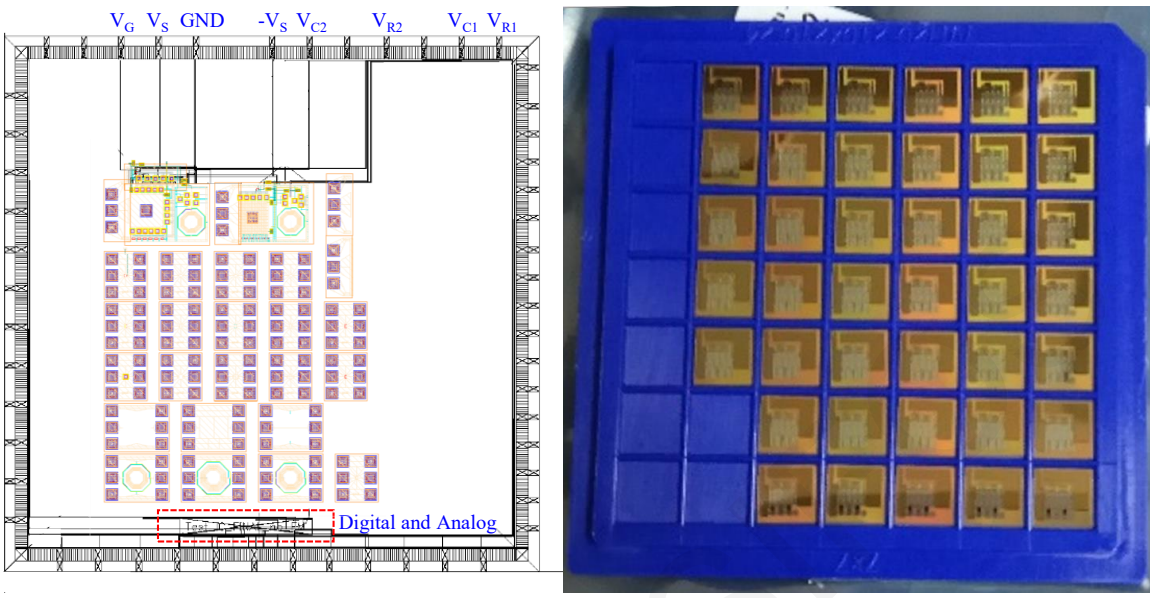


(a) (b)

Figure 3.17: RF measurement structures, which include the LEs and individual circuit elements. In (a) the measurement structures are shown in the CADENCE layout environment while (b) shows a photograph of the fabricated ASIC.

All RF measurement structures shown in Fig. 3.17(a) were placed in a 5 mm × 5 mm layout, as shown in the manufacturing blueprint in Fig. 3.18(a). In this 5 mm × 5 mm layout, analog and digital biasing pads were placed at its perimeter where V_C, V_R, ground (GND), positive (V_S) and negative supply ($-V_S$) nodes are connected. Additionally, a V_G pad was placed on the top left, to bias the gate of the MOSFET used as a varistor. Analog and digital circuits were placed in this layout to test their performance and catch any potential errors. These can be seen at the bottom of Fig. 3.18(a) enclosed by a red dashed line. The remaining pads at the perimeter were used by the analog and digital circuits. Forty 5 mm × 5 mm dies were produced by this initial MPW run, which can be seen in Fig. 3.18(b).

A close-up view of the fabricated LE can be seen in Fig. 3.19(a) along with the open-short de-embedding structures in Fig. 3.19(b) and Fig. 3.19(c). The LE's varistor and the varactor were implemented through multi-fingered MOSFETs, as described in Section 3.3.1. This was implemented to obtain a low static power consumption. The pitch of the GSG pads is 150 μm, and the LE circuit area is 640 μm by 520 μm, where the inductor is the largest on-chip component.



(a) (b)

Figure 3.18: Test ICs containing RF measurement structures and analog and digital circuits. In (a) the complete layout in the CADENCE layout environment is shown, while in (b) 40 manufactured dies can be seen.

The MSF LE were designed to be integrated on a ASIC, which is then packaged through a WLCSP process that puts solder bumps directly on the die, thus avoiding the parasitic inductance of wirebonding and other more complex packaging techniques [97, 98]. The MSF LE circuit is positioned in the physical layout around a rectangular top layer metal, labelled "Pad" at the centre of Fig. 3.19(a), to emulate the effect of a solder bumping pad. On the left side of the bumping pad, ground signal ground (GSG) probe pads can be seen that are connected to the LEs via a taper. On the top side of the bumping pad the DC block capacitor (C_1) and the varistor (M_1) are positioned. The DC block capacitor consists of five 1.8 pF MiM capacitors. The varactor (M_2) is positioned at the lower side of the rectangular pad and consists of five 0.43 pF MOSFET varactors, where the finger width and length of the device fingers are adjusted to increase the quality factor as described in Section 2.2.2, [62]. The ground pads are connected to a metallic ring around the rectangular pad. The on-chip RF choke (L_1) is on the right of the rectangular pad. Between the RF choke and the V_C pad, MiM capacitors are placed to reduce the impedance of the node. Additionally, each biasing node has an electrostatic discharge (ESD) protection device connected to it [102].

The measurement set-up for the on-wafer measurements can be seen in Fig. 3.20. The MSF LEs were measured by supplying the appropriate voltages, applied to the

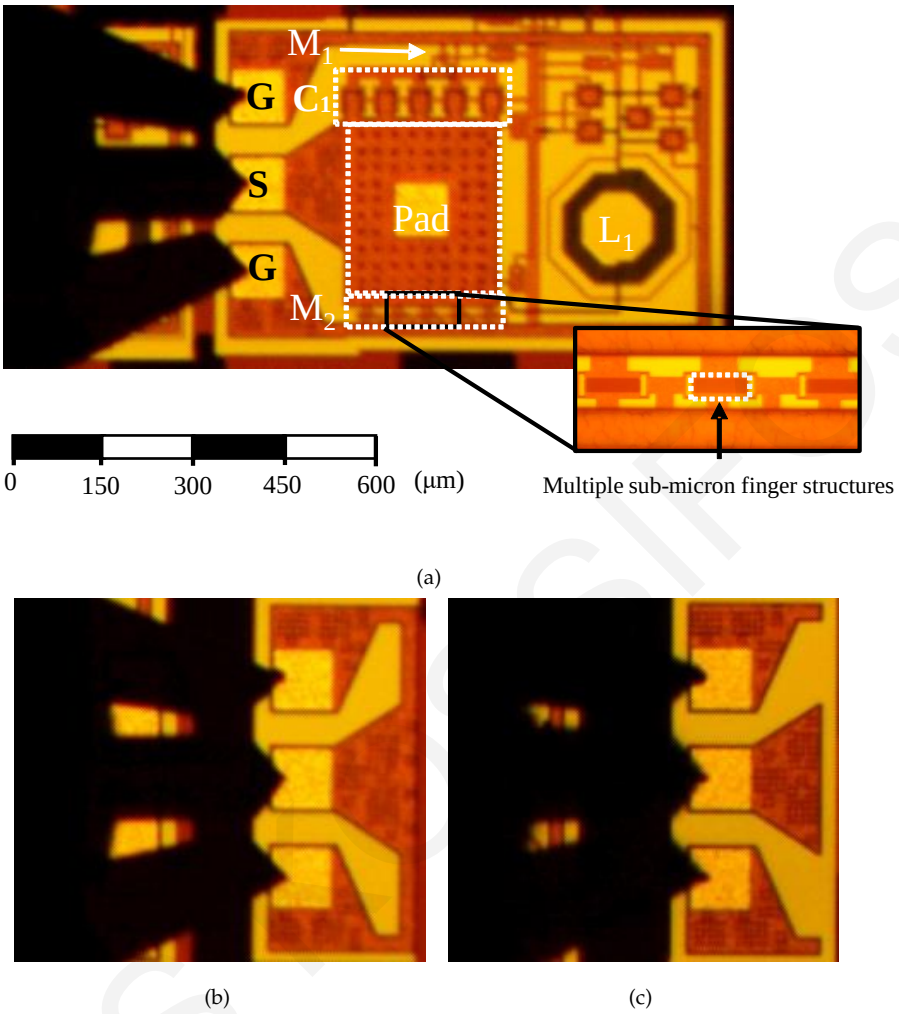


Figure 3.19: Photographs of the fabricated and measured structures. (a) MSF integrated LE circuit (DUT) and the de-embedding structures, (b) short circuit, and (c) open circuit.

V_R and V_C nodes from a Keithley 4200-SCS and the S-parameters were obtained from an Agilent E8363B VNA. V_R was incrementally increased from zero to 1.8 V, which is the maximum operating voltage of the technology, and V_C is incrementally increased from the (negative) minimum operating voltage of -1.8 V to the maximum of 1.8 V. This results in a matrix of measurements, which are de-embedded by using the technique proposed in [67] and converted to parallel configuration RC values. The technique used [67] is a one port adaptation of the OS technique (Section 2.3.1.1).

The equivalent parallel configuration RC values are plotted in Fig. 3.21 at a frequency of 5 GHz for various biasing levels. For V_R the following biasing levels (in mV) were used: 0, 400, 500, 600, 700, 1000 and 1800, and for V_C: -1800, -250, -100, 0, 100, 250, 1800. It should be noted that in the final ASIC implementation, a digital network controller will be used that includes multi-bit DACs to precisely control these voltage levels at mV resolutions. From the measurements, it can be seen that

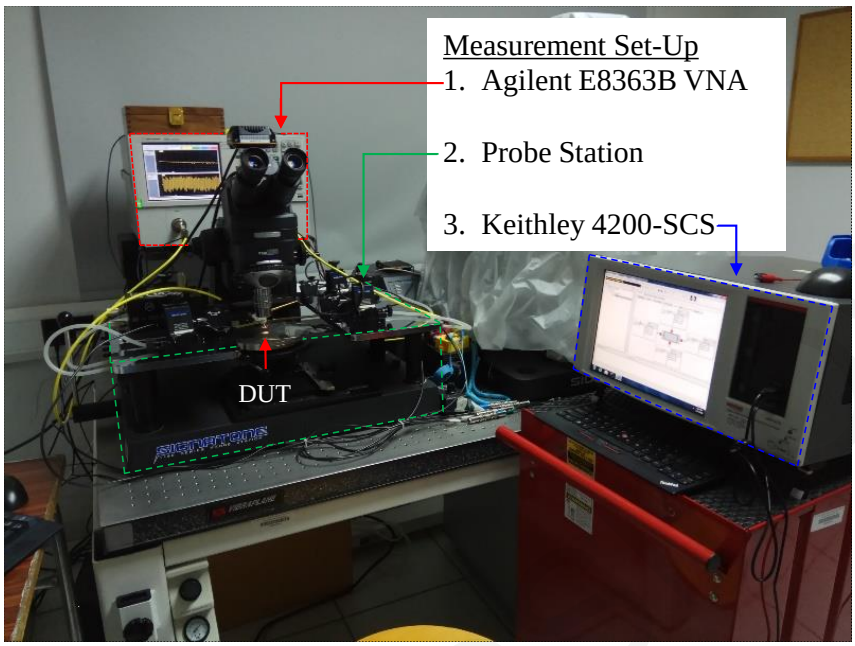


Figure 3.20: Loading element's on-wafer measurement set-up. The set-up consists of a probe station equipped with two MW probes and DC probes, a vector network analyser (VNA) acquiring the S-parameters and a semiconductor characterization system providing the biasing voltages.

a distinct area is obtained, where the minimum equivalent parallel resistance is approximately 25 Ω and the maximum equivalent parallel resistance is approximately 265 Ω. The equivalent parallel capacitance range obtained is approximately from 2.1 pF to 5 pF. In Fig. 3.21, the solid lines are plotted by keeping the V_C biasing level constant and by varying V_R. Similarly, in Fig. 3.21 the dashed lines are plotted by keeping the V_R biasing level constant and by varying V_C. This is done to show how the biasing voltages affect the LE. By increasing the gate voltage (V_R) of M_1 (varistor), the equivalent parallel resistance value decreases, and by increasing the gate voltage (V_C) of M_2 (varactor) the parallel capacitance decreases. There is also variation in the equivalent capacitance for different varistor bias values. This can be attributed to the DC block capacitance and the parasitic diodes formed at the source and drain regions of the MOSFET. Also, variations in resistance have been observed for different varactor biasing values, which are attributed to the quality factor of the varactor changing with voltage, as is generally known from the Q-V curves (see [62]).

Through the measurements of the individual circuit elements listed in Table 3.2 and shown in Fig. 3.17, discrepancies between circuit element simulations and measurements were identified. These measurements can't be shared without voiding non-discloser agreements, but the findings can be elaborated for the purposes of this

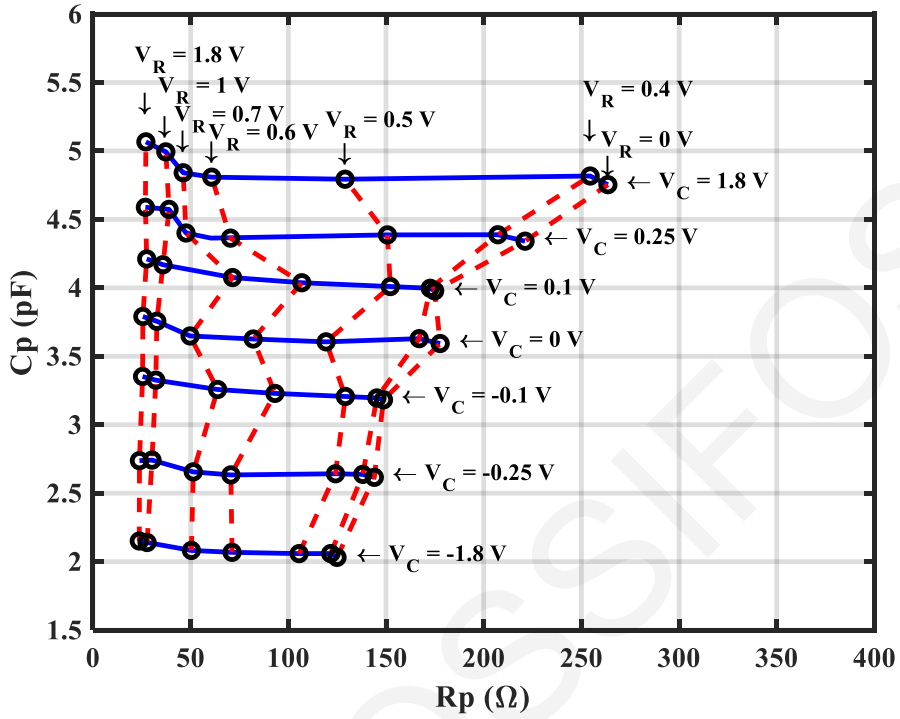


Figure 3.21: Measured parallel *RC* range for the MSF LE at 5 GHz.

chapter. The measured *RC* perimeter in Fig. 3.21 was expected to extend to a larger parallel resistance (R_P) range and therefore obtain a larger *RC* area. This reduction in *RC* area was more pronounced in the negative V_C biasing voltage. Through individual circuit element measurement, the main culprit for the parallel resistance reduction was found to be the MOS-varactor. The MOS-varactor's quality factor (Q) seemed to be optimistic in the provided device model in the PDK compared to the measurements. The inductors and MiM capacitor's quality factor slightly were lower and therefore also contributed to some extent to the parallel resistance being slightly smaller.

These findings made this intermediated step, the MPW fabrication and measurement of the LE, beneficial to the overall PMSF development. Multiple LEs were measured with very similar *RC* areas. One can argue if the correct path was to use these measurements in the EM co-simulations in Kesight ADS. With only a very small sample of LEs measured, and the entiyer IC population originating from the same the same wafer one can't draw an incorrect conclusions. Multiple measurements over multiple wafers were needed to correctly predict the correct LE's *RC* range since it relies on the quality factor of its sub-components. A different approach was adapted, in the next PMSF design in Chapter 4 a conservative *RC* range was used to

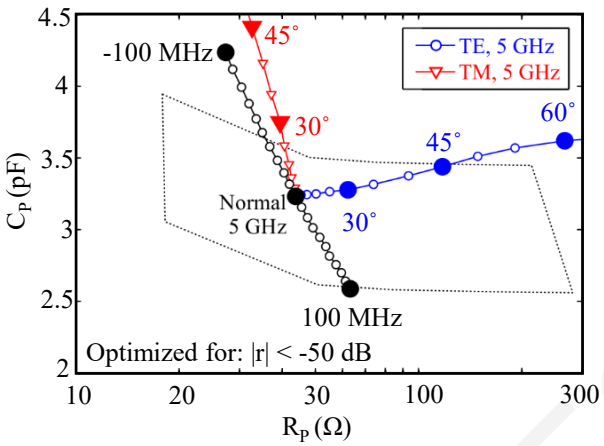


Figure 3.22: Required LE *RC* values for perfect absorption of *y*-polarized oblique incidence for both TE and TM polarizations at 5 GHz.

evaluate the performance of the PMSF as to ensure it's operation over large quality factor variations.

3.4 Metasurface Performance

The example unit cell geometry targeted a perfect absorber at a design frequency of 5 GHz. At this frequency, absorption of TE-polarized waves (see legend in Fig. 3.2(a)) was studied at various angles of θ while keeping the angle $\phi = 0°$, corresponding to the *xz*-incidence plane with reference to Fig. 3.3(a). The absorption of TM-polarized waves was studied at various angles of θ at an orthogonal plane with respect to the TE polarization ($\phi = 90°$), corresponding to the *yz*-incidence plane with reference to Fig. 3.3(a). This discrimination between the TE and TM planes of incidence is caused by the asymmetric connection (in the *x*- and *y*-directions) of the L_1-L_4 vias to the MSF patches on the top layer, as shown in Fig. 3.3(a). The discrimination between the TE and TM planes for *y*-polarized incidence arose as a tradeoff between fabrication limitations, available loading impedance ranges and the design target for angle-tunable perfect absorption for at least one polarization [95]. Oblique TM polarization has narrower angle tunability due to the E-field component parallel to the vertical vias (L_1-L_4 and L_4-L_2), which gives rise to currents and mutual coupling between the lateral traces of the grounding and RF terminals (in L_4). Finally, *x*-polarized incidence in both TE and TM planes will severely underperform due to the trade-off mentioned; the physical reason is the large distance of the through vias to the edges of the patches along the *x*-axis, Fig. 3.3(a).

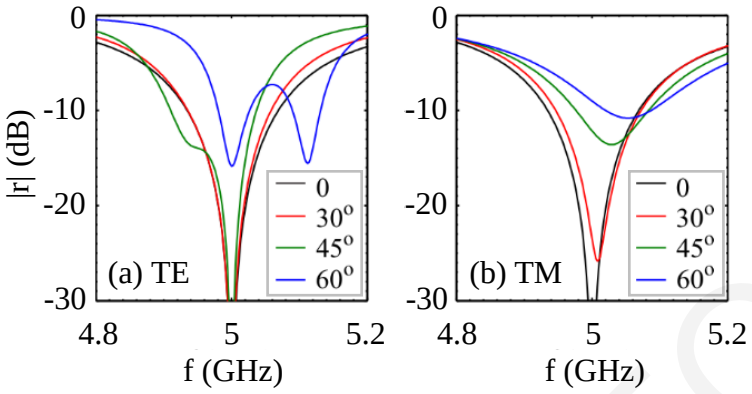


Figure 3.23: Reflection spectra for optimal *RC* values within the range provided by the ASIC, for oblique incidence for (a) TE, and (b) TM polarizations.

The functional MSF performance can be seen in Fig. 3.22, where the optimal *RC* values for absorption are overlaid with the 180 nm semiconductor process range to demonstrate the capabilities of this example unit cell. Given the envisioned 8-bit resolution of the DACs biasing the LEs can seemingly continuous tune its *RC* response to all the values within the *RC* perimeter plotted with a doted gray line(in Fig. 3.22). The optimum *RC* combination for minimizing reflection (maximum absorption) is plotted with blue circular and red triangular markers for TE and TM polarizations, respectively. Since the LEs can match these *RC* combinations, the unit cell can perfectly absorb at the target frequency of 5 GHz for an angle range. For TE and TM polarizations the *RC* combinations overlap with the LE's *RC* perimeter from normal up to 45° and 25°, respectively, and therefore, the MSF can perfectly absorb over that angle range. The TE angle range is larger, given that this was the target polarization in the design process.

The performance is further examined in Fig. 3.23, where the reflection coefficient is plotted for various angles of incidence as a function of frequency considering the optimum *RC* load for each case. At normal incidence, the reflection coefficient is less than -50 dB. This degrades as the angle of incidence increases, as shown in Fig. 3.23(a)a for TE polarization. However, it remains below -30 dB up to 45° that can be covered with the 180 nm technology, accommodating the majority of RCS reduction applications. Similar behaviour is found for the TM polarization, depicted in Fig. 3.23(b). The reflection coefficient at 5 GHz remains below -20 dB up to 25° that can be covered with the 180 nm technology. Finally, the optimal *RC* values for normal incidence are plotted in Fig. 3.22 for 5±0.1 GHz using black

circular markers to illustrate the frequency effect on the *RC* values. The bandwidth that can be accommodated for normal incidence is approximately 150 MHz around the target frequency of 5 GHz.

3.5 Discussion and Conclusion

For this given MSF example design, the targeted polarization affects the technology selection. From Fig. 3.22 it can be seen that TM polarization does not need large resistance tunability, but requires a larger capacitance range. If emphasis were to be placed on the TM polarization, then a 350 nm technology would have been more appropriate. The 350 nm technology can easily be adapted to a TM polarization absorber and is more affordable. Similarly, for solely TE polarization performance, the 65 nm technology is more appropriate, since TE requires a larger resistance tuning range and a lower capacitance range. As the semiconductor manufacturing costs increase exponentially with decreasing feature sizes, a trade-off results in the choice of 180 nm technology. This can realize large angles of incidence that would satisfy the majority of radar cross section (RCS) reduction applications.

An example PMSF absorber design has been presented and has been used to demonstrate the feasibility of a low-cost, low-power ASIC design for adaptive and programmable MSFs. The ASIC design has been explored for various technology nodes, where the performance has been evaluated in view of implementing tunable complex impedance LEs. After selecting the appropriate 180 nm semiconductor process technology with a nominal supply voltage of 1.8 V, it has been demonstrated that perfect absorption can be achieved (-50 dB reflection coefficient) at normal incidence as well as at oblique angles up to 45° for TE polarization and 25° for TM polarization assuming an only positive supply voltage.

Even though the design presented demonstrated the feasibility of producing a PMSF absorber, the design can't justify the time consuming process of producing ASICs for the following reasons:

- The textured top side of the PMSF, the rectangular patches, were chosen for this design since they are analytically well understood (Section 2.1). Square patches don't posses a series inductive component in their equivalent circuit like other unit cell shapes, Jerusalem crosses etc. [103–106]. This inductive

component was expected to limit the frequency bandwidth and angular range of the PMSF. Even so, the rectangular patch type unit cell couldn't achieve a satisfactory performance without focusing on one polarization and compromising the other. This was done by breaking the unit cell's symmetry. Not to mention that for practical manufacturing reasons, namely the placement of the ASIC below the ground plane and its connectivity to the textured top side made the analytical modelling of the unit cell difficult without the use of none-analytical methods.

- The top-level architecture of the ASIC incorporates four individually addressed LEs. The ASIC's footprint or LEs layout was designed to be symmetric when rotated within the unit cell. This was meant to give the ASIC an added flexibility compared to the theoretical or initial work presented in [92]. Control of the reflection coefficients for both x and y polarizations and cross polarization conversion was favourable. This couldn't be achieved by this design since it required a larger RC range than the one provided by the LE. The co-authors of [107], strived to control both polarizations and polarization conversion, but settled on a suboptimal performance, even when using a LE RC range from circuit simulation, which are not effected by layout parasitics [95].

- The design frequency of 5 GHz was chosen for demonstration purposes, a compromise between cost, manufacturability and ease in the experimental validation stage. The measurements of the PMSF required it to cover a large enough area ($5 \times 5\ \lambda^2$) in order to minimize the edge effects. This size could have been manufactured with the PCB manufacturing facilities of the VISORSURF consortium [55]. The size of the bistatic set-up used to measure the PMSF's reflection coefficients would need to excite the PMSF with a plane wave. In order to excite the PMSF with a plane wave, either the distance between the antennas and PMSF need to be greater than the Fraunhofer distance or lenses need to be used between the PMSF and the transmitting antennas (Section 2.3.2). Lenses were not available and the anechoic chamber dedicated for the measurement was restricted in size, therefore, a higher frequency was favoured as it will require less distance between the PMSF and the transmitting antennas. As for the cost of the PMSF, migrating to a higher frequency the area of the PMSF becomes physically smaller, thus relaxing the measurement

and manufacturing constraints, but the semiconductor process would need to migrate from silicon to SiGe or GaAs. These semiconductor processes (SiGe or GaAs) were too expensive to pursue.

The above points opted the design of a more complex PMSF design. The design is described in Chapter 4. Part of the work in Chapter 4 pre-dates the work in this chapter. The design utilizes the same ASIC, while aiming to increase the functionality of the PMSF by alleviating the constrains imposed on the work in this chapter.

The design in Chapter 4 utilizes a different PMSF textured layer which is not well understood analytically, but which provides more degrees of freedom compared to the rectangular patch design proposed in this chapter. Furthermore, with the establishment of sub-6 GHz fifth generation (5G) networks, operating at 3.3 GHz to 3.8 GHz (S-band), a design operating in the S-band with a center frequency of 3.6 GHz would enable the PMSF to be utilized in a 5G network in various antenna and future wireless environment applications, while also increasing the LE *RC* range. Furthermore, the frequency reduction impact in the experimental validation will be tolerable.

3.6 Contribution

The multidisciplinary work presented in this chapter was partially published in [22,107] and had contributors from four institutions within the VISORSURF consortium [55]. The four institutions are UCY (University of Cyprus), FORTH (Foundation for Research and Technology - Hellas), Aalto Univesity, and IZM (Fraunhofer Institute for Reliability and Microintegration). Contributors affiliated with UCY predominantly contributed to the ASIC design, actual PCB layouts for production, and chip powering/communication/networking aspects. Contributors affiliated with FORTH and Aalto predominantly contributed in the MSF electromagnetic design, related PCB material specifications, the unit cell geometry and absorber performance evaluation. Contributors affiliated with IZM provided fabrication guidelines for the design and handled the PCB manufacturing.

Explicitly, the author contributed with the design of the first MSF LE, it's topology within the ASIC, the selection of the semiconductor technology among the economically affordable technologies and the LE's connectivity to the unit cell.

Chapter 4

Multifunctional Dual Polarization ASIC Enabled Metasurface

In this chapter, the metasurface (MSF) loading elements (LEs) are utilized in an innovative MSF, where the LE's small size and simple tunability are exploited. The LEs are designed such that four of them can easily fit on a single ASIC and leave sufficient space for on-chip mixed-signal circuits for LE control, as well as a digital network controller. The selected semiconductor technology presented in Chapter 3 is used, and the experimental results are used to design an innovative programmable metasurface (PMSF) design. Through targeted electronic and electromagnetic co-design, an innovative metasurface unit cell is implemented and a programmable metasurface is demonstrated. Experimental measurements of the fabricated loading element circuit in a 180 nm complementary metal-oxide semiconductor (CMOS) technology are used in an electromagnetic simulator to demonstrate programmable perfect absorption at normal and oblique angles of incidence for both transverse electric (TE) and transverse magnetic (TM) polarizations. The LE size allows four to be realized on a custom ASIC, with these, the PMSF is shown to control independently and simultaneously the absorption of both TE and TM polarizations. Furthermore, DAC and digital control circuits can be integrated with in the same ASIC.

Assuming multi-bit discrete states, provided by the DAC biasing the LEs, a finely tuned amplitude and phase response can be obtained. With this ability, complex wavefronts can be generated. Complex wavefronts, such as multiple pencil beam patterns are demonstrated, where each pencil beam's polarization can be

programmatically set between linear, circular, or even elliptic polarization. The presented design operates in the vicinity of 3.6 GHz, and therefore has the potential to be incorporated into multiple-user mobile communication systems, including 5G networks and future wireless telecommunication networks.

It is shown that these ASICs offer the potential to increase the functionality of PMSFs while reducing their cost and energy consumption. This approach requires a large number of ASICs and entails significant challenges for the PMSF development. Statistical models of RF and MW components are not provided by the majority of commercially available semiconductor technologies, so their effects are usually tackled in an empirical manner. These RF and MW components are used for the loading of each unit cell within the PMSF, and the effects of component's mismatch cascades to the scattered far field (FF) of the PMSF. A study of the effects of mismatch on the scattered far field of an ASIC-equipped PMSF is presented for the case when the PMSF is set to perfectly absorb and when the PMSF is set to generate multiple pencil beams. A correlation between the degradation of the scattered far field and the components' standard deviation is shown.

4.1 Introduction

MTMs are composite materials which exhibited properties that can't be reproduced by materials found in nature. In the beginning of the century, MTMs experimentally demonstrated negative-refractive index by achieving simultaneously negative electrical permittivity and negative magnetic permeability [2]. The device was composed by an array of electrically small unit cells which. This unit cells, were composed by metallic split ring resonators and strips. Since then, researchers have constructed numerous MTM devices, of which two noteworthy examples could effectively cloak an object [3] and resolve beyond the diffraction limit [4]. MTMs with their aforementioned advance electromagnetic manipulation properties have found application in many RF and MW component devices [6,8,9].

Electrically thin, two-dimensional MTMs, known as metasurfaces (MSFs), are composite materials that have been shown to demonstrate many novel properties such as anomalous refection [12,83], perfect absorption [11,108] and nonlinear refection [109]. Electronically tunable MSF refectors [21,87] and absorbers [88] have been studied extensively. Furthermore, other means of tuning MSFs have been demon-

strated. Magnetically tunable MSFs have been demonstrated in [28] by employing ferrite material in the MSF. An investigation of an optically tunable MSF absorber, which does not employ semiconductor electronics in the radio frequency (RF) path has been shown in [30]. This was enabled by the optomechanic properties of poly disperse red 1 acrylate, which was shown to possess a memory effect [31]. Liquid crystals have been used in MSF design to achieve tunable behaviour [23,110], while graphene has also been used to achieve a tunable response [25,26].

By designing the reflection phase of each unit cell, MSFs have demonstrated wavefront manipulation such as multibeam reflection and simultaneous polarization conversion [89]. Additionally, isoflux patterns with circular polarization have been synthesized [90], and local multipoint distribution service patterns have been generated [91]. Programmable metasurfaces (PMSFs) have been recently demonstrated by individually tuning each MSF unit cell electronically through software in order to reduce the number of components and increase the resolution in synthetic aperture radar systems [111], and to dynamically control scattering, focusing and polarization rotation [32]. Also, by dynamically programming the modulation of the reflection phase, accurate control of the harmonic level of a non-linear reflecting MSF was obtained [35]. Furthermore, by programming the reflection phase of each unit cell, reflective [34] and transmissive [33] holograms were demonstrated in the microwave region.

The approach in [32] and [35] uses only reactively tunable commercially-available off-the-shelf (COTS) components and large distributed elements to create a high impedance in order to bias the MSF loading elements (LEs) from beneath the ground plane without affecting the RF signal. This is a simple and common methodology, but can prove to be difficult to implement since the MSF's unit cells are electrically small and leave little area for multiple tunable MSF LEs. Furthermore, their solution requires a lot of power to bias the diodes, making larger surfaces impractical.

An investigation of the MSF capabilities has been shown in [92], where the MSF was continually tuned by ideal adjustable complex impedance elements. The tuning range for the LEs required in this MSF design extends to zero resistance, which is not feasible. Furthermore, the work in [92] does not support independent absorption of the transverse electric (TE) and transverse magnetic (TM) polarization components.

In this chapter, the proposed MSF design operates using realistic component properties. This is demonstrated in simulations by using measured results taken

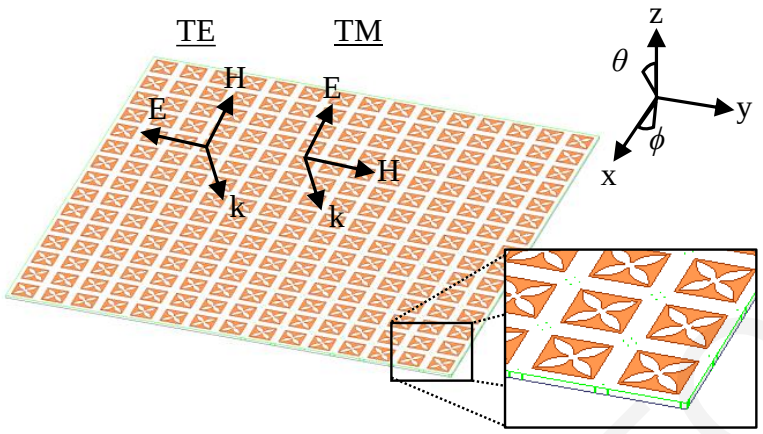


Figure 4.1: Proposed programmable MSF design. The MSF design consists of 14×14 unit cells.

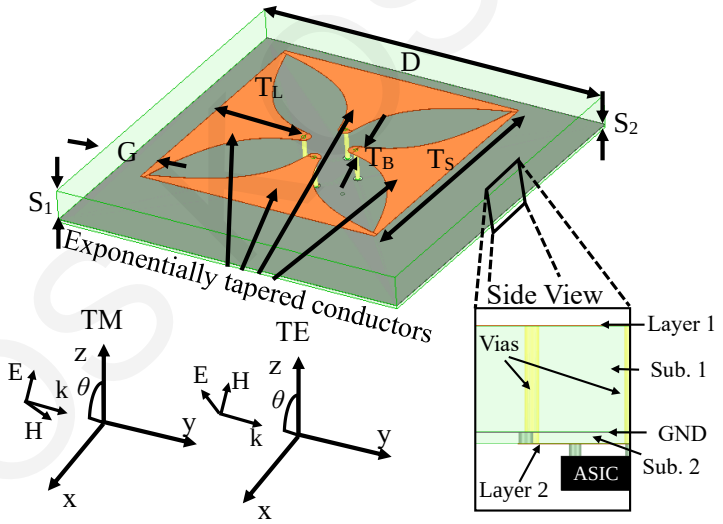
from a tunable complex impedance LE that was implemented in a commercially-available 180 nm CMOS technology. When biased, the proposed LE circuit draws a negligible amount of current, as opposed to [32]. The MSF's LEs are optimized for absorption in the low GHz region (S-band). The MSF is constructed from unit cells, each consisting of four exponential tapers, arranged in a cross-like structure, and connected at the center through a custom ASIC containing four MSF LEs, with independent tunability. Perfect absorption is achieved at normal and oblique angles, independently and simultaneously for both TE and TM polarizations, by using the ability to tune each LE individually. The MSF design presented in this chapter is a proof of concept. The ability to tune the absorption of both TE and TM polarizations with reduced power consumption, in conjunction with the low cost gained from the IC's mass production, enables the MSFs design to be deployed in numerous applications. At the design frequency of 3.6 GHz, the MSF can be used to absorb fifth generation (5G) network signals to improve antenna isolation. Furthermore, by addressing each unit cell individually, amplitude-only synthesis methods can be used to synthesize wavefronts. The design can be adapted to other frequency bands, thus enabling its use in other applications such as interference reduction in WiFi networks, and RCS reduction in stealth technology.

Furthermore, within the finite complex impedance area that can be achieved by the ASIC, other specific points that do not match the propagating wave's impedance for a given angle of incidence and polarization will reflect a portion of the incident wave with a finite amplitude and phase. This is particularly useful, since this provides control of both the amplitude and phase for each unit cell. By utilizing the control circuit and DAC that are integrated in the ASIC, each unit cell can be

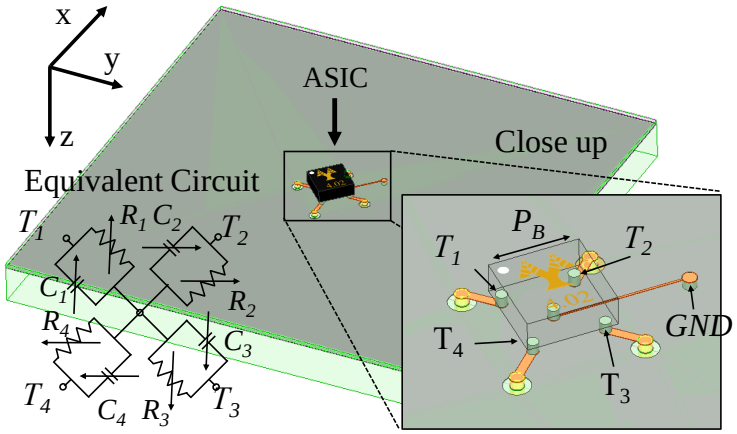
addressed and set to a specific reflecting amplitude and phase. This ability is true for both orthogonal polarizations (TE and TM).

The proposed design utilizing this ability is to be able to produce complex wavefont patterns. Wavefront patterns like multiple pencil beams, and a mixture of OAM and pencil beams where the reflection coefficients are calculated using a purely analytical methods [16]. With this ability, the proposed MSF design can not only find place in future MSF-aided indoor wireless telecommunication systems [38] but also in outdoor telecommunication systems where there is a need to support multiple users, such as 5G networks and future telecommunication systems.

This chapter is organized as follows. In Section 4.2 the unit cell of the proposed design is presented in detail. In the same section, it's perfect absorption capabilities



(a)



(b)

Figure 4.2: Programmable MSF unit cell geometry (a) top view and (b) bottom view showing the integrated MSF loads.

are demonstrated. The wavefront generation capabilities of the design are demonstrated in Section 4.3. A study on the effects of mismatch on ASIC-equiped MSFs is represented in Section 4.4. The chapter ends with the conclusion and a short discussion in Section 4.5.

4.2 Programmable Metasurface Unit Cell

The proposed PMSF unit cell geometry can be seen in Fig. 4.2. The top side of the unit cell shown in Fig. 4.2(a) consists of four exponentially tapered conductors (on Layer 1) terminated through four vias to the bottom side (on Layer 2) of the unit cell to an ASIC shown in the side view inset of Fig. 4.2(a) and Fig. 4.2(b). The ASIC contains four MSF LEs, each occupying a space of 520 μm $\times$ 640 μm, acting as tunable complex impedance loads. The substrate consists of two layers of R-5785(N) (ε_r=3.36, tan δ=0.0015 at the design frequency of 3.6 GHz) with a thickness of 2.137 mm (S_1) for the top layer (Sub. 1) and 0.215 mm (S_2) for the bottom layer (Sub. 2). Between the top and bottom layer a copper sheet is placed (GND), effectively acting as a ground plane.

On the bottom side, the ASIC connects to the four vias through the edge pins of the ASIC shown as T_1 to T_4 in the inset of Fig. 4.2(b). The vias are connected to the top side through circular openings in the ground plane. The center pin is connected to ground through a 45 μm width line. The ASIC forms an impedance network as shown in the equivalent circuit in the bottom left insert of Fig. 4.2(b), where it

Table 4.1: Programmable metasurface unit cell's geometry parameters.

Geometric Parameter	Dimension (mm)	Description
S_1	2.137	Top Substrate Thickness
S_2	0.215	Bottom Substrate Thickness
D	26.0	Period of the Unit Cell
G	4.0	Gap Distance
T_S	20.0	Taper Start Width
T_B	1.0	Taper End Width
T_L	7.0	Taper Length
P_B	1.6	ASIC's RF Port Pitch

consists of four parallel *RC* connections. This equivalent parallel *RC* connections are represented in this section as four complex impedances Z_A, Z_B, Z_C, and Z_D, as can be see in Fig. 4.3. These impedance, are referred to as MSF LEs and can be tuned individually within the finite range shown in Fig. 4.4.

The MSF LEs were measured by supplying the appropriate voltages, applied to the V_R and V_C nodes from a Keithley 4200-SCS and the S-parameters were obtained from an Agilent E8363B VNA as described in Section 3.3.7. The V_R and V_C nodes were initially set to their minimum voltage of -1.8 V and zero respectively and incrementally increased to 1.8 V, which is the maximum operating voltage of the technology. The obtained LE response from the VNA was de-embedded using a one port adaptation of the OS technique (Section 2.3.1.1) described in [67] and converted to parallel configuration *RC* values.

The equivalent parallel configuration *RC* values are plotted in Fig. 4.4 at a frequency of 3.6 GHz for various biasing levels. From the measurements, it can be seen that a distinct area is obtained, where the minimum equivalent parallel resistance is approximately 25 Ω and the maximum equivalent parallel resistance is approximately 290 Ω, while the equivalent parallel capacitance range obtained is approximately from 1.7 pF to 4.4 pF.

In this design, a more conservative *RC* range, smaller than the one shown in Fig. 4.4, is used in order to account for process variations, and to ensure the robustness of the design. The capacitance range considered has a minimum value of 2 pF and a maximum of 3.5 pF and the resistance range is from 25 Ω to 150 Ω.

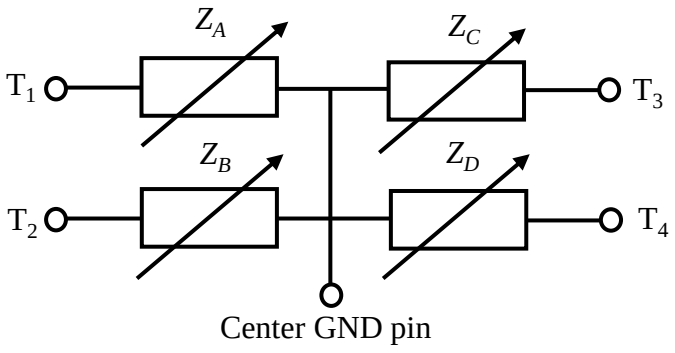


Figure 4.3: Equivalent circuit of the ASIC chip that consists of four MSF LEs

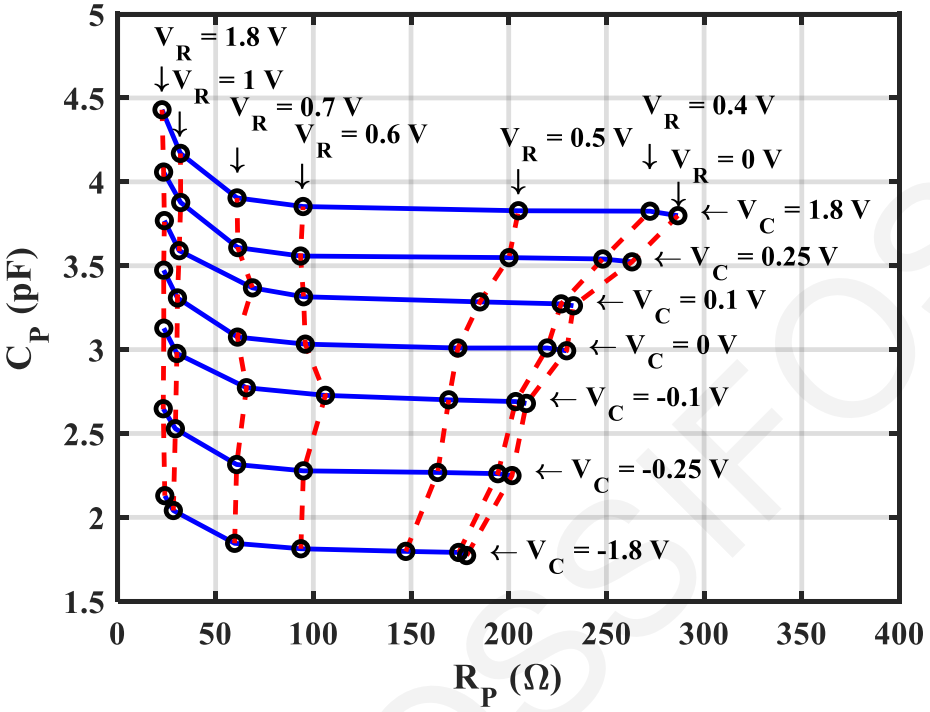


Figure 4.4: Measured parallel *RC* range for the MSF LE at 3.6 GHz.

The finite measured *RC* range from the real chip implementation was entered into a full-wave simulator and the electromagnetic response of the MSF was obtained. The unit cell was simulated using master-slave boundary conditions in ANSYS HFSS in order to obtain the response of the complete MSF. The *RC* values were entered as RLC boundaries in a parallel configuration. The magnitude of the reflection coefficient at the design frequency for various incident angles and for a range of capacitance and resistance values is plotted in Fig. 4.5 and Fig. 4.6 for TM and TE polarizations, respectively.

Here, it is considered that perfect absorption is obtained when the magnitude of the reflection coefficient is less than or equal to -30 dB. This means that for each incident angle, perfect absorption is obtained not only for a singular *RC* load value, but rather for an *RC* area. Within this area, there is one optimum *RC* value that achieves the minimum reflection coefficient. The optimum *RC* values for absorption are R_P = 41 Ω and C_P = 2.7 pF for a normally incident wave for both TM and TE polarizations (Fig. 4.5(a) and Fig. 4.6(a)). As the angle θ increases, the difference for optimum *RC* values between the TM and TE polarizations begins to diverge. For small angles of incidence, an *RC* value could be set on all the loads to obtain perfect absorption. This is the case for an incident angle θ equal to 15° where the

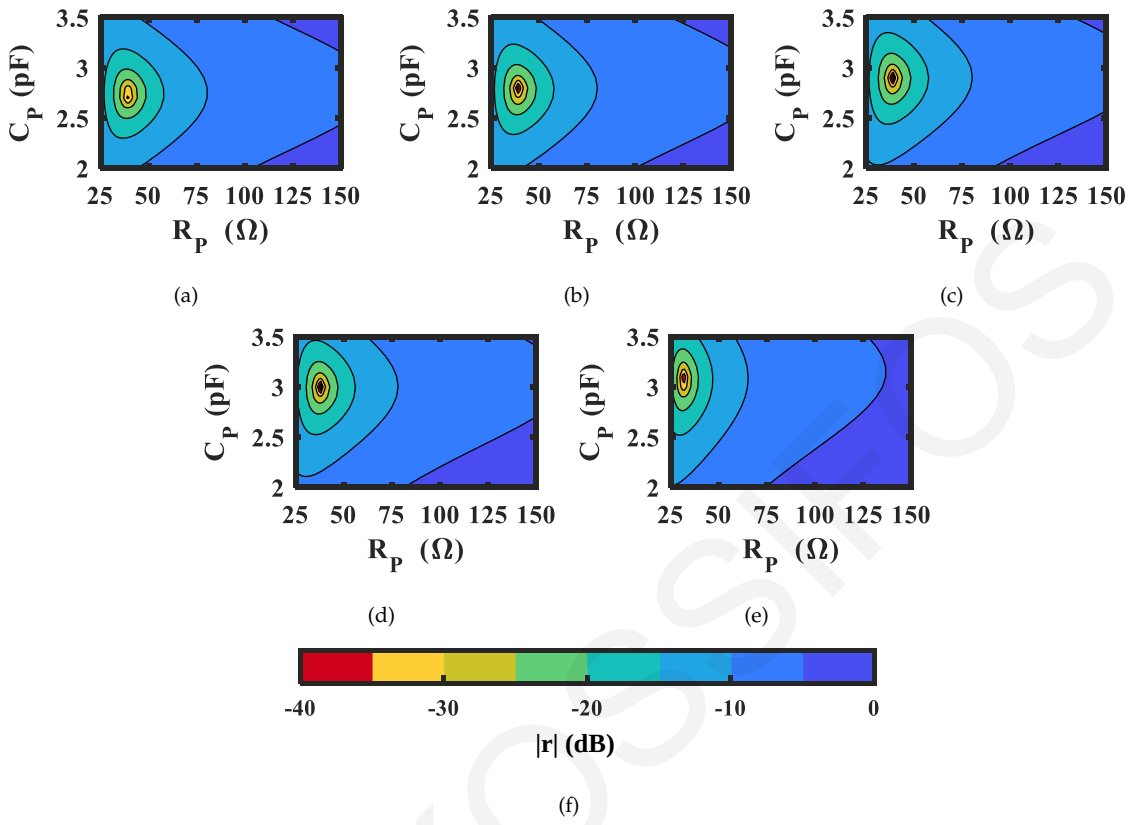


Figure 4.5: Reflection coefficient magnitude in dB for TM polarization and angles of incidence range from $\theta = 0°$ to $60°$. (a) $\theta = 0°$, (b) $\theta = 15°$, (c) $\theta = 30°$, (d) $\theta = 45°$, (e) $\theta = 60°$.

-30 dB area overlaps between TM (Fig. 4.5(b)) and TE (Fig. 4.6(b)) polarizations and a single *RC* combination can achieve a reflection coefficient below -30 dB (e.g. R_P = 41 Ω and C_P = 2.8 pF). For greater angles of incidence, the -30 dB area does not overlap between the TE and TM polarizations, as can be seen for incident angles of $\theta = 30°$ (Fig. 4.5(c) and (Fig. 4.6(c)), $\theta = 45°$ (Fig. 4.5(d) and Fig. 4.6(d)) and $\theta = 60°$ (Fig. 4.5(e) and Fig. 4.6(e)). This means that there is no single *RC* combination that could achieve perfect absorption for both TM and TE polarizations for oblique incidence greater than $\theta = 15°$. Considering the most oblique incidence angle shown in Fig. 4.5 and Fig. 4.6, $\theta = 60°$, in Fig. 4.5(e) one can see that the optimum *RC* values for TM polarization are R_P = 32 Ω and C_P = 3.1 pF, and in Fig. 4.6(e) for TE polarization the optimum *RC* values are R_P = 82 Ω and C_P = 3.3 pF. If the MSF LEs could not be individually controlled through the integrated circuit electronics and had to be controlled from a global voltage across the entire array, then they would have to have a common *RC* value. In this case, if the common *RC* values were to be set for the TM polarization in all four loads, this will only achieve a reflection coefficient that is not less than -10 dB for TE polarization (Fig. 4.7(a)). Similarly, if

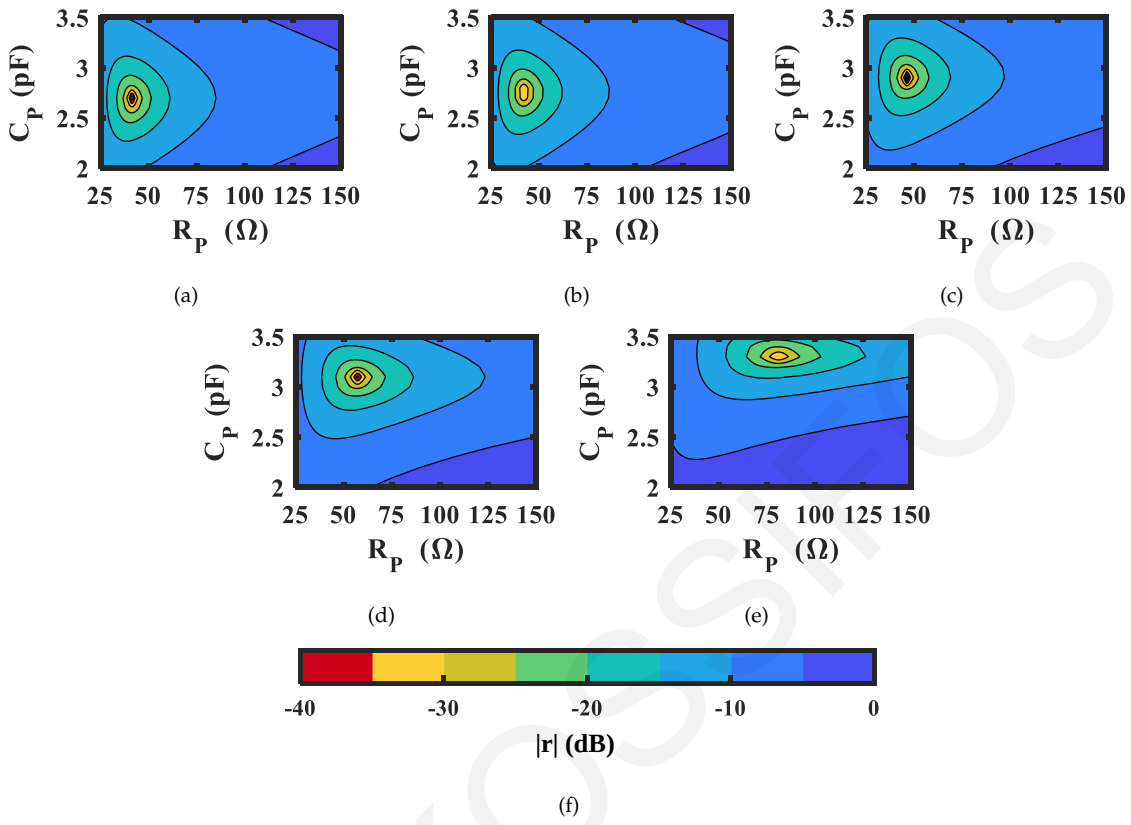


Figure 4.6: Reflection coefficient magnitude in dB for TE polarization and angles of incidence range from $\theta = 0°$ to $60°$. (a) $\theta = 0°$, (b) $\theta = 15°$, (c) $\theta = 30°$, (d) $\theta = 45°$, (e) $\theta = 60°$.

the common RC values were to be set for TE polarization, the TM absorption will suffer and only achieve a reflection coefficient no more than -10 dB (Fig. 4.7(b)).

Considering Fig. 4.2 and Fig. 4.3, one can observe that a TE polarized incident wave with an incident angle θ, which has an electric field only along the y direction, will only generate a potential difference between T_1 and T_3. This means that for TE polarization loads, Z_A and Z_C are not acting upon the MSF since there is no potential difference between them and Z_A and Z_C are only effectively active. In Fig. 4.8, the surface current density is plotted on the top conductors of the MSF, and on the bottom conductors that connect to the ASIC (at the centre of the plots). Fig. 4.8(a), the unit cell is excited with a TE polarized wave at an incident angle θ of 60°. It can be seen in that the highest currents (depicted in red colour) are at the centre of the plot on the bottom conductors that connect to the ASIC in the y direction, and the ones in the x direction are in green color, meaning there is very little current flowing in the x direction. This indicates that for the TE polarization, only the loads Z_A and Z_C are acting upon the MSF surface impedance. Similarly, a TM polarized incident wave which has an electric field only in the x direction, will cause a potential difference

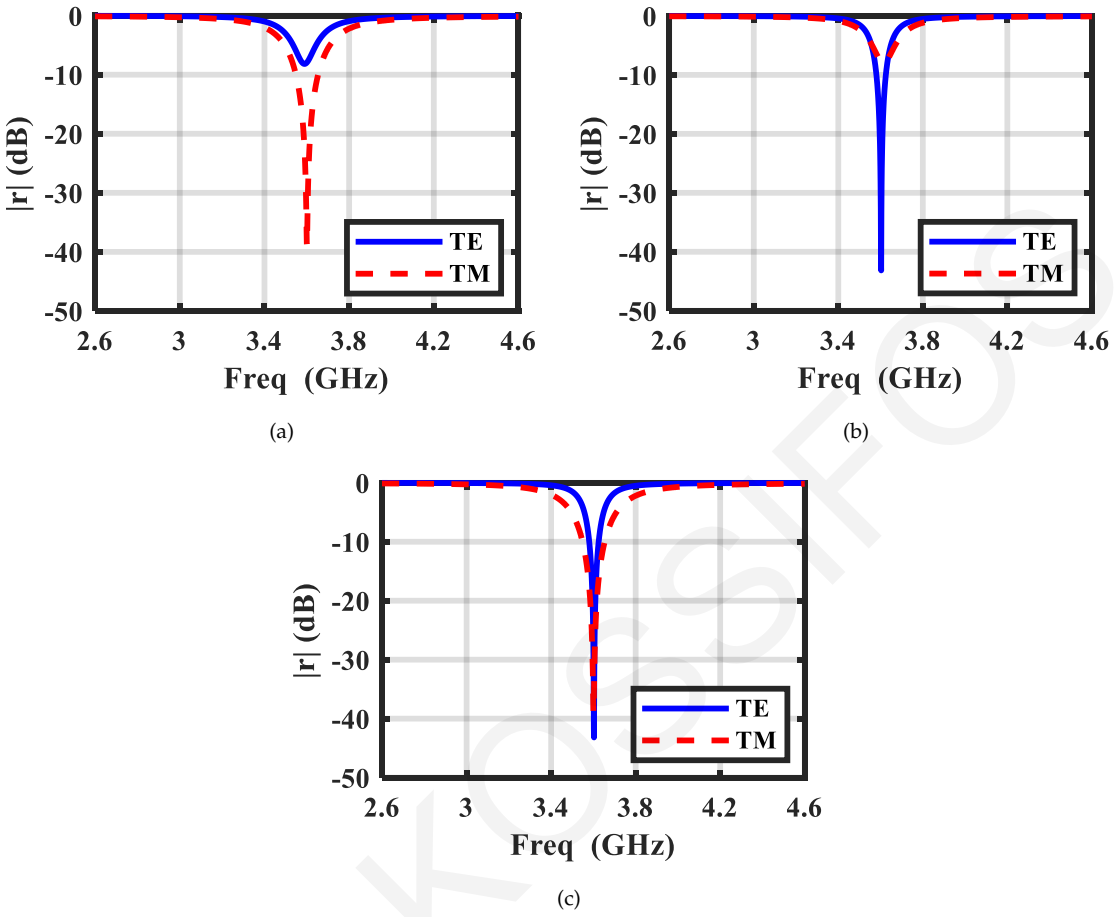


Figure 4.7: Reflection coefficient magnitude for $\theta = 60°$. In (a) all loads are in tuned for TM polarized absorption Z_A, Z_B, Z_C and Z_D *RC* values $R_P = 32\ \Omega$ and $C_P = 3.1$ pF. In (b) all loads are tuned for TE polarized absorption Z_A, Z_B, Z_C and Z_D *RC* values $R_P = 82\ \Omega$ and $C_P = 3.3$ pF and (c) *RC* values for Z_B and Z_D are tuned for TM polarized absorption ($R_P = 32\ \Omega$ and $C_P = 3.1$ pF) and *RC* values for Z_A and Z_C are TE polarized absorption ($R_P = 82\ \Omega$ and $C_P = 3.3$ pF). (*RC* values are in parallel connection)

between T_2 and T_4. In this case, only Z_B and Z_D effectively act upon the MSF surface impedance. In Fig. 4.8(b), the unit cell is excited with a TM polarized wave at an incident angle θ of 60°. In this case, the strong currents are in the x direction at the centre of the plot. An incident wave which has electric field components in both the x and y directions, such as the off-axis linearly polarized case of Fig. 4.8(c), the circularly polarized case of Fig. 4.8(d) or even elliptically polarized cases, can be vectorially decomposed into their x and y components, and the loads on the x (Z_B and Z_D) and y (Z_A and Z_C) axes can be tuned individually in order to obtain perfect absorption for both polarizations. The great advantage of having multiple, independently controlled LEs in a single ASIC is that the bias for each LE can be optimized independently so as to maximize absorption for both the TE and TM polarizations simultaneously. Furthermore, if one were to try to get this kind of

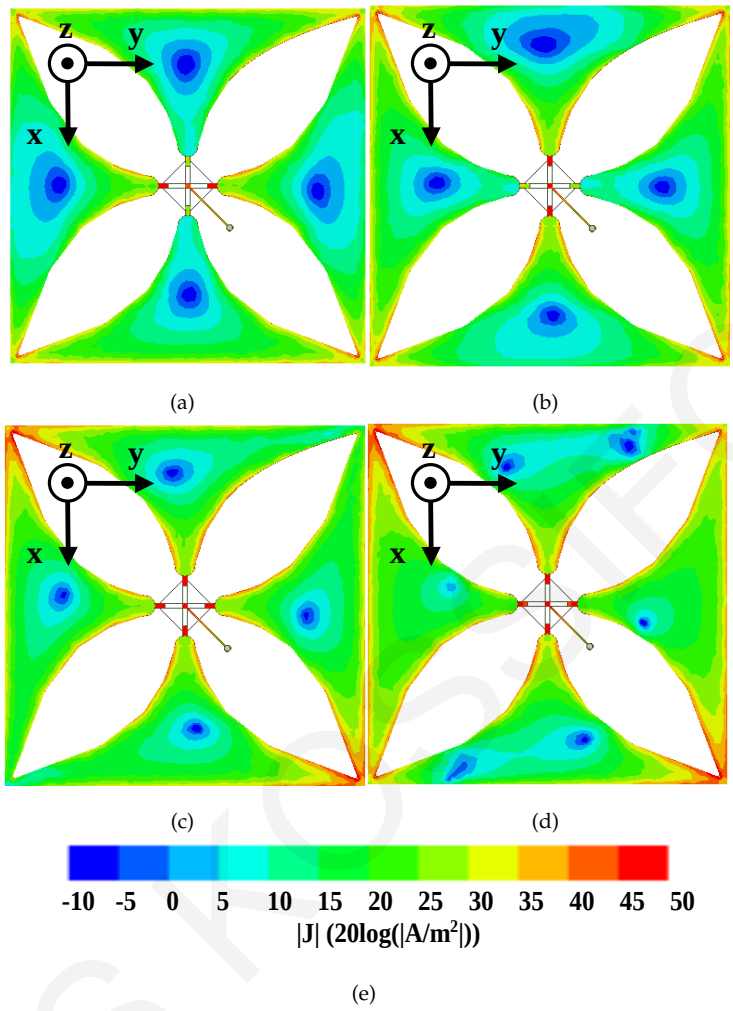


Figure 4.8: Surface current density magnitude for $\theta = 60°$. In (a) the incident wave is TE polarized and the *RC* values for all loads are set for TE absorption, Z_A , Z_B, Z_C and Z_D *RC* values are R_P = 82 Ω and C_P= 3.3 pF. In (b) the incident wave is TM polarized and the *RC* values are set for all loads for TM absorption, Z_A, Z_B, Z_C and Z_D *RC* values are R_P = 32 Ω and C_P= 3.1 pF. In (c) the unit cell is excited with a linear polarization (|TE|=|TM|, ∠TE-∠TM=0°). In (d) the unit cell is excited with a circular polarization (|TE|=|TM|, ∠TE-∠TM=90°). For both (c) and (d) *RC* values for Z_B and Z_D are tuned for TM polarized absorption (R_P = 32 Ω and C_P = 3.1 pF) and *RC* values for Z_A and Z_C are tuned for TE polarized absorption (R_P = 82 Ω and C_P = 3.3 pF). (*RC* values are in parallel connection)

controllability with discrete, commercially-available off-the-shelf components, their large size would be prohibitive, and there would be significantly higher parasitics involved with multiple packages. In Fig. 4.8(c) the unit cell is excited with an incident wave that is linearly polarized, while in Fig. 4.8(d) it is circularly polarized. Optimal *RC* values for TM polarization are set to Z_B and Z_D, and the optimal *RC* values for TE polarization are set to Z_A and Z_C. It can be seen that in both cases the surface currents are stronger at the ASIC connection, indicating that the electromagnetic wave is dissipated on the ASIC's LEs. In Fig. 4.7(c), the magnitude of the reflection

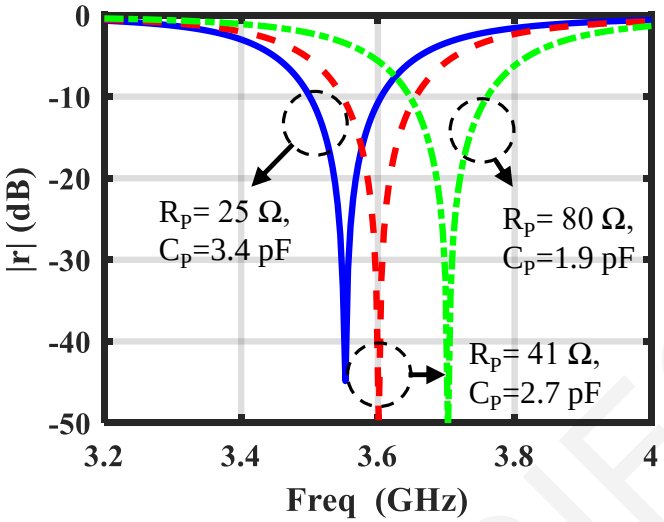


Figure 4.9: Reflection coefficient magnitude for TE polarization at normal angle of incidence ($\theta = 0°$) for optimal loading element combinations, demonstrating frequency-tunable perfect absorption.

coefficient is plotted for an incident angle θ of 60°. Optimal RC values for TM are set to Z_B and Z_D, and the optimal RC values for TE are set to Z_A and Z_C. Both TM and TE polarizations are absorbed perfectly at the design frequency, regardless of the phase and magnitude difference between them.

Even though this particular design aims to implement an adaptive MSF absorber at a single frequency (3.6 GHz), it is also worth mentioning its frequency-tunability capabilities. In Fig. 4.9 the reflection coefficient is plotted for TE polarization at a normal angle of incidence. It can be seen that the MSF exhibits perfect absorption over a range of frequencies around 3.6 GHz by adjusting both the resistance and capacitance values of all the loads within the measured achieved range, as shown in the labels of Fig. 4.9.

The absorption of a wave that contains electric fields in both the x and y directions is the more common case if an MSF were to be installed within a realistic scenario where the MSF is not aligned to the wave source. The flexibility to adjust the absorption of both orthogonal electric fields independently is a key feature for tunable MSF absorbers where the direction and polarization of the incident wave changes in time. A key enabler of this feature is the custom integrated circuit with tunable MSF loading elements, giving the ability to provide a tunable complex impedance, within a much smaller area than any commercially-available off-the-shelf components. Furthermore, there is no need for the use of distributed high impedance nodes that take up valuable space on a PCB, such as radial stubs and

quarter wavelength lines.

4.3 Multibeam Synthesis

The functionality shown so far of the MSF design shown in Fig. 4.1 was global, meaning that all the unit cells were controlled in the same manner. The ASIC in terms of RF operation for non-global operation still uses four LEs that forms a double T network between four terminals (T_1-T_4), as shown in the inset figure of Fig. 4.2(b). The equivalent circuit of the ASIC can also be seen in Fig. 4.2(b). This equivalent circuit possesses a complex impedance which effectively loads the unit cell, and thus alters it surface impedance [22].

In the previous section, it was shown that by loading the unit cell with an appropriate complex impedance one can match the surface impedance to the propagating wave impedance, and thus obtain perfect absorption. This was shown to be obtained for TE and TM polarizations for wide angles of incidence. Furthermore the absorption of TE and TM polarised waves can be controlled simultaneously or independently [22].

Within the finite complex impedance area that can be achieved by the ASIC,

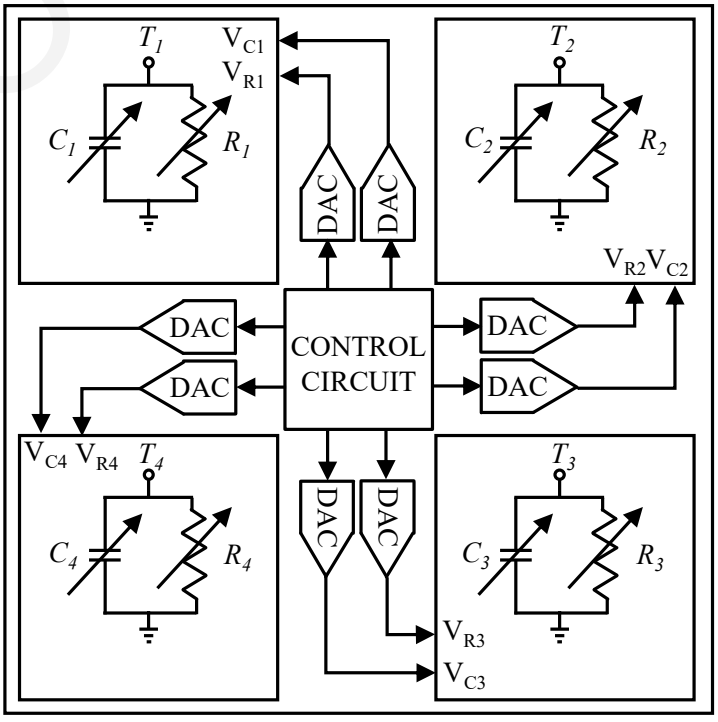
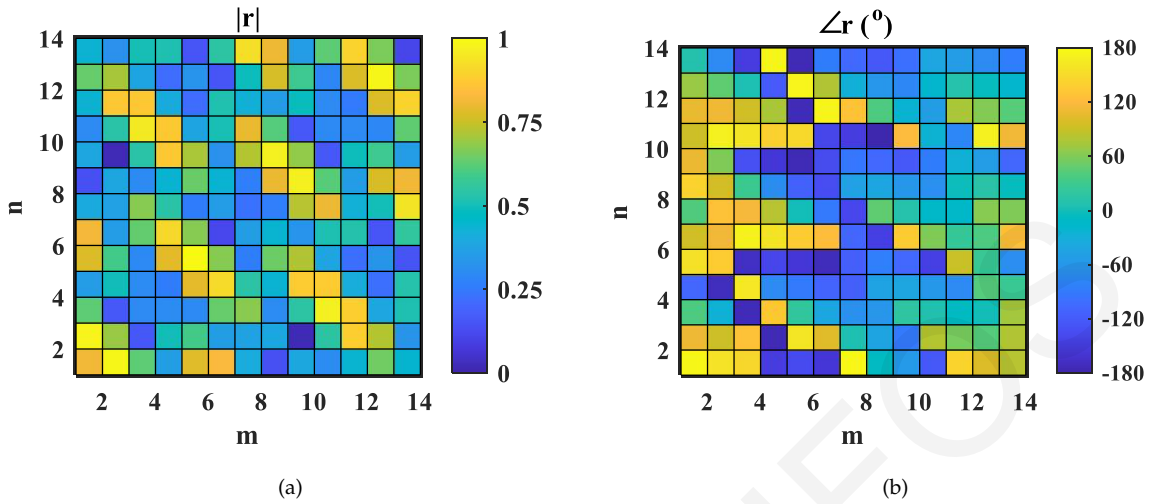


Figure 4.10: Top-level diagram of the ASIC, showing the four varactors and the four varistors that load the MSF, the eight DAC, and the communication control circuit.



(a) (b)

Figure 4.11: (a) Magnitude, and (b) phase of the calculated reflection coefficients required to generate three pencil beams.

other specific points that do not match the propagating wave impedance for a given angle of incidence and polarization will reflect a portion of the incident wave with a finite amplitude and phase. This is particularly useful, since this provides control of both the amplitude and phase for each unit cell.

Amplitude and phase control would be particularly useful for not only absorption applications but also for synthesis applications. Synthesis of a reflected wavefront would entail that control of each unit cell can be performed. This is a non-global operation where each unit cell needs to be programmed in a different manner. As will be shown later in this chapter, by incorporating DAC and a control circuits within the IC, such synthesis functions can be performed.

4.3.1 Single Polarization Wavefront Synthesis

Let's consider a MSF design consisting of 14×14 unit cells, as can be seen in Fig. 4.1. The details of the individual unit cell can be seen in Fig. 4.3. The ASIC consists of four programmable varistors and varactors [22]. A varistor and a varactor is connected to each one of the four terminals (T_1 to T_4) and a centre common terminal that connects to the ground. Within the ASIC, additional eight DAC and an asynchronous control circuit [96] can be integrated to achieve individual unit cell programmability. The top level diagram of the ASIC can be seen in Fig. 4.10 [107].

Taking advantage of the ability to control amplitude and phase, one can utilize the addition theorem [16] to calculate the reflection coefficient of each unit cell for

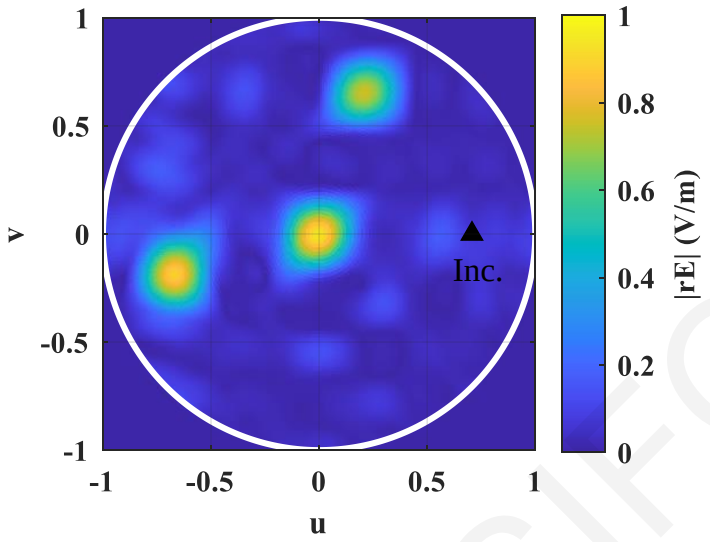


Figure 4.12: Normalized reflected electric field over the *uv* coordinates. The reflection coefficients shown in Fig. 4.11 were implemented and the incident wave direction is indicated with a black triangle.

a MSF consisting of M×N = 14×14 unit cells. The calculated normalized reflection coefficients that are required in order to generate a more complex wavefront, for example three pencil beams. The reflection coefficient amplitude and phase are plotted in Fig. 4.11. The MSF was designed in ANSYS HFSS, and was excited with a plane wave at 3.6 GHz. The MSF was loaded with the appropriate complex impedances for each unit cell, which were realized using one of the 2^{16} discrete LE's states.

The obtained reflected electric field can be seen in Fig. 4.12, plotted in the *uv*-coordinates. The *uv* coordinate variables are related to the spherical coordinate variables θ and ϕ as follows:

$$u = sin\ \theta\ cos\ \phi,\ v = sin\ \theta\ sin\ \phi. \tag{4.1}$$

The incident plane wave is marked with a black triangle in Fig. 4.12, and the three resultant pencil beams are clearly indicated by the high-intensity yellow dots. Polar plots of the results shown in Fig. 4.12 are also plotted in Fig. 4.13(a) and Fig. 4.13(b) for the $\phi = 18°$ and $\phi = 72°$ cuts, respectively. Between the two latter figures, the three pencil beams can be clearly seen. A single pencil beam and even more than three pencil beams can be realized in a similar manner with the presented design.

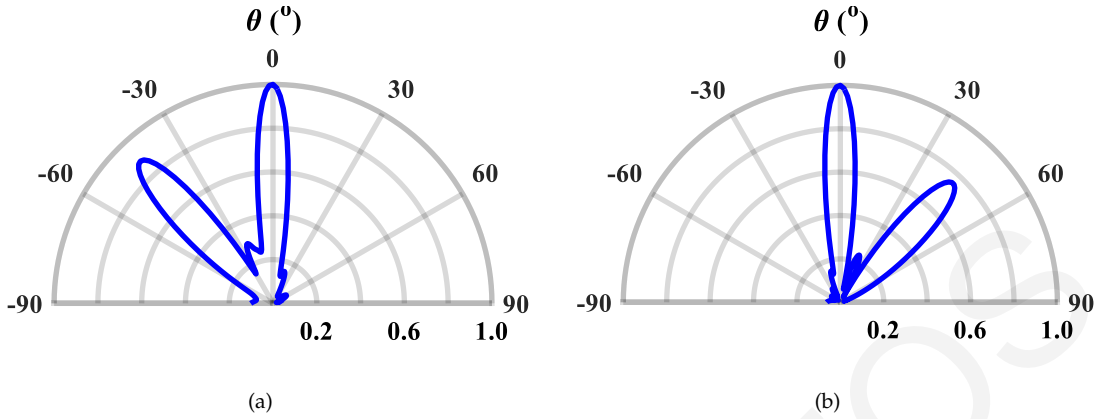


Figure 4.13: Polar plots of the electric field (V/m), for (a) $\phi = 18°$, and (b) for $\phi = 72°$.

4.3.2 Dual Polarization Wavefront Synthesis

The multibeam capabilities of the design can be extended to programtically load the unit cell in an anisotropic manner in order to control the TE and TM polarizations independently. In this way, polarization diversity of the MSF design reported in [22] can be demonstrated. The design was shown to be able to produce multiple pencil beam patterns [45]. Four pencil beams at 3.6 GHz are generated utilizing the addition theorem [16]. The polarization state of each pencil beam is demonstrated to switch between LP, CP and even elliptic polarization (EP).

The reflection coefficient can be expressed as a 2×2 matrix for both TE and TM polarizations:

$$r = \begin{bmatrix} r_{xx} & r_{xy} \\ r_{yx} & r_{yy} \end{bmatrix}. \tag{4.2}$$

The loading varactors and varistors that are connected on terminal T_1 and T_3 are placed in the y-axis direction (see Fig. 4.2(b)). By controlling the resistance and capacitance values of these elements (R_1 and C_1 for T_1, R_3 and C_3 for T_3) one can control the reflected amplitude and phase of the TE polarization (r_{yy}). Similarly, the resistance and capacitance values of the varactors and varistor connected to T_2 (R_2 and C2) and T_4 (R_4 and C_4) are connected on the x-axis direction. This gives them control of the reflected amplitude and phase of the TM polarization (r_{xx}). Furthermore, since the TE and TM polarizations are orthogonal to each other, the varactor and varistor values on T_1 and T_3 will not affect the TM polarization control and similarly the varactor and varistor values on T_2 and T_4 will not affect the TE polarization control. This ability was exploited in [22] to perfectly absorb an incident wave which contained both TE and TM polarization components.

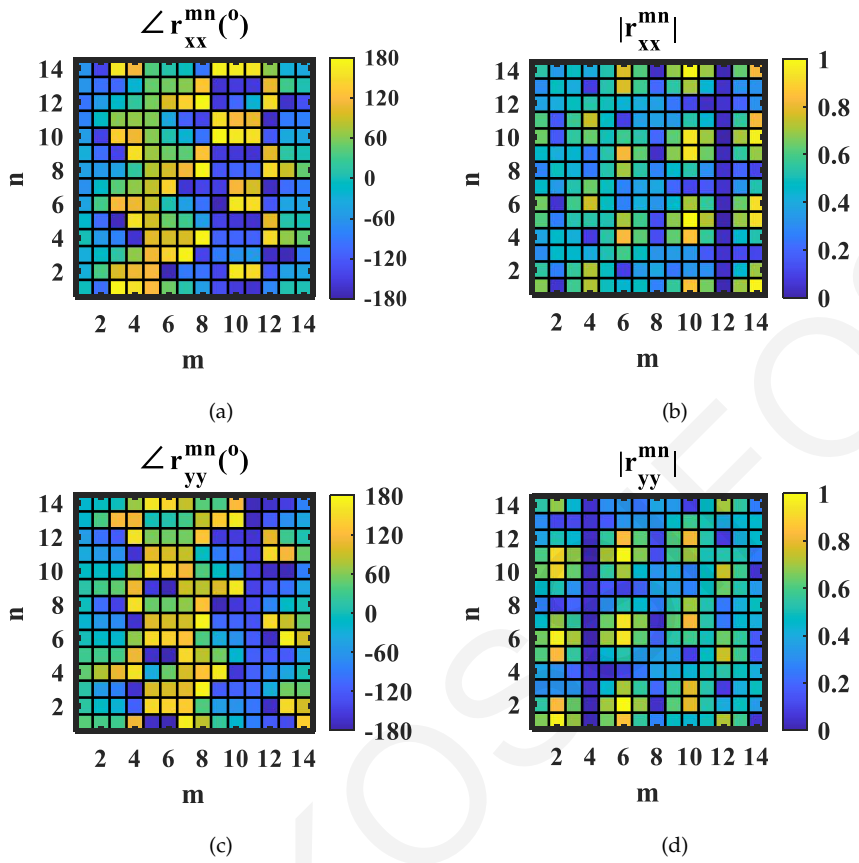


Figure 4.14: Calculated reflection coefficients for r_{xx} and r_{yy}, (a) $\angle r_{xx}$, (b) $|r_{xx}|$, (c) $\angle r_{yy}$ and (d) $|r_{yy}|$.

Even though the ASIC can address each varactor and varistor independently, in this work it is considered that the resistance and the capacitance values of the varistor and the varactor that are connected to T_1 and T_3 are equal. Similarly, the resistance and the capacitance values of the varistor and the varactor that are connected to T_2 and T_4 are also considered equal.

The reflection coefficients that produce a pattern with four pencil beams were calculated using the addition theorem [16]. In order to set the polarization state for each pencil beam, their orthogonal components are phase shifted, as described in [89]. In order to demonstrate the capabilities of this MSF design, one pencil beam was set to be right-hand circular polarization (RHCP), one to be left-hand circular polarization (LHCP) and the other two to be linearly polarized. The calculated reflection coefficients are plotted in Fig. 4.14. In Fig. 4.14(a) and Fig. 4.14(b) the angle and magnitude of r_{xx}, respectively, are plotted, and in Fig. 4.14(c) and Fig. 4.14(d) the angle and magnitude of r_{yy}, respectively are plotted. Here, n and m are the index in the x and y-directions, respectively.

By relating the reflection coefficient to a varistor and varactor values (RC values),

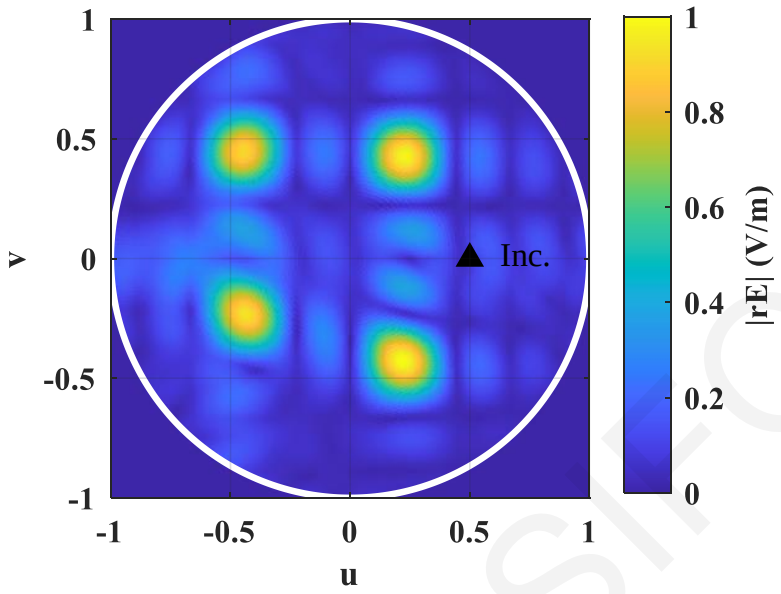


Figure 4.15: Normalized total reflected electric field (V/m) produced by the MSF when implementing the reflection coefficients shown in Fig. 4.14. The incident wave direction is indicated with a black triangle.

the reflection coefficient distribution takes a physical form. A Visual Basic script was utilized to implement the MSF in ANSYS HFSS with the appropriate loading values. The MSF was excited with a plane wave at 3.6 GHz.The obtained reflected electric field can be seen in Fig. 4.15, plotted in the *uv* coordinates. The incident plane wave direction is marked with a black triangle in Fig. 4.15. The four pencil beams can be clearly seen with bright yellow color over the blue background.

In Fig. 4.16 the results of Fig. 4.15 are plotted in more detail. In Fig. 4.16(a) a 3D plot of the total electric field is plotted and the polarization of each beam is indicated. The four beams are plotted in $\phi = 27°$ (Fig. 4.16(b)), $\phi = 63°$ (Fig. 4.16(c)), $\phi = 117°$ (Fig. 4.16(d)) and $\phi = 135°$ (Fig. 4.16(e)) on polar plots. Two LP pencil beams are shown ($\phi = 27°$, $\phi = 63°$), together with two CP pencil beams (RHCP $\phi = 117°$, LHCP $\phi = 135°$), where in both cases the axial ratio is near unity as expected. All polar plots in Fig. 4.16 are overlaid with the calculated reflected electric field and are in good agreement.

4.3.3 Orbital Angular Momentum Beam Synthesis

Beams with orbital angular momentum (OAM) were also generated by MSF designs [18,112]. OAM beams are an attractive solution in telecommunication systems

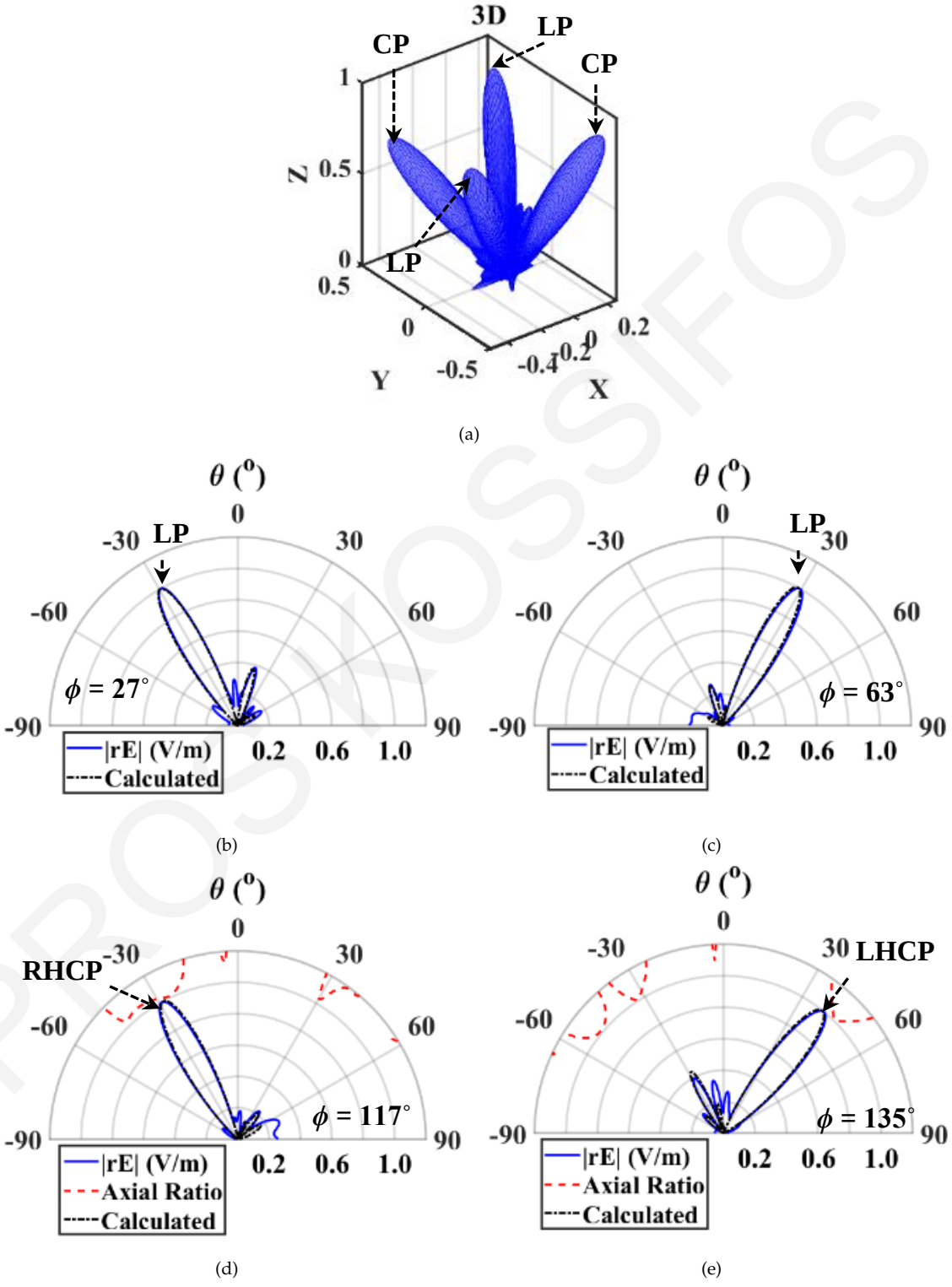


Figure 4.16: (a) 3D plot of the electric field (V/m) shown in Fig. 4.15, and four polar plots of the electric field, one for each pencil beam (b)-(e). (b) $\phi = 27°$, (c) $\phi = 63°$, (d) $\phi = 117°$ and (e) $\phi = 135°$. The polarization of each pencil beam is indicated on each polar plot and in the 3D view in (a). On the circularly polarized pencil beams in (d) and (e), the axial ratio is overlaid.

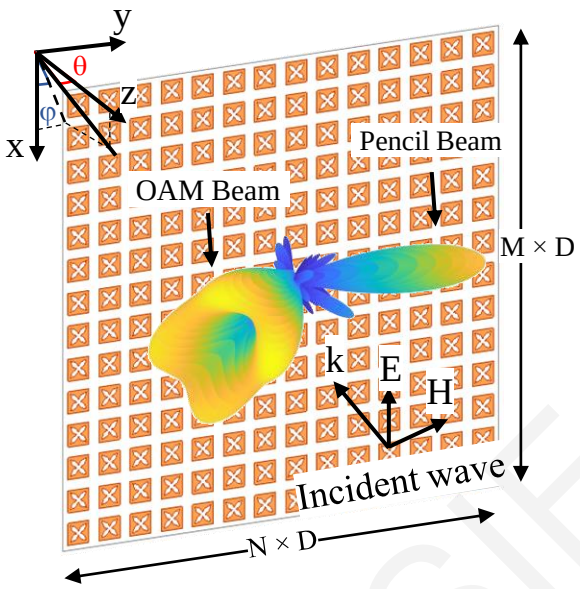


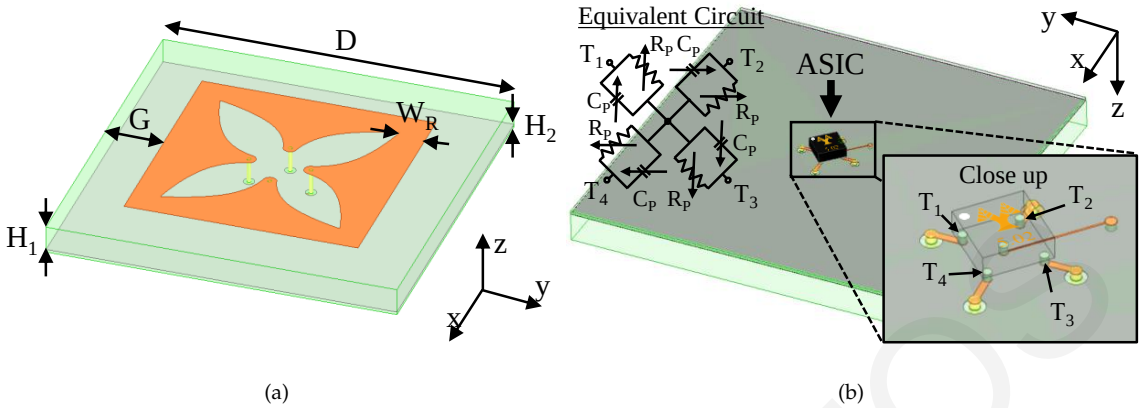
Figure 4.17: Proposed MSF design consisting of 14×14 unit cells, modified to operate at 4.1 GHz.

since they can be spectrally efficient and possess anti-jamming capabilities. For this reason, the author chose to demonstrate the MSF design in producing such beams.

In this section, the advanced capabilities of a MSF design reported in [22,45] are demonstrated. In the previous sections, the design was shown to be able to perfectly absorb incident waves [22] and to produce multiple pencil beam patterns [45]. In this section, the design was adapted to operate at 4.1 GHz, and programmed to generate a complex pattern consisting of a pencil beam and an OAM beam. The proposed MSF design can be utilized in MSF-assisted indoor and outdoor telecommunication systems.

The proposed MSF design can be seen in Fig. 4.17. The design consists of 14×14 unit cells. The unit cell geometry can be seen in Fig. 4.18, and it has been described in [22,45], where its perfect absorption and multibeam generation capabilities were demonstrated. The top side of the unit cell can be seen in Fig. 4.18(a). The bottom side of the unit cell can be seen in Fig. 4.18(b), where the integrated circuit is located. The ASIC loads the MSF with four parallel resistors and capacitors (RC) at the four terminals T_1 to T_4. The equivalent circuit of the ASIC can also be seen in the insert of Fig. 4.18(b). Small variation in the geometry of the unit cell were done and a different substrate is used in the design as it was available at the time. The specific geometric parameters used in this simulation can be found in Table 4.2. The substrate used was Megtron 6 by Panasonic.

The unit cell was simulated in periodic boundary conditions to correlate the



(a) (b)

Figure 4.18: MSF unit cell geometry, (a) top view, and (b) bottom view showing the ASIC and its equivalent circuit.

RC values to the reflection amplitude and phase responses at the design frequency of 4.1 GHz. The reflection coefficient to produce the complex reflected pattern overlaid in Fig. 4.17 were calculated using [16, 18, 112]. The amplitude and phase of the calculated reflection coefficients can be seen in Fig. 4.19(a) and Fig. 4.19(b), respectively for all the unit cell.

Here, n and m are the index in the x and y-directions, respectively. The correlated resistance and capacitance values can be seen in Fig. 4.19(c) and Fig. 4.19(d), respectively.

A Visual Basic script was implemented to create the MSF in ANSYS HFSS with the correlated *RC* values. The MSF was illuminated using a plane wave excitation with the polarization shown in Fig. 4.17. The simulated total scattered field can be found in Fig. 4.20 plotted over the uv-coordinates. The results clearly show a pencil beam and an OAM beam at the desired direction.

The ASICs' accuracy in providing the set *RC* response in each LE was not addressed in the previous sections. Some error is expected in the *RC* values and some variability between ASICs' responses. Furthermore, even in the same ASIC

Table 4.2: Unit cell's geometry parameters adopted for operation at 4.1 GHz.

Geometric Parameter	Dimension (mm)	Description
H_1	1.82	Top Substrate Thickness
H_2	0.2	Bottom Substrate Thickness
D	25.5	Period of the Unit Cell
W_R	20.0	Rectangular Ring Width

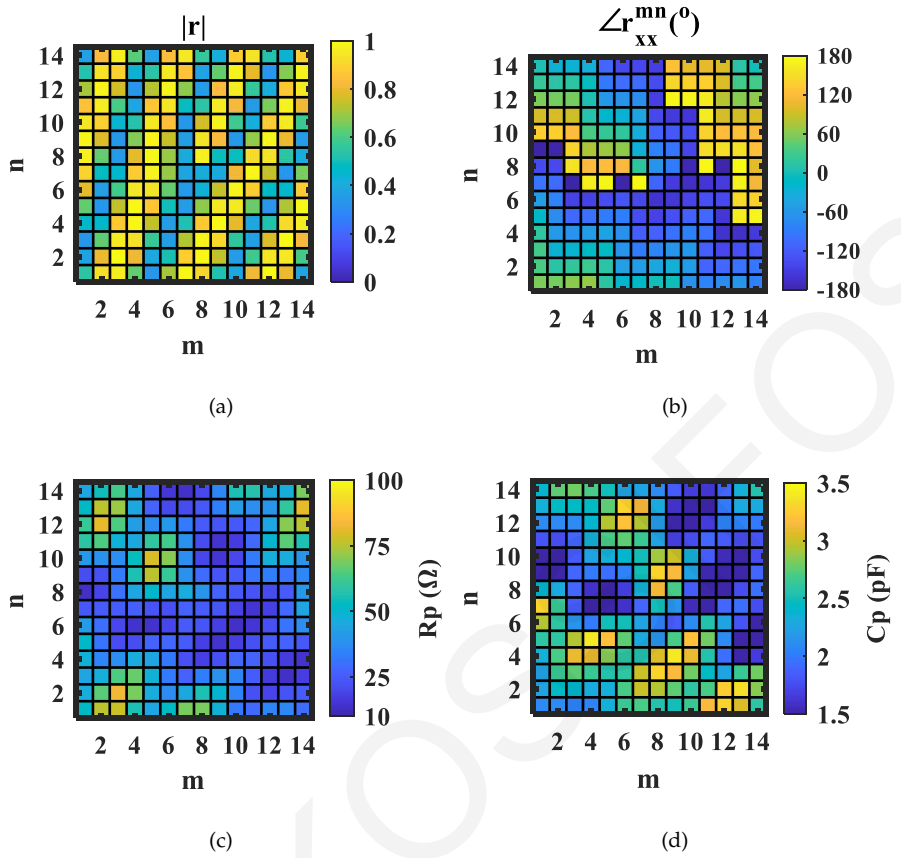


Figure 4.19: Calculated reflection coefficient, (a) amplitude and (b) phase. Correlated (c) resistance and (d) capacitance values.

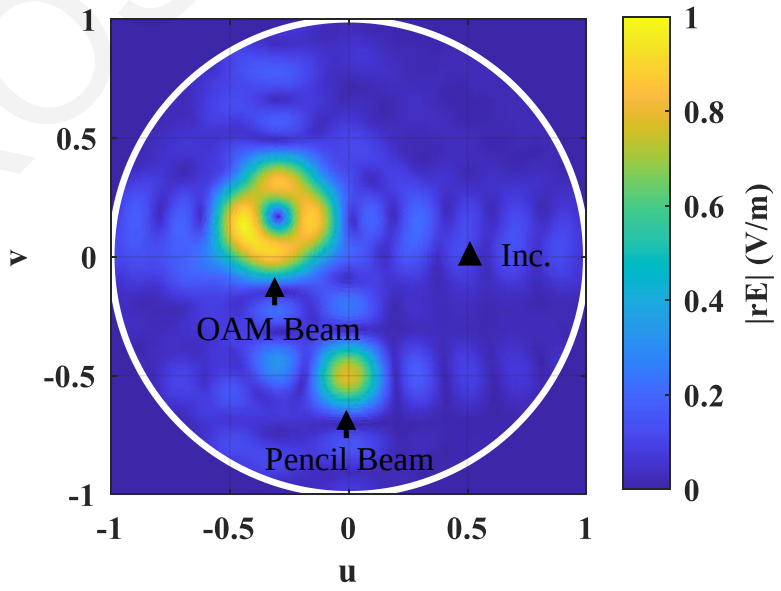


Figure 4.20: Normalized reflected total electric field (V/m) over the *uv*-coordinates. Incident plane wave direction indicated with a black triangle.

some variation between varactors or varistors is expected. This error would arise from a myriad of manufacturing imperfections within each ASIC. A study on these

effects is presented in next section to address these effects on the perfect absorption and wavefront synthesis capabilities of the PMSF.

4.4 ASIC Mismatch Effects

The electronic control of MSFs provided the possibility to control each unit cell individually, without human or user intervention through software. By biasing each unit cell through the outputs of an FPGA and connecting it to a computer, software control was now possible. This simple logical step gave birth to programmable metasurfaces (PMSFs). By controlling each unit cell through software, PMSFs were able to demonstrate multiple reconfigurable functions, such as polarization, scattering and focusing control [32], holography [33,36], non-linear harmonic control [35,113], machine-learning imaging [36], and frequency recognition for self-adaptivity [37].

PMSFs, having demonstrated multiple and reconfigurable electromagnetic manipulation capabilities, now provide the potential to greatly improve wireless telecommunications through the smart radio environment reconfiguration paradigms [38–42], and to increase the capabilities and agility of antenna applications as shown in the previous sections (Section 4.3.1-Section 4.3.3 [43–45]), and [46,47]. These PMSFs can be found in the literature as intelligent reflective surfaces (IRSs), reconfigurable intelligent surfaces (RISs), reconfigurable reflective surfaces (RRSs) and even hypersurfaces. PMSFs in their current state rely on power-hungry and costly FPGAs. The work presented so far in this chapter, aims to reduce the power consumption and cost of PMSFs [22,95,107] while increasing their capabilities. This is achieved with the incorporation of the custom ASIC in all the unit cells. The designs significantly expand the multifunctional properties of the design presented in [92] and use the custom integrated MSF LEs presented in Section 3.3.1 [22] in every ASIC. These PMSF designs presented in this chapter (Chapter 4) and Chapter 3 triggered the development of the first family of custom ASICs which is later presented in the next chapter (Chapter 5) [114]. These ASICs as intended, will incorporate DACs, control circuits and four individually addressed LEs.

In order for PMSFs to be established as a common telecommunication technology, significant steps need to be taken towards their commercialization. Other aspects besides cost and power consumption need to be addressed. The large number of ICs needed for the implementation of PMSF designs [22,43–45,95,107] may be

desired or expected to each have an identical response. Unfortunately, ICs during their manufacturing experience process variations and mismatch that will alter their actual responses from their nominal ones [115, 116]. This is because a process' sequential computer controlled manufacturing steps may not control doping factors, temperature and device dimensional features such as, the line widths that are often comparable to the wavelength of the light used in the lithography process. These are just a few reason among a myriad of reasons why process variations and mismatches occur. Reproducibility in standard IC processes is achieved by taking into account statistical models of the IC's components and making the design tolerant to them [117,118]. These models are obtained by measuring a large number of components in multiple wafer batches in a standard IC process, and by extracting statistical model parameters [119]. The curve for these variations is typically a skewed normal distribution with a standard deviation (σ). Although the effects of process variations and mismatch are present in all devices and both are caused by manufacturing imperfections, there is a distinction between them. Process variations are the wafer-to-wafer variations which will cause the mean value response of a device population to deviate in a wafer batch, while the mismatch is the device-to-device variation within a wafer batch, this will cause the standard deviation of a device population [119]. A process will produce its worst-case scenarios when the tightly computer controlled sequential manufacturing steps for various manufacturing reasons may produce a device that is at the two edges of the normal distribution. The two worst-case scenario models are named *fast* and *slow* models.

Probabilistic models are usually supplied with the PDK for common IC technologies. Unfortunately, this is not the case for the RF/ MW components. RF and MW components are only supplied with fast and slow models and it is common that one can make an RF/MW design still operate even with these two extreme cases by using various biasing or tuning and compensation techniques [120, 121], but in the case of PMSF designs where the IC numbers are relatively large this might be impractical. Process variations can be compensated at a global scale when the size of the PMSF can be populated with ICs from the same batch. Mismatch on the other hand, would be hard to compensate without the use of a computer-aided heuristic approach. Furthermore, the mismatch effects on the far field response of a PMSF remain unknown.

This section studies the effect on the scattered far field of an IC-equipped PMSF

design which is subjected to different degrees of mismatch variations. In this study, a standard deviation of 10% to 40% of the component values of the LEs of the IC is applied.

4.4.1 Mismatch Metasurface Simulation

The proposed PMSF design in this chapter, can be programmed to control the reflection coefficient (magnitude and phase) of each unit cell for both TE and TM polarizations. This is achieved by simply changing the capacitance and resistance values of each varactor (C_1 to C_4) and varistor (R_1 to R_4). This can be exploited to demonstrated the perfect absorbance of complex polarization incident waves for a wide angle range as shown in Section 4.2 [22], and even the generation of complex wavefronts Section 4.3 [43–45]. The results presented in this chapter so far were ideal, meaning that they consider that all the ICs are identical [22, 43–45]. This scenario is not realistic, since some variability due to process variations and mismatch is expected between ICs and even between different LEs within the same IC. This variation is expected to follow a normal distribution with a mean value and a standard deviation (σ). Unfortunately, for RF/MW components these statistical models are not supplied by the foundries with their PDK.

This lack of statistical models leaves modern PMSF engineers to face this challenge. One can address this by producing the models, but the post-packaging characterization of a large number of ICs to produce the statistical model will be a cumbersome and costly process. This process will also be subjected to the variability of connectors, to PCB calibration standard errors and de-embedding errors. Furthermore, even when obtaining the statistical models, a large number of PMSF simulations with such expected standard deviation of the component values will require a large amount of computational resources and time to complete.

In this section, such scenarios of an IC-equipped PMSF design that is subjected to mismatch are simulated. The PMSF is simulated in ANSYS HFSS, where the PMSF is created with custom Visual Basic scripts [22,43–45]. The LEs are implemented using RLC boundary sheets and the PMSF is illuminated by a plane wave at $\theta = 30^\circ$ and $\phi = 0^\circ$, whose electric field contains θ and ϕ polarization components, both equal to 1 $^V/_m$. The size of the PMSF is kept at a 14×14 unit cells, which is the maximum size that can be simulated with the available resources.

4.4.1.1 Perfect Absorbance Case

In this section, the case where the PMSF is set to perfectly absorb an incident wave is studied. The incident wave contains both TM and TE components. Since the incident wave's angle is $\theta = 30°, \phi = 0°$ the TM component is the x-polarized component, and it will be programmed for absorption by the tunable elements located along the x-axis, the RC elements R_1, C_1 and R_3, C_3 [22]. Their RC values are 1.9 pF and 40 Ω. The TE component, which in this case is the y-polarized component will be programmed for absorption by the RC elements R_2, C_2 and R_4, C_4 which will have the RC values of 2 pF and 44 Ω.

These RC values are nominal values which realistically are not provided by all the ICs while having the same state. A normal distribution around these nominal RC is applied for the PMSF simulations to emulate the mismatch effects. A standard

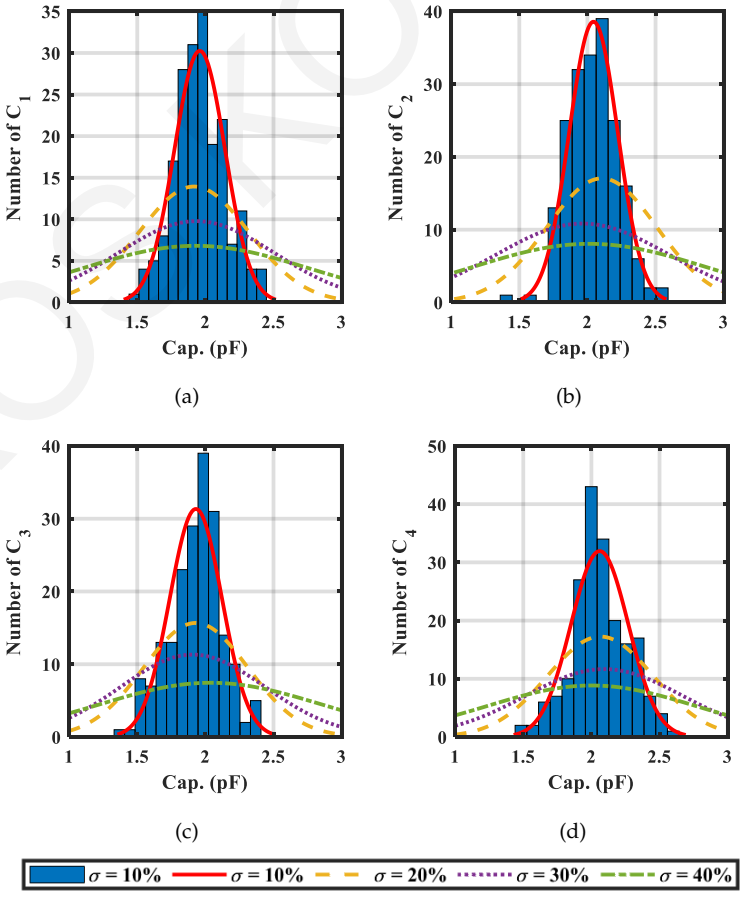


Figure 4.21: Capacitance values for the 14×14 unit cell PMSF. All plots contain a histogram for the population of capacitances for a standard deviation, σ, of 10% of their nominal values, and fitted curves for the populations for 10%, 20% ,30% and 40% standard deviation. (a) C_1, (b) C_2, (c) C_3, (d) C_4 and in (e) the legend is shown.

deviation, σ, of 10% to 40% of the nominal RC values is considered.

The distribution of the capacitance of the LEs is shown in Fig. 4.21, while the distribution of the resistance of the LEs is shown in Fig. 4.22. In all distributions of the capacitances (C_1 *to* C_4 in Fig. 4.21(a) to Fig. 4.21(d)) and the resistances (R_1 *to* R_4 in Fig. 4.22(a) to Fig. 4.22(d)) a histogram showing the population of capacitance or resistance values is plotted for σ = 10%. This population is generated with the "normrnd" function and curve fitted with the "fitdist" function in MATLAB™. On the same plots, curve fitted distributions for the generated RC populations for σ = 20%, 30% and 40% are plotted.

The simulated scattered total electric field results ($E_{Tot.}$) of the PMSF can be seen in Fig. 4.23 plotted over the uv coordinates. In Fig. 4.23(a) the ideal scenario where all the ICs have the nominal RC values is plotted (σ = 0%). In this scenario, all the

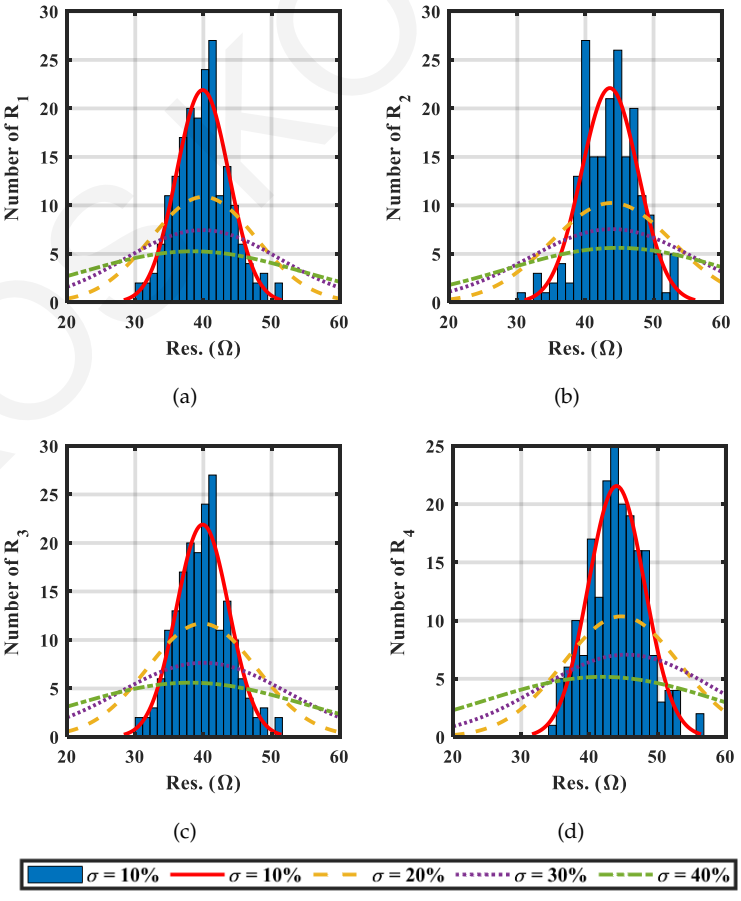


Figure 4.22: Resistance values for the 14×14 unit cell PMSF. All plots contain a histogram for the population of resistances for a standard deviation, σ, of 10% of their nominal values and fitted curves for the populations for 10%, 20%, 30% and 40% standard deviation. (a) R_1, (b) R_2, (c) R_3, (d) R_4 and in (e) the legend is shown.

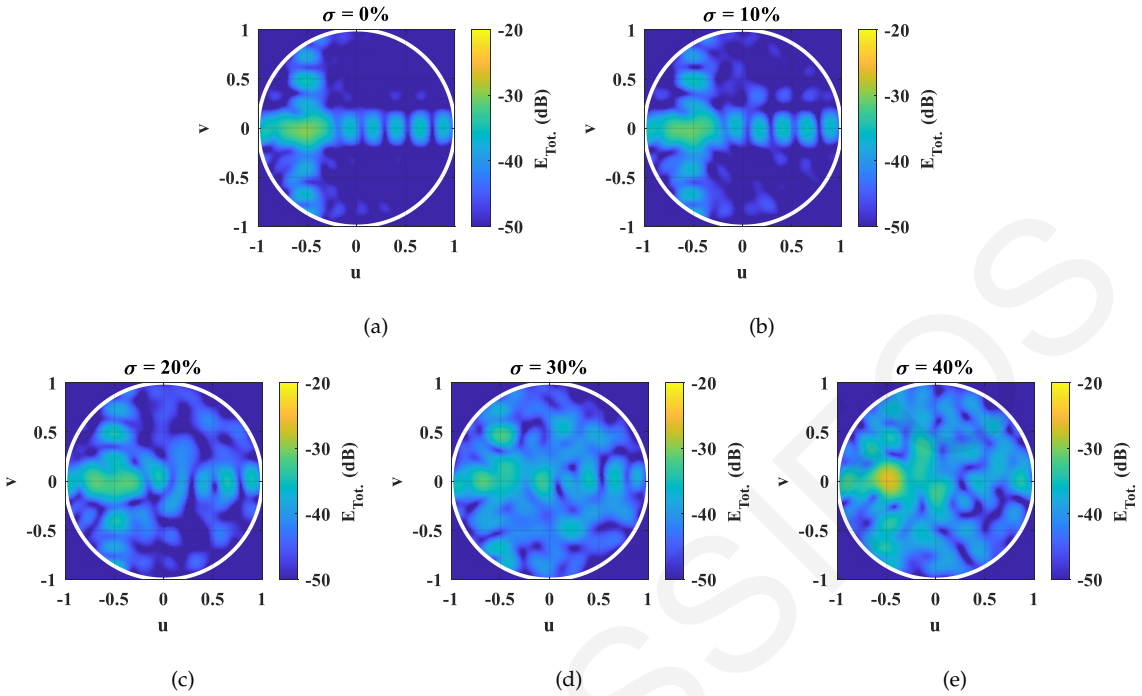


Figure 4.23: Scattered total electric field plots for a standard deviation (σ) equal to (a) 0% (nominal *RC* values), (b) 10%, (c) 20%, (d) 30% and (e) 40%.

reflected field is below -30dB. This reflected field is mainly attributed to the edge effects of the PMSF. This field can be considered as a reference point for the PMSF design. The reflected field resembles a small beam following Snell's law (at u = -0.5 and v = 0) with some sidelobes. The sidelobes are placed along the v = 0 line and the u = -0.5 line. By increasing the standard deviation to 10% (Fig. 4.23(b)) a more random pattern starts to appear, where noticeable fields are present outside the v = 0 line and the u = -0.5 line. This increasing scattered electric field trend is also true when the standard deviation increases to 20% (Fig. 4.23(c)) and 30% (Fig. 4.23(d)). When the standard deviation is increased to 40% (Fig. 4.23(e)) the *RC* values are spread out to the point where the response of the PMSF is so random that a clear reflected beam emerges at u = -0.5 and v = 0.

By plotting the total scattered power in the visible region ($P_{scat.}(\sigma)$) in (4.3), and curve fitting the simulated points, one can identify that there is an exponential relationship between σ and $P_{scat.}(\sigma)$, as shown in Fig. 4.24.

$$P_{scat.}(\sigma) = \int_{\theta=0}^{\pi/2} \int_{\phi=0}^{2\pi} \frac{(E_{Tot.}(\theta,\phi))^2}{\eta} \sin(\theta)\, d\phi\, d\theta. \tag{4.3}$$

Specifically the fitted curve followed the following format:

$$P_{scat.}(\sigma) = \alpha_1\, e^{\alpha_2 \sigma} + \alpha_3\, e^{\alpha_4 \sigma} \tag{4.4}$$

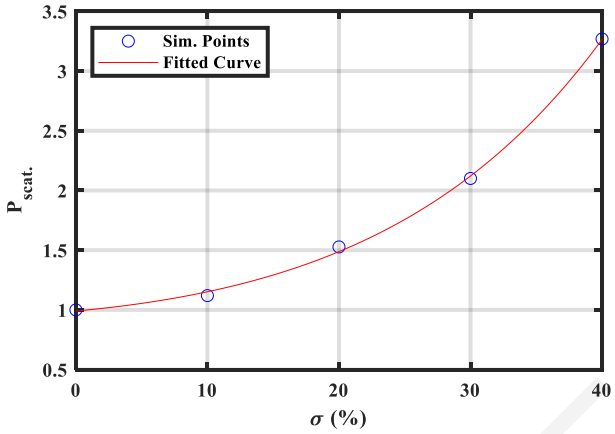


Figure 4.24: Normalized total scattered power ($P_{scat.}$) vs the IC's process standard deviation (σ). A fitted curved is plotted to unite the simulated data points.

where α_1, α_2, α_3 and α_4 are equal to 0.6783, -0.0105, 0.3122 and 0.05501, respectively. From the plot in Fig. 4.24, it can be observed that a standard deviation of 10% will produce little difference in the scenario where the PMSF is set to perfectly absorb an incident wave. In this case, $P_{scat.}(\sigma)$ will increase by roughly 15%, but for a standard deviation of 20% $P_{scat.}(\sigma)$ will increase by roughly 50%. For a standard deviation of 30% and 40% $P_{scat.}(\sigma)$ an increase of roughly 210% and 325% respectively is found. Although there are no statistical models available for the RF/MW components in the commercially available 180 nm technology used for the IC implementation [22, 114], a standard deviation of 10% remains in the expected deviation range found in the literature for RF/MW IC components [64, 122]. For this reason, it can be concluded that the PMSF design will operate even without ideal LE conditions, and with a standard deviation of the component element values up to 10%.

4.4.1.2 Multiple Beam Case

Similarly to the previous section, in this section the case where the PMSF is set to produce multiple pencil beams is studied. Two pencil beams are set to be reflected off the MSF one $\theta = 25°$ and $\phi = 225°$, and a second at $\theta = 25°$ and $\phi = 90°$. The incident wave again contains both TM and TE components and is at an angle of $\theta = 30°, \phi = 0°$. The TM component again is the x-polarized component and it is programmed by the tunable elements located along the x-axis, the RC elements R_1, C_1 and R_3, C_3. Their RC values are correlated again from the calculated reflection coefficients. Similarly, the TE component, which in this case is the y-polarized component, is programmed by the RC elements R_2, C_2 and R_4, C_4.

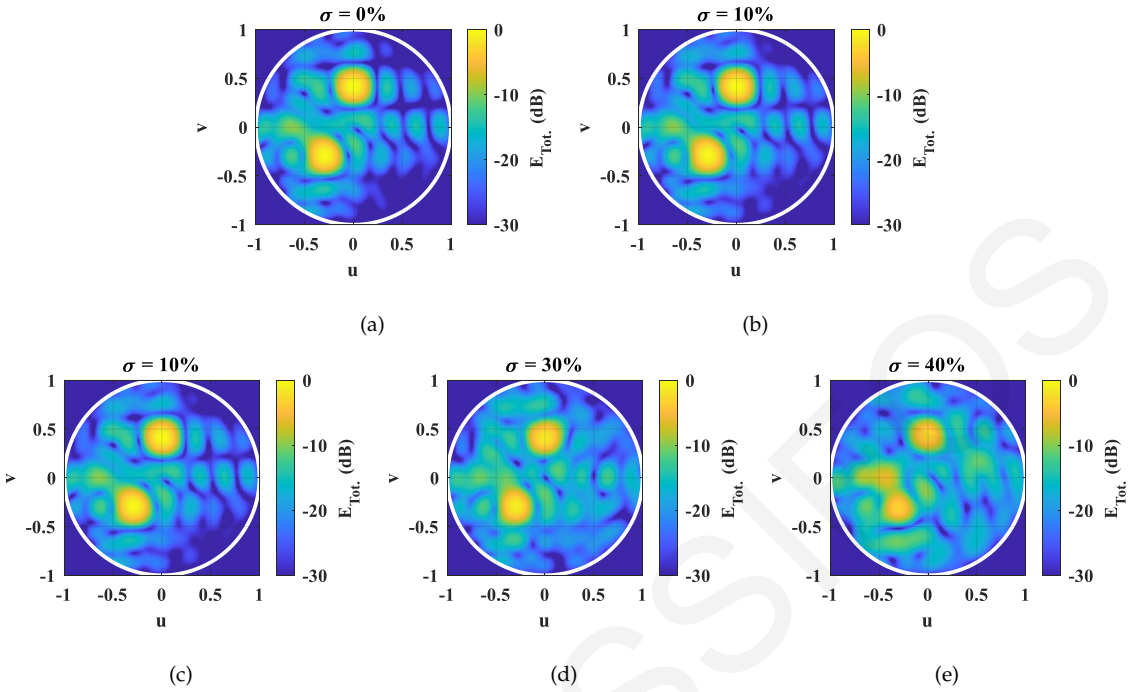


Figure 4.25: Scattered total electric field in dB plotted over the *uv* coordinates for a standard deviation (σ) of (a) 0%, (b) 10%,(c) 20%, (d) 30% and (e) 40%.

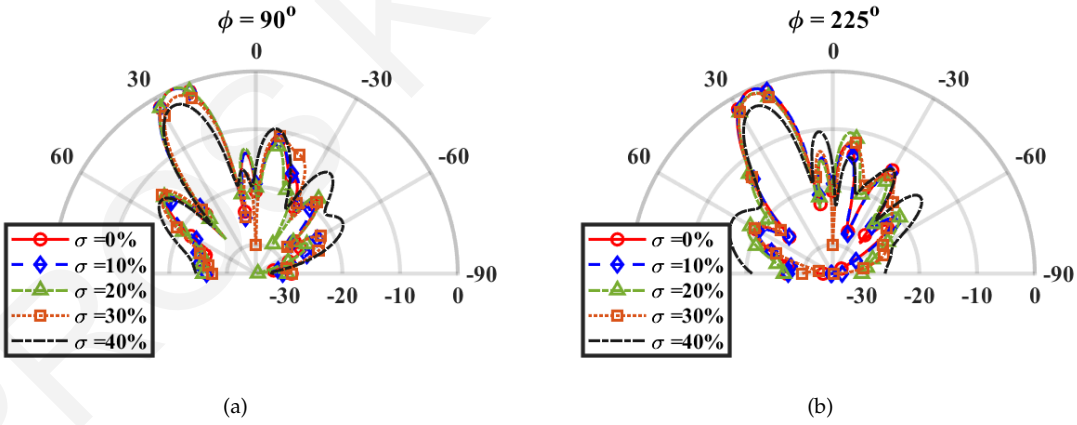


Figure 4.26: Polar plots of the scattered total Electric Field of Fig. 4.25 in dB. (a) $\phi = 90°$ and (b) $\phi = 225°$.

In this case there are not any nominal *RC* values since all unit cells are set to produce a different reflection coefficient. A normal distribution around the set *RC* is applied for the PMSF simulations to emulate the mismatch effects. A standard deviation, σ, of 10% to 40% of the nominal *RC* values is considered for all the unit cells *RC* LEs.

The simulated scattered total electric field results ($E_{Tot.}$) of the PMSF can be seen in Fig. 4.25 plotted over the *uv* coordinates. Two beams are clearly seen in all of the plots in Fig. 4.25, (Fig. 4.25(a)-Fig. 4.25(e)). In Fig. 4.25(b) a slight background

or sidelobe level increase can be seen. Sidelobe level increase can also be observed in Fig. 4.25(c) and Fig. 4.25(d). In Fig. 4.25(e) a third beam emerges at an angle following Snell's law.

In Fig. 4.26 the same results in polar form are plotted. It can be seen in both figures that the beams' intensity remains the same for a standard deviation up to 20%. For larger standard deviations (30% and 40%) the beams degrade, while the half power beam width increases.

4.5 Conclusion

Based on the experimentally measured effective *RC* range of the integrated PMSF LE, an innovative PMSF unit cell has been designed and optimized for absorption applications in the S-band around 3.6 GHz. By using the PMSF LE designed in this work, there is no need for the use of distributed high impedance nodes for biasing the LEs. The small space occupied on the ASIC, enables other communication and control circuits to be included on the ASIC, thus giving extra flexibility and freedom to the PMSF designer to integrate multiple adaptive PMSF LEs on a single ASIC.

An ASIC containing four of the proposed LEs was integrated into a planar PMSF consisting of exponential tapers arranged in a cross-like structure without breaking the symmetry of the unit cell. The unit cell achieved independent and simultaneous control of the absorption of both TE and TM polarized waves with incident angles ranging from 0° to 60°, thus overcoming the limitation found with the previous design in Chapter 3.

Control of the reflection coefficient's magnitude and phase for both TE and TM polarizations was demonstrated. Assuming individual control of each unit cell with the use of the proposed ASIC, which also contains control circuits and eight DACs, complex wavefront generation can be achieved by the proposed design. Complex wavefronts such as, multiple pencil beams and a mixture of OAM and pencil beams.

Multiple pencil beams with flexible polarization control were generated by this MSF design equipped with an ASIC on each unit cell. An example of a pattern with four separate pencil beams, each with linear, RHCP or LHCP polarizations was demonstrated. Additionally, an OAM and pencil beam pattern were generated. The calculated and simulated results are in good agreement, demonstrating the

capabilities of the proposed design.

With the demonstrated abilities, the design can perfectly absorb incident waves containing both TE and TM polarizations, such as an incident CP wave. This ability makes it attractive in RCS reduction and stealth technology applications. The presented wavefront generation capabilities of the design make it suitable in current multiple-user 5G and future telecommunication systems.

There are no statistical models provided by common silicon processese for RF/MW components, and there is no information available in the literature on the FF effect on IC-equipped PMSFs. For this reason, a study was conducted and the effects of mismatch on IC-equipped PMSFs have been presented. A standard deviation of 10% to an extreme of 40% of the nominal varactor and varistor's *RC* values have been considered. For a standard deviation of 10% the absorbance of an IC-equipped PMSF degrades by only a 15%. The same standard deviation has very little effect on the performance of the PMSF when producing a dual beam pattern. These results provide the confidence that realistic PMSFs that use ASICs implemented in commercially available silicon technologies will perform well under normal mismatch variations. In the next chapter (Chapter 5), the development and manufacturing of the ASICs is presented.

Chapter 5

ASICs for Programmable Metamaterials and Metasurfaces

Reconfigurable and programmable MSFs are man-made surfaces, which consist of sub-wavelength periodic elements, unit cells, that can be reconfigured to manipulate incident electromagnetic waves. However, reconfigurable MSFs developed to-date, have limitations in terms of impedance range, reconfiguration delay and power consumption. Also, these systems are costly, and they require bulky electronics and complex control circuits, which makes them unattractive for commercial use. The performance of the PMSF designs in Chapter 3 and Chapter 4 clearly demonstrates the benefits that ASICs can provide. In Section 4.4, the effects of ASIC mismatch was studied, and it was confirmed that the PMSF will operate under normal mismatch conditions. Here, in this chapter, with the findings of Chapter 3, Chapter 4, and the results from Section 4.4, the first family of CMOS ASICs that enable microsecond and microwatt reconfiguration of complex impedances at microwave frequencies is presented. The approach utilizes the asynchronous digital control circuitry, with simplified networking capabilities, allowing simple and fast reconfiguration via digital devices and user-friendly software. A low-cost solution is obtained that can cover arbitrary MSFs areas, with different sizes, shapes and unit cell geometries.

5.1 Introduction

Metasurfaces (MSFs) are electrically thin composite materials that consist of periodically spaced, sub-wavelength unit cells. These composite materials have gained the interest of many researchers, due to their ability to demonstrate novel functionalities, such as perfect absorption [22, 85, 92, 95, 107, 123], anomalous reflection [12, 83, 124], and beam shaping [125] to mention a few.

Reconfigurable MSFs have also been demonstrated by incorporating various tunable elements within the unit cell. Electrical tunability has been obtained using varactor diodes [20, 21], complex-impedance IC LEs [22, 92, 95, 107], liquid crystals [23] and power amplifiers [126]. Besides electrical tunability, other means of tunability have been demonstrated, such as magnetic [28] and optical [29] tunability. Optically tunable behaviour has also been shown by utilizing the optical properties of PDR1A [30], which has been shown to possess a memory effect [31].

Recently, programmable MSFs have emerged [32–36, 113, 126, 127]. These are tunable MSFs that control individual unit cell states through software. Often, the control of each unit cell is binary and is implemented through an FPGA development board [32, 34, 127]. An increase in unit cell state was achieved by incorporating digital-to-analog converters (DACs) between the FPGA and the tunable elements of the unit cell [33, 35, 36, 126]. With the individual unit cell control, programmable MSFs have demonstrated multifunctional applications e.g. polarization, scattering and focusing control [32], multi-focal spot control [33], holography [34], imaging [36], non-linear harmonic manipulation [35] and even beam steering while controlling the harmonic power level [113].

The advanced electromagnetic manipulation that programmable MSFs possess has made them an attractive solution for future wireless telecommunications. A recent study [38] showed that improved wireless connectivity can be achieved by incorporating MSFs in telecommunication systems. Even though this technology is still in its infancy, basic experimental verifications of simplified telecommunication systems based on programmable MSFs have been shown [128, 129].

Although the incorporation of PMSFs in wireless telecommunication systems can provide a clear advantage over traditional multiple input multiple output (MIMO) implementations and transceiver architectures [128, 129], there are major drawbacks that need to be addressed before they can be adopted. In particular, such

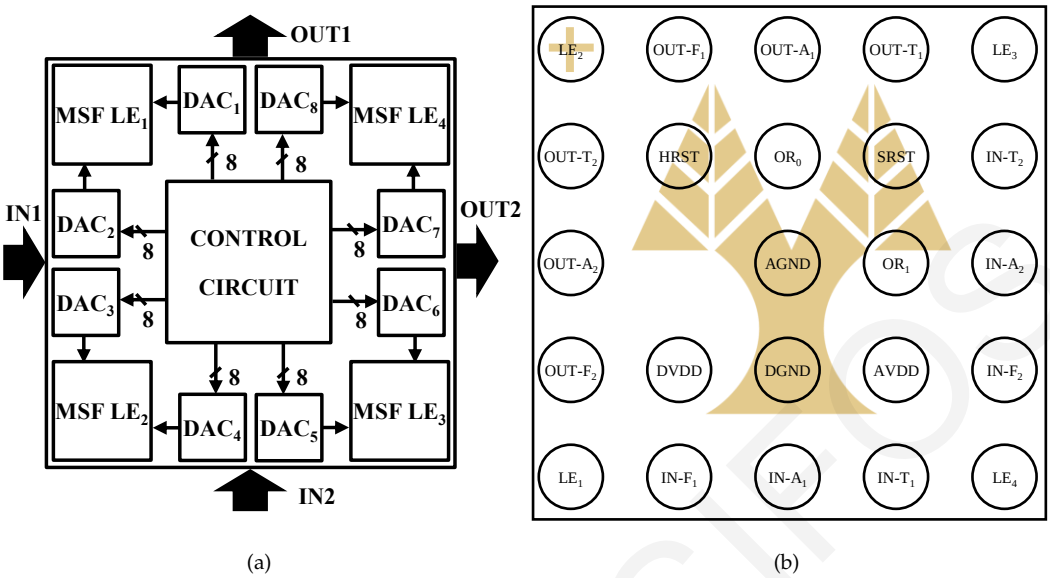
PMSFs need to be cost-effective, scalable, low-power and low-noise. The solution with FPGAs feeding discrete shift registers, to drive multiple DACs, that finally bias multiple power-hungry varactor diodes, although promising, cannot address the requirements for real-time programmability of MSFs. Furthermore, the bulky and complex electronics required in these systems limits their expandability and the option to be used by engineers that are not familiar with that particular system.

To address all of these requirements, major upgrades in the programmable MSF architecture need to be implemented. In this chapter, the first family of application-specific integrated circuits (ASICs) designed for PMSFs are presented. The ASICs satisfy all these requirements imposed by MSFs, and can become part of a MSF by connecting and controlling the surface impedance of each unit cell via software. They incorporate in a single die an asynchronous control circuit, multiple DACs and multiple complex impedance LEs.

5.2 Toward the First Family of ASICs

As described in Section 3.3, the ASICs utilize an asynchronous methodology for the control circuit to reduce noise and increase speed, while simultaneously consuming less power [96], when compared to traditional clocked systems. An eight-bit DAC is incorporated within the ASIC (Fig. 5.1(a)) in order to provide a fine adjustment of the low-power complex impedance LEs [22]. Four complex impedance LEs are incorporated in each ASIC, and can be individually addressed to provide more flexible control over the MSF unit cells. As was shown in simulations [22] for preliminary designs, the MSF design is able to show control of amplitude and phase of the reflection coefficient for both polarizations, independently and simultaneously. This ability was exploited to not only perfectly absorb an incident wave, but also to manipulate and transform various wavefronts [43, 44].

In this section, an intermediate step taken which will lead to the first family of MSF ASICs (Section 3.3) is presented. The purpose of the intermediate step is to test implemented building blocks of the proposed architecture (Fig. 5.1(a)) individually before a full wafer manufactured step. Risk mitigation strategies taken in this intermediate step are discussed. Although the section focuses mostly on the author's contribution, the RF part, the LEs, significant steps were needed to implement the ASICs from the control circuit, the DAC and the LE components side.



(a) (b)

Figure 5.1: Top-level network ASIC architecture in (a), and its footprint (b).

The foundational ASIC architecture can be seen in Fig. 5.1(a). The architecture consists of four LEs, eight DACs and a control circuit. Each loading element utilizes a MOSFET varistor and a MOSFET varactor to adjust the real and imaginary part of the impedance, respectively, while simultaneously having negligible static power consumption since their consumption is mainly due to of the leakage current through eight RF MOSFETs, which is very low compared to the rest of the circuits. Eight, 8-bit DACs are used to finely tune the varistor and varactor of each loading element of the ASIC. The digital inputs of the DACs are provided by the digital control circuit located at the center of the chip. The control circuit has two main operations. The first is to be part of a communication grid that will send/receive data packets to/from neighbouring nodes, in order to store the appropriate payload in its memory. The second is to provide the necessary digital inputs to the DACs, and in turn to tune the surface impedance of the corresponding unit cell.

5.2.1 Control Circuit

The control circuit operation is briefly described in this section. As mentioned previously in Section 3.3.5, the control circuit's operation has two main functions. The first is to provide the digital input to the eight DACs, which bias the LEs, and second is to send or receive data packets to / from neighbouring nodes in order to deliver the payload to the appropriate ASIC of the network which is formed on the MSF.

Table 5.1: Pin description of network ASICs.

Pin Name	Description
LE_x	Loading Element x Terminal
$IN-T_x$	Input True Signal
$IN-A_x$	Input Ack Signal
$IN-F_x$	Input False Signal
$OUT-T_x$	Output True Signal
$OUT-A_x$	Output Ack Signal
$OUT-F_x$	Output False Signal
$DVDD$	Digital Power
$AVDD$	Analogue Power
$DGND$	Digital Ground
$AGND$	Analog/RF Ground
$HRST$	Negative Hard Trigger Reset (or $\overline{HRST}$)
$SRST$	Negative Soft Trigger Reset (or $\overline{SRST}$)
OR_x	Orientation pins

The details of the control circuit and its network capabilities were published in [130]. The control circuit uses asynchronous circuits and communicates via handshake. Synchronous digital circuits are by far predominant in control circuit designs, however to maximize the ASIC usability for various MSF designs, and to avoid all issues associated with the clock tree synthesis of synchronous digital systems, an asynchronous route was adopted [96, 130]. A synchronous digital system would require a clock tree with scalability adjustments and would have to satisfy the requirements of flexible MSFs and walls of irregular shapes. In addition, the clock skew would have to be well controlled to eliminate any setup and hold time violations. Addressing all these with a synchronous digital system, would require a static system with scalability limitations. By using asynchronous digital circuits, the scalability becomes as simple as connecting unit cells or tiles of MSFs together, since there is no clock signal to synchronize the operations. Once the wires are connected, the system can operate without requiring any modifications or optimizations. Power consumption is also minimized by using the asynchronous circuit approach. Under static conditions, the asynchronous control circuit consumes only leakage current,

whilst the synchronous counterpart would consume both static and dynamic current, at every clock cycle. Specialized circuitry and techniques can be adopted to turn off certain parts of the chip when not needed, but still the buffers of the clock tree would be enabled. Also, the available area for the control circuit is limited due to the small size of the chip, and such synchronous circuits would consume a significant amount of free space allocated for the DACs and the LEs. Another major advantage of the asynchronous circuit approach, is related to the significantly reduced levels of electromagnetic emissions that are generated during programming [131]. A synchronous approach generates significant amounts of broadband noise during switching activity, given all transitions will happen at the same time. This creates problems for MSF absorber applications [22, 95, 107], given that the surface radiate EM waves at each clock event. This is not the case in our control circuit because the noise generated is lower and more evenly spread timewise, since only the chips that exchange data are enabled, while the rest are idle.

A CMOS 180 nm semiconductor technology was selected for the ASICs that balanced cost per die, mixed-signal capabilities, RF characteristics as well as low-power digital circuit capability operating at 1.8 V. Our proposed chips can realize reconfigurable MSFs and adjust the complex loading impedance of each unit cell individually. Depending on the application and MSF design, a large number of chips are required. These could amount to thousands of chips for a one square-meter MSF, thus chip cost is a critical factor. Wafer-level-chip-scale package (WLCSP) technology was selected because it enables both better RF performance, since bond wire parasitics and variations are minimized, as well as lower cost per chip when fabricated in large quantities, because the process of wire-bonding is not required and also the solder-balling process is much simpler and cost-effective. The diameter of the solder-ball spheres and the pitch of the balls were chosen to be 250 nm and 400 nm, respectively. Smaller solder spheres and smaller pitch sizes are available, but this increases printed circuit board (PCB) costs, on which the MSF is patterned. For smaller pitch sizes, special PCB processes are required and the reliability decreases. Therefore, the balls and pitch were kept at a size to comply with widely available high-frequency laminate PCB manufacturing design rules. The size of the ASICs was chosen to be 2.2 mm $\times$ 2.2 mm to increase their yield and subsequently keep the cost relatively low. The size of the chips and pin pitch subsequently dictated the number of available input/output (I/O) pins to be twenty five (Fig. 5.1(b)). The size of

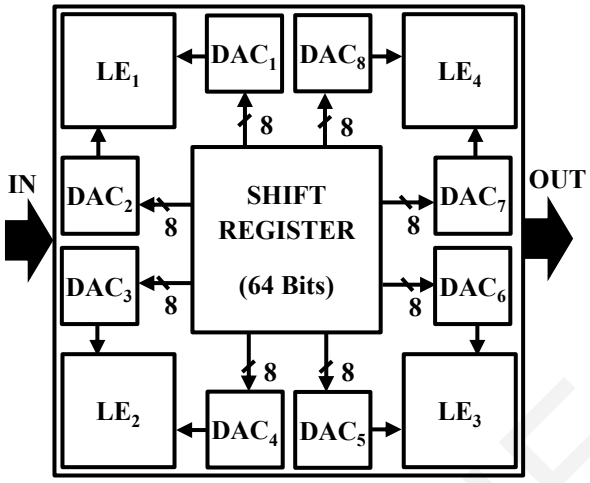


Figure 5.2: Top-level ASIC architecture where the control circuit is replaced with a simple 64 bit shift register as a contingency plan.

the ASIC and the pin limitation add constraints to the chip architecture. The number of available LEs were chosen to be four and this dictates the number of DACs, and subsequently the control circuit's complexity, communication, and control scheme. Due to the pin limitation, a serial communication scheme between the chips was adopted.

Due to the control circuit's complexity, it required numerous pins for communication and orientation. The footprint of the ASIC with network capabilities is shown next to its top-level architecture in Fig. 5.1(b) while a short description of the pins can be found in Table 5.1. A contingency plan was adopted as an intermediate step, a second MPW manufacturing step, before a full-wafer manufacture attempt. The contingency plan involved the replacement of the control circuit with a simple shift register. This shift register would still be asynchronous and serve the control circuit's two main functions. The shift register's top-level architecture can be seen in Fig. 5.2. The main difference between the two is the number of inputs and outputs. The network control circuit forms a 2D routing like network as described in Section 3.3.5, while the shift register control circuit will connect it to its neighbouring ASICs sequentially and will occupy the MSF area in a meander-like pattern. An example of sixteen ASICs occupying a 4×4 unit cell PMSF can be seen in Fig. 5.3. Each ASIC's output is connects to the next ASIC's input, thus forming a long shift register. Alternate rows change direction to occupy the 2D area and the first and last ASIC connect to the gateway.

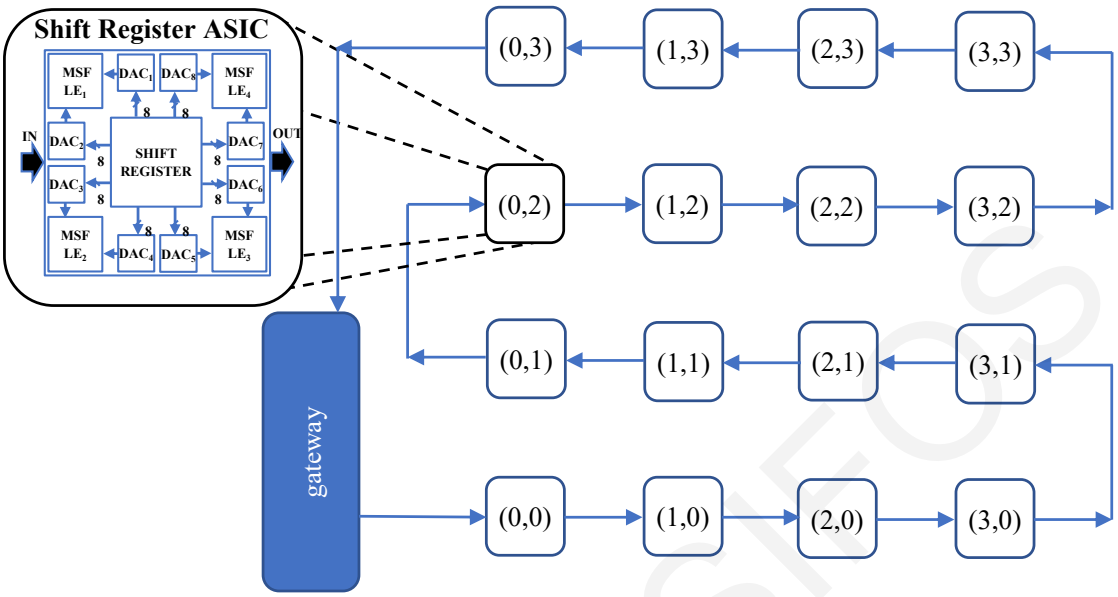


Figure 5.3: Sixteen shift-register ASICs populating a 4 × 4 unit cells. The ASICs are connected in a series and form a meander-like pattern. The gateway connects to the input of the first ASIC and to the output of the last ASIC.

This meander-like connection of the shift register control circuit ASICs will have a major drawback compared to the network operation ASICs, that it will not operate if any of the ASICs are not operating. It will not have any tolerance to faults, meaning that even one dry solder joint will render the whole MSF non-operational. For the sake though of demonstrating the LE range and some programmable EM manipulation it will suffice.

5.2.2 Digital to Analog Converter

Digital-to-analog converters (DACs) are used to convert the digital output from the control circuit data to an analog voltage value that can bias all the LEs V_C and V_R nodes. The DACs' simplified schematic can be seen in Fig. 5.4. A rail-to-rail two-stage resistor string DAC architecture was adopted for its simplicity, compact layout and low power consumption. Since the DAC would be biasing the gate of the MOS-varistor and MOS-varactor, it didn't have the need for any output buffer, which meant a further decrease in power and layout size.

This DAC's architecture utilizes two resistor strings with two multiplexers, in order to reduce the total number of resistors from 2 M to $2{\times}2^{M/2}$ as opposed to a normal resistor string. This results in a lower switch count, parasitic capacitance, de-

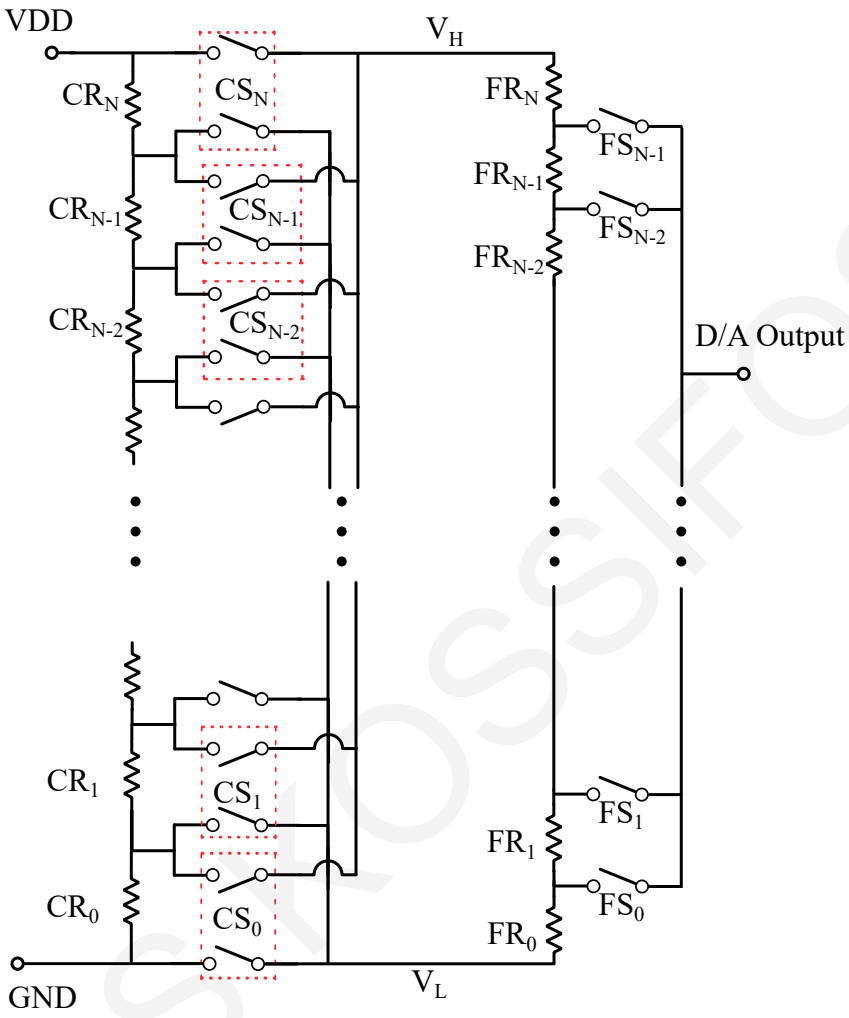


Figure 5.4: Simplified rail-to-rail two-stage resistor string DAC schematic.

coder complexity reduction and layout size. This 8-bit DAC architecture, is switched by coarse ($CR_0 - CR_N$) and fine resistor ($FR_0 - FR_N$) strings (Fig. 5.4). The coarse resistor string is switched by the four most significant bits (MSBs), the significant nibble (four bits), through the $CR_0 - CR_N$ switches and the fine resistor string by the four less significant bits (LSBs), the less significant nibble, through the $FR_0 - FR_{N-1}$.

All N+1 coarse resistors ($CR_0 - CR_N$) where N+1 is equal to 16, are identical. This creates an incremental voltage drop from the supplied voltage (VDD) to ground potential ($VDD/16$). Each node in the coarse resistor string is connected to switches, which serve as the first multiplexer. When a pair of switches ($CS_0 - CS_N$) closes, the voltages in the nodes N coarse resistor are transferred to one of the two outputs of the multiplexer, V_H and V_L. V_H connects the higher voltage potential to the top of the fine resistor string, while V_L at the bottom of the fine resistor string. This step effectively connects the coarse resistor string to the fine resistor sting ($FR_0 - FR_N$). Then, the less

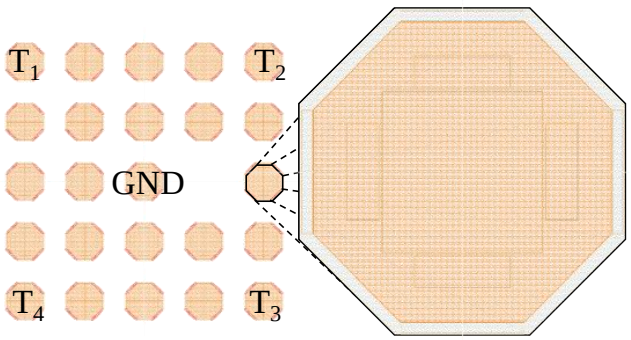


Figure 5.5: Custom octagonal pads for WLCSP.

significant nibble, controls the fine switches which connects the output to a divided by N+1 $V_H - V_L$ voltage. These two sequential divisions result in $(N+1) \times (N+1) = 256$ steps.

5.2.3 Loading Elements

The LEs are presented in this section. The steps taken to adapt the LE design presented in Section 3.3.1 to a WLCSP ASIC are presented. The complete WLCSP, its pads and traces were expected to affect the performance of the MSF LEs. The pads will add some parasitic capacitance and resistance, and will also have ESD protection devices, which will also introduce some parasitic effects. The company providing the PDK, in order to protect their intellectual property, only provided the pads as abstract cells (black box representation) without any circuit model to take into account the parasitic effects of the pads. An RF/MW IC design will need to include these effects early on in the design cycle. For this reason, custom octagonal pads were designed in order to be able to include the parasitics effects of the pads in the simulations. The pads were designed with only the two top metals in order to minimize their parasitic capacitance, as recommended for high frequency applications, [132]. As they were intended to be used in WLCSP, they didn't require mechanically strengthened pads, as is the case for wire-bonding pads. The designed pads can be seen in Fig. 5.5.

The LE circuit schematic of Fig. 3.8 was adapted to the designed octagonal pads and can be seen in Fig. 5.6. The LEs are connected between the four RF terminals (T_1-T_4) and the ground pad (GND). In order to minimize the parasitic resistance of the layout, a thick top metal was used and is routed in every available space between the pads from the LEs to the ground pad. This extra metallization though, adds an additional parasitic shunt capacitance and a series inductance and resistance. The

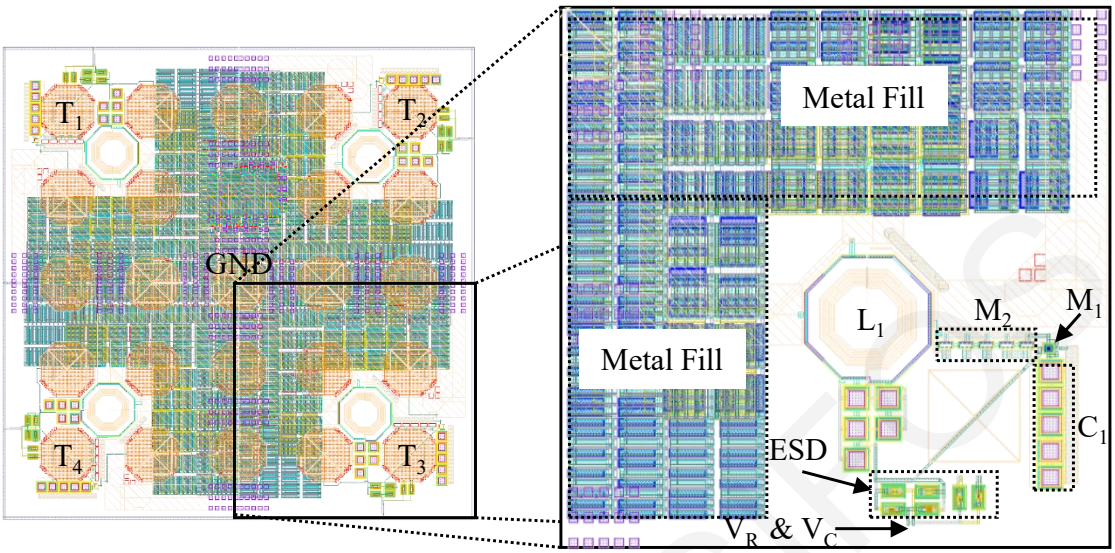
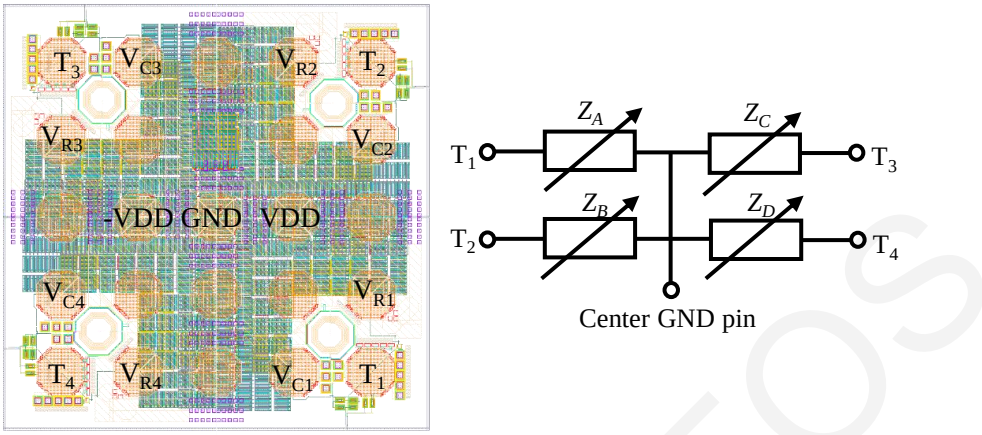


Figure 5.6: MSF LE's layout adapted to the ASIC's footprint in Fig. 5.1(b). The octagonal WLCSP pads can be easily identified on the left, where the ground (GND) and LE terminals can be seen (T_1 to T_4). On the right, a close up of the LE layout with the pads removed for clarity can be seen. All the circuit elements and metal fill can be seen in the close up.

parasitic capacitance can be compensated by removing some capacitance from the varactors.

The inductor (L_1) can be seen clearly in the layout in Fig. 5.6, since it is the largest component. The inductor's size was chosen to fit between the octagonal pads with some clearance for routing and to possess a high equivalent parallel inductance and resistance. The varactor (M_2) consists of five MOS-varactors which are located at the top side of the pad. This was implemented in order to minimize their distance from the ground pin and reduce the parasitic resistive losses and inductance. The varistor (M_1) with the DC-block capacitor (C_1) performance is not sensitive to its location, since the resistivity of the wiring is not comparable to the varistor's resistance. The DC-block capacitor is implemented using MiM capacitors, since they offer better performance and a smaller layout when compared to MoM capacitors. Low capacitance ESD protection devices [102] are used for the RF pads in order to minimize their effect.



(a) (b)

Figure 5.7: Four different LEs within the same IC. The layout can be see in (a) with overlaid the pin's description, and in (b), it's equivalent circuit.

5.2.4 Intermediate Step Dies

The purpose of the contingency plan was to test the building blocks (DAC, shift register control circuit and LEs) individually and as a whole. A die, which included LEs, DACs and a simplified control circuit (Fig. 5.2), and a shift register was designed. An individual test of the LEs at this step, would be serve as a confirmation of its operation and *RC* range validation in its WLCSP. For this purpose, a second die with a complete ASIC LE layout was designed without the control circuit and DACs, as shown in Fig. 5.7(a). In the same figure, the pins connected to the LEs biasing nodes (V_R and V_C) are marked. Since the complete layout contained four LEs, redundancy was added in this layout to compensate for process variations that could shift the LE's *RC* range. This was done by designing each LE with a different *RC* range. The best LE would be chosen after its measurement. Therefore, all LEs in this die have different *RC* ranges ($Z_A\,|_{(V_R=aV,V_C=bV)} \neq Z_B\,|_{(V_R=aV,V_C=bV)} \neq Z_C\,|_{(V_R=aV,V_C=bV)} \neq Z_D\,|_{(V_R=aV,V_C=bV)}$). Furthermore, a negative supply voltage (-VDD) was added in this design to add further redundancy. The negative supply voltage would allow us to bias the MOS-varactors biasing nodes (V_{C1} to V_{C4}) with a negative voltage. The negative *RC* range can be emulated in the final design by rotating the gate to the drain/source terminals. Therefore, the four LEs ranges and the negative supply voltage allow a total of eight *RC* range variations to choose from.

The four LE designs were designed with the same individual circuit element methodology described in Section 3.3.1. The LEs were simulated in CADENCE

VIRTUOSO™ using steady state S-parameter simulations, and the layout parasitics were extracted using ASSURA™. The conversion of the S-parameter to the four complex impedance loads (Z_A, Z_B, Z_C and Z_D) shown in Fig. 5.7(b) is the same as in Section 3.3.1. The complex impedances can be converted easily to the series resistance ($R_S = \Re(Z_{tot})$) and a series reactance ($X_S = \Im(Z_{tot})$) where Z_{tot} is the total individual impedance of either one of the loads. The loads can then be converted to a parallel connection as follows:

$$R_P = \frac{R_S^2 + X_S^2}{R_S} = R_S + X_S Q, \tag{5.1}$$

and the parallel reactance (X_P) is equal to:

$$X_P = \frac{R_S^2 + X_S^2}{X_S} = \frac{R_S}{Q} + X_S, \tag{5.2}$$

where, Q is the quality factor and is given by:

$$Q = \frac{X_S}{R_S}. \tag{5.3}$$

The simulated schematic results with the extracted parasitics can be found in Fig. 5.8 for all four LEs for the frequency of 5 GHz. The real and imaginary part ($\Re(Z_{tot})$, $\Im(Z_{tot})$) are plotted in Fig. 5.8(a), Fig. 5.8(d), Fig. 5.8(g) and Fig. 5.8(j) for the four complex impedance loads, Z_A, Z_B, Z_C and Z_D, respectively. Series resistance and capacitance (R_S, C_S) plots can be found in the next column of Fig. 5.8, in Fig. 5.8(b), Fig. 5.8(e), Fig. 5.8(h) and Fig. 5.8(k) for the four complex impedance loads, Z_A, Z_B, Z_C and Z_D, respectively. Parallel resistance and capacitance (R_S, C_S) plots are plotted in the right column of Fig. 5.8, in Fig. 5.8(c), Fig. 5.8(f), Fig. 5.8(i) and Fig. 5.8(l) for the four complex impedance loads, Z_A, Z_B, Z_C and Z_D, respectively.

Z_A loading element's equivalent parallel RC values vary from 1.6 pF to 3.6 pF and from 20 to 600 Ω (Fig. 5.8(c)), Z_B's RC values vary from 1.2 pF to 2.8 pF and from 20 to 640 Ω, Z_C's RC values vary from 0.3 pF to 2.5 pF and from 20 to 660 Ω and Z_D's RC values vary from 1.8 pF to 4.2 pF and from 20 to 570 Ω. Variations in the resistance in these ranges, the maximum parallel resistance reducing with increase of capacitance, is attributed to the quality factor of the varactor changing with voltage as it is generally known from the Q-V curves (see [62]).

The parasitics extracted using ASSURA in CADENCE VIRTUOSO took into account only capacitance and resistance effects. Due to the relatively large metallization of the LEs' layout, and the high frequency where the LE operate in, the

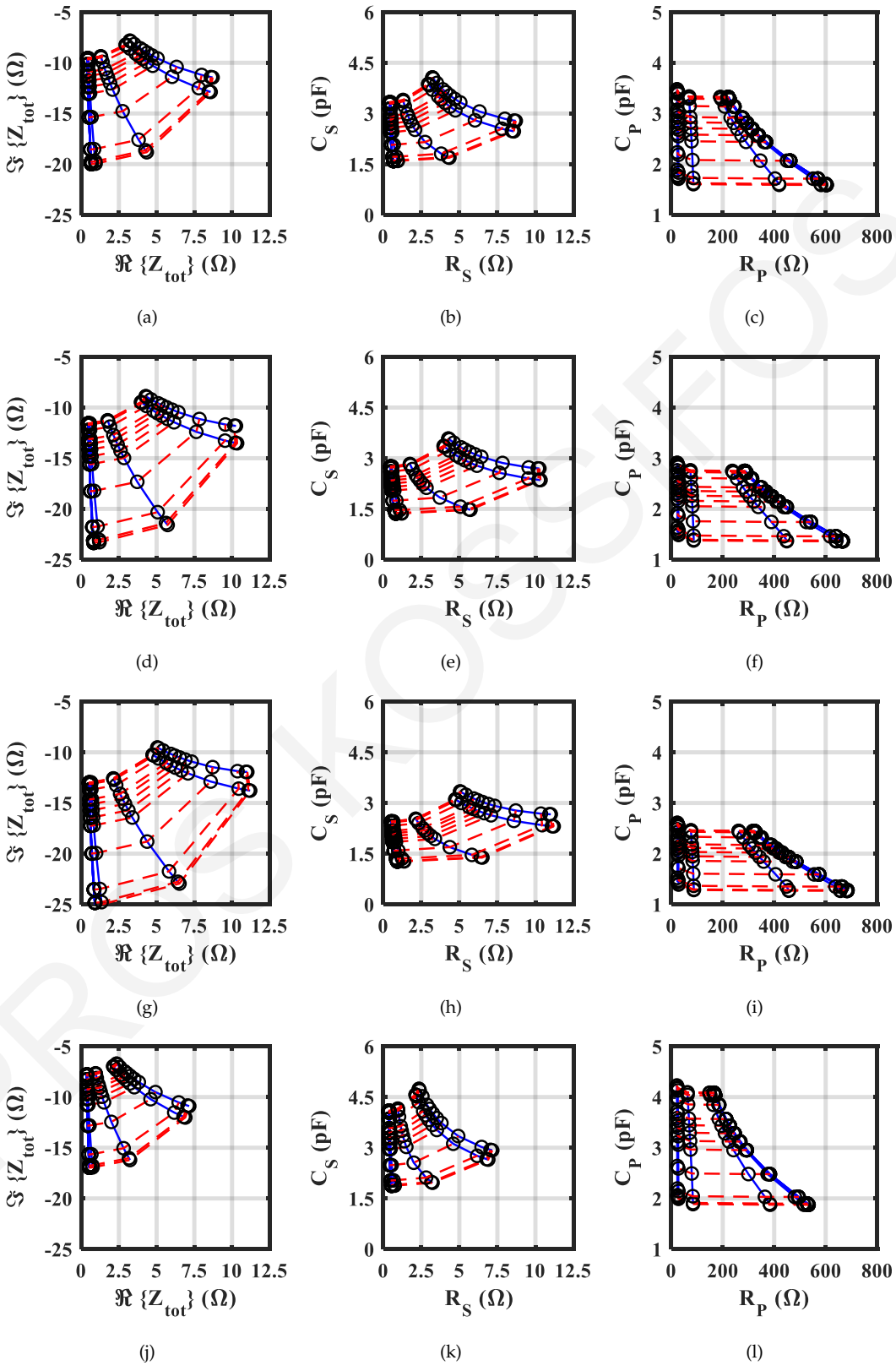
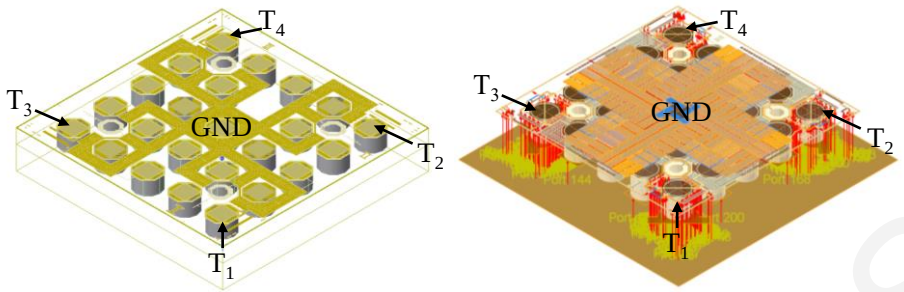


Figure 5.8: ASIC shown in Fig. 5.7 LE range plots. Results obtained through simulations in CADENCE VIRTUOSO and parasitics extracted in ASSURA. Z_A range plotted in (a), (b) and (c). Z_B range plotted in (d), (e) and (f). Z_C range plotted in (g), (h) and (i). Z_D range plotted in (j), (k) and (l). Ranges are plotted at 5 GHz and for $\Re\{Z_{tot}\}$ vs $\Im\{Z_{tot}\}$, series *RC* and parallel *RC*. The different ranges of impedances for each LE can be observed for bias voltages ranging from -1.8 V < V_C < 1.8 V and 0 < V_R < 1.8 V.



(a) (b)

Figure 5.9: 3D view of the ASIC's LE layout as shown in the Keysight's ADS. In (a) only the top thick metal is visible, while in (b) all metal layers and ports are visible. Over 300 ports are used.

inductive parasitics were also essential for the accurate simulation of the *RC* range. In order to accurately simulate the LEs' layout, it was imported into Keysight's ADS software and was simulated using its built-in method of moments electromagnetic solver, Momentum. The 3D layout can be seen in Fig. 5.9(a). The layout was incorporated with solder balls and an under bump metallization (UBM) layer. The metal fill layers placed to satisfy metal density rules (Fig. 5.6) were also simulated. These metals will also emulate the effect of the complete package on the performance of the LE, since metallization from the DACs and control circuit will be placed below the LEs. The complete layout metallization was simulated with extracted S-parameter files from the selected technology's circuit components. The layout, which includes the metal fill and the ports where the circuit elements connect, can be seen in Fig. 5.9(b).

The simulated results obtained from Keysight's ADS can be seen in Fig. 5.10. The equivalent parallel connection *RC* response for Z_A, Z_B, Z_C and Z_D are plotted in Fig. 5.10(a) to Fig. 5.10(d), respectively. Differences in the obtained results are easily identified with both the capacitance and resistance ranges shifting compared to the simulated results with the extracted parasitics from the ASSURA layout verification toll (Fig. 5.8). This shift is caused not only by the solder ball effect, which is not included in the results in Fig. 5.8, but mainly due to the inductive parasitic of the LE layout.

5.2.5 Single Die Pad Passivation and Ball Placement

The previous designs for individual LEs (Fig. 5.7(a)) and the shift register controller (Fig. 5.2) testing were manufactured through in an MPW. The dies can be seen in Fig. 5.11(a) and Fig. 5.11(b). The MPW provided would yield a small number

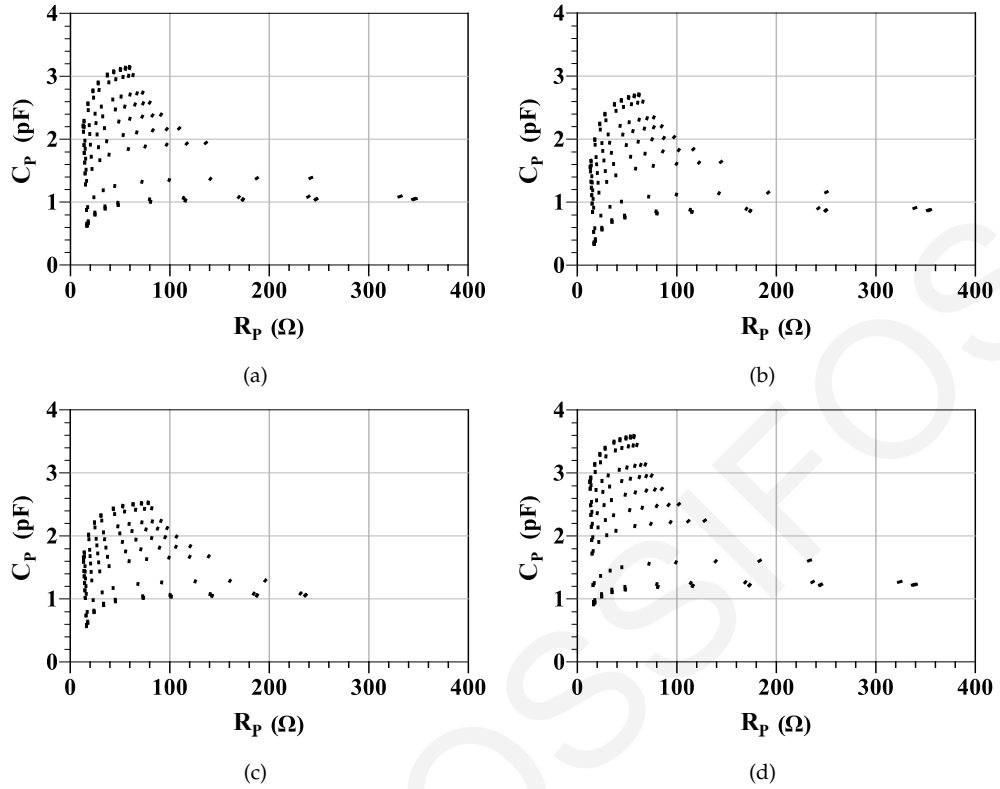
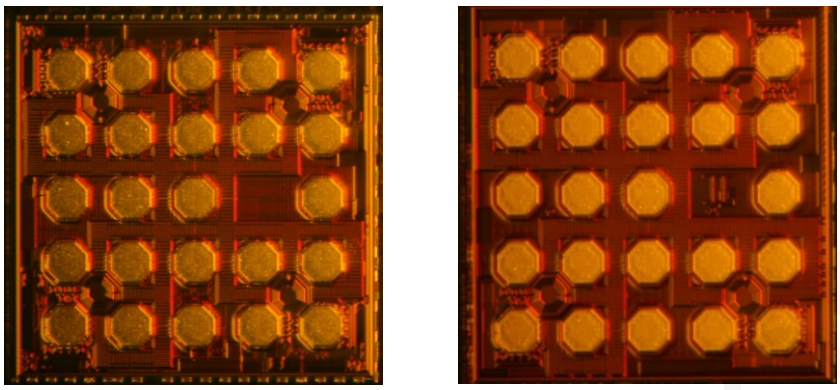


Figure 5.10: Test ASIC with LE layout *RC* ranges simulated in Keysight's ADS software using method of moments. Parallel configuration *RC* range are plotted in (a) for Z_A, (b) Z_B, (c) Z_C and (d) Z_D at the frequency of 5 GHz. The different ranges of impedances for each LE can be observed for bias voltages ranging from -1.8 V < V_C < 1.8 V and 0 < V_R < 1.8 V.

of individual ASIC dies. On these dies, there was no option to place solder balls on each pad, nor to provide metallization on each pad to allow the solder balls to properly adhere. This metallization is called UBM, and is needed since the pads' metal is aluminium (Al), which forms a thin oxide which prevents the solder from properly wetting its surface and adhering to it [133].

Within the VISORSURF consortium [55], IZM has had a long experience with electroless nickel/gold (Ni/Au) processes. IZM offered to deposit the UBM layer and place solder spheres on each pad. IZM's experience though was also on wafer level electroless Ni/Au processes. Single die UBM was significantly harder. There were extensive efforts to bring the single die in polyurethane carriers and then plate in the main electroless baths. This could not yield any qualitative Ni/Au UBM deposit. As a result, other techniques were tried by IZM like Au-stud bumps on Al pads. These attempt were successful mechanically. One stud bump or 4 stud bumps just to cover more the Al pad were positioned on the Al pads, whereas dispensed solder paste was deposited on the PCB to be measured. A single die with Au-stud bumps can



(a) (b)

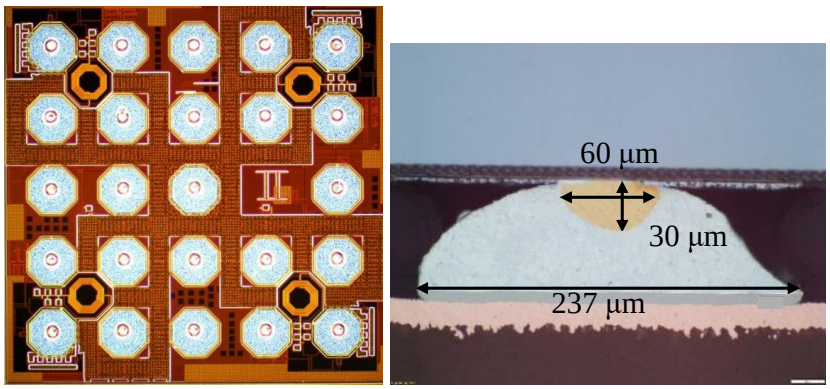
Figure 5.11: Single dies produced on a MPW. In (a) the design containing four LEs (Fig. 5.7(a)) and (b) the design containing the shift register control circuit, DACs and LEs (Fig. 5.2).

be seen in Fig. 5.11(a). A cross-section of the Au-stub bump is shown in Fig. 5.12(b). The solder ball flowed to a diameter of 237 μm, occupying the whole pad. On the top of Fig. 5.12(b), the dimensions of the Au-stud are shown which are 60 μm $\times$ 30 μm.

5.2.6 Intermediate Step, Loading Element Measurement

The experimental section for measuring the ASIC dies, that were produced in the second MPW is described in this section. The experimental part involved the deign of PCBs for the population of the bumped ASICs and the development of a de-embedding method along with de-embedding boards, to remove the PCB's effect from the measured results.

The total number of pins in this ASIC introduced a pin constraint which forced the LE to place the ground pin in the middle pad of the ASIC, as described in



(a) (b)

Figure 5.12: Single chip with Au stud bump (a). 25 μm Au wire diameter cut and formed as stud bump with a shoulder of 75 μm. A cross-section of the solder ball with the Au stud is shown in (b).

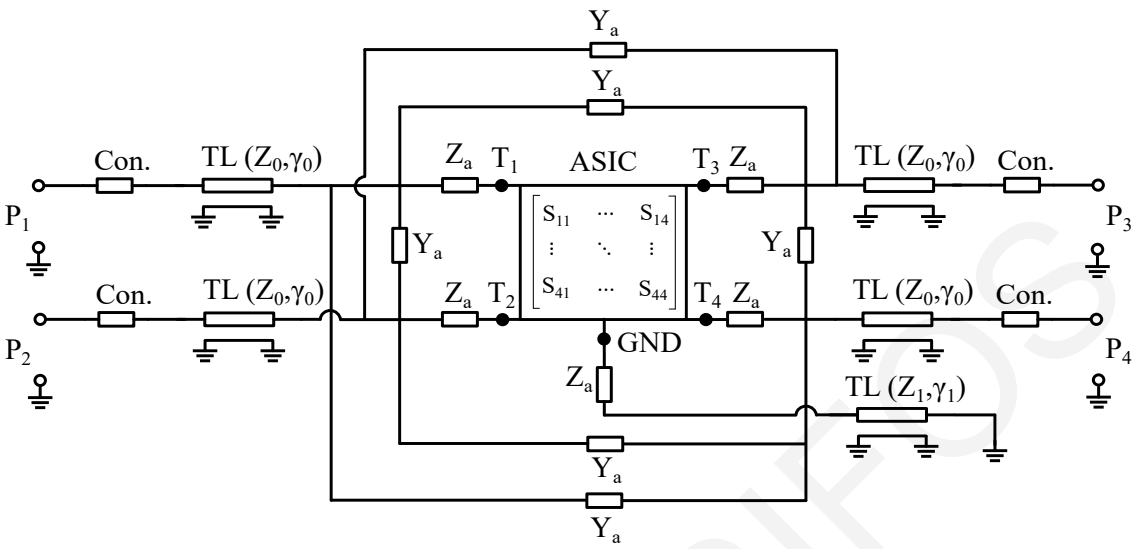


Figure 5.13: PCB simplified equivalent circuit. The circuit consists of connectors (Con), TLs and lumped impedances and admittances.

Section 3.3. In order for this ground pin to connect to the PCB ground layer or a ground plane, it needed to be routed with a PCB trace under the ASIC. Usually in WLCSP, which resembles ball grid arrays (BGAs), the pins are recommended to be routed with multiple PCB layers [134]. Since micro-vias were not available within the VISORSURF consortium, this routing needed to be implemented without utilizing any other metallic layer below the ASIC.

This metallization under the ASIC is in the RF signal's path and affect the measurement. For this reason, a custom de-embedding strategy was derived in order to satisfy the measurements and validate the design in this intermediate MPW step. The equivalent circuit of the populated boards can be seen in Fig. 5.13. The TLs and connectors (Con.) are the theoretical representation of the traces and the coaxial connectors leading from the LEs' terminals (T_1 to T_4). The centre ground (GND) pin can be seen in the same figure at the bottom of the five terminal ASIC symbol. The center pin is routed to ground through a series impedance and TL. The series impedances Z_A are caused by the solder balls' series inductances and resistance. Shunt admittances Y_A at the end of the TLs are expected as the effect of capacitive coupling between the terminals, and discontinuity effects caused by the transition from the TL to the solder ball.

The design of the two populated PCBs, one for the four-LE ASIC (Fig. 5.7(a)),

and the second for the simplified asynchronous control circuit (Fig. 5.2), can be seen in Fig. 5.14(a) and Fig. 5.14(b), respectively. The ground trace can be seen in the insert of Fig. 5.14(a). The RF terminals of the ASIC are connected to 50 Ω CPWG TLs which lead to the edge of the PCB, where 3.5 mm connectors are located. Four through-hole DC connectors are placed at the corners of the PCB, which lead to the V_R and V_C pads of the ASIC.

Since the measurements needed to cover a relatively small frequency range (2 - 6 GHz) the two-length method (Section 2.3.1.4) was chosen for the characterization of the TLs. The length (L) and two length ($2L$) de-embedding boards can be seen in Fig. 5.14(d) and Fig. 5.14(e) respectively. Once the TLs' characteristic impedance (Z_0) and propagation constant (γ) are characterized, the reference plane of the measurement is moved to the end of the TL by removing the connectors (Con.) and TLs. This is also done to an *open* board (Fig. 5.14(c)) which is identical to the populated PCB but without any ASIC placed on it. In this manner, the reference plane is moved on that *open* PCB and the shunt admittances Y_A are obtained and removed from the measurement. An equal length ground trace, which is shown in the insert of Fig. 5.14(a), is placed on the separate de-embedding board (Fig. 5.14(g)). The ground trace is connected at the center of the TL with one end connected to a ground plane, and this de-embedding board is referred as "TL-short". By moving the reference plane to the middle of the "TL-short" board, the ground trace response can be obtained and removed from the measurement. Due to the ASIC 0.4 mm pad pitch and pad diameter 0.25 mm, the larger ground trace width that could be implemented was 45 μm. This lead to a high impedance ground trace, which skewed the de-embedded results, therefore two parallel ground traces were placed. An extra though de-embedding board (Fig. 5.14(f)) was also manufactured to add some redundancy in the measurement.

The measurement set-up for the single-die solder-bumped ASICs can be in Fig. 5.15. The populated board with the ASIC which contained four LEs can be seen in the bottom left insert of the figure, while the de-embedding boards can be seen in the bottom right of the figure. The board was supplied with the appropriate supply (VDD, -VDD and GND) and biasing voltages to the V_R and V_C connector pins from a Keithley 4200-SCS. The S-parameters were measured from an Agilent E8363B VNA connected to the coaxial, 3.5 mm connectors of the PCB.

Although the single-die bumping procedure described in Section 5.2.5 produced

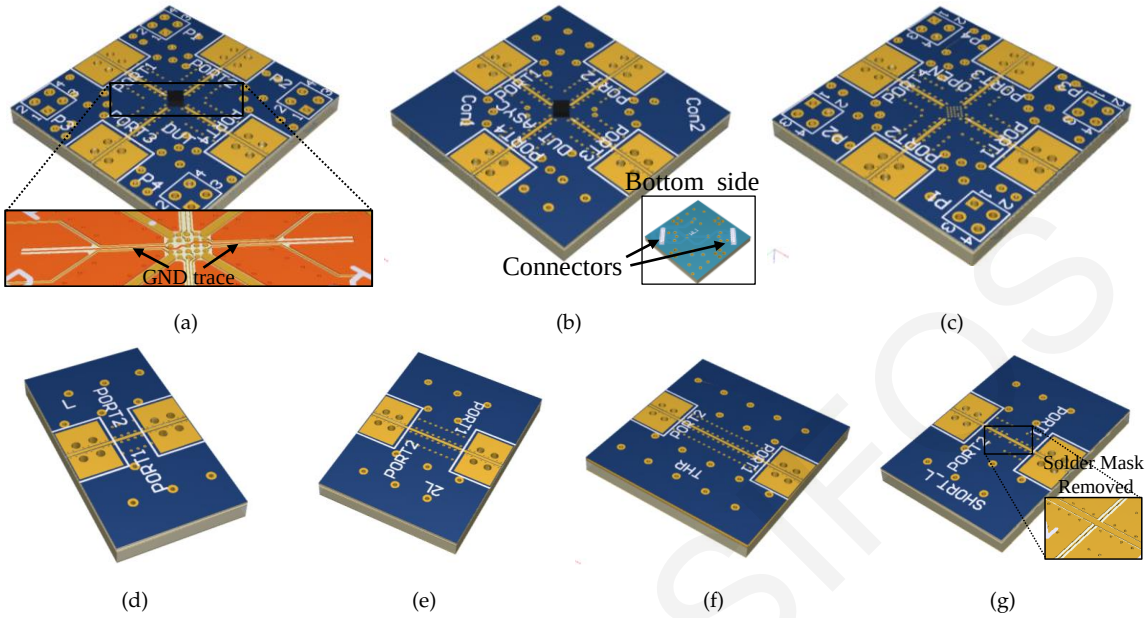


Figure 5.14: Populated PCBs with the bumped ASICs and de-embedding boards. (a) Four LEs PCB, (b) shift register PCB. De-embedding boards can be seen in (c)-(g). (c) open, (d) L, (e) 2L, (f) though and (g) TL-short.

mechanically sound solder bumped dies, the electrical properties of the dies were compromised. The solder bumped dies were damaged by ESD in the bumping process. This was confirmed by measuring the resistance in the V_C nodes to ground of the ASICs. This node is connected to the gate of the MOS-varactor and should have been in the MΩ range but was in the kΩ range.

This ohmic test, was repeated on ASICs that didn't go through the single-die bumping process, and were found to have an intact gate with a resistance in the

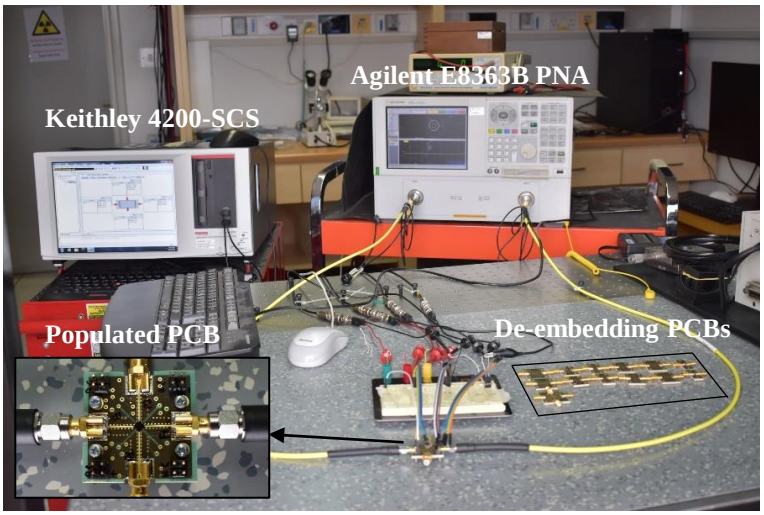


Figure 5.15: Measurement set-up for single-die solder-bumped ASICs. The populated PCB and the de-embedding PCBs can be seen in the figure.

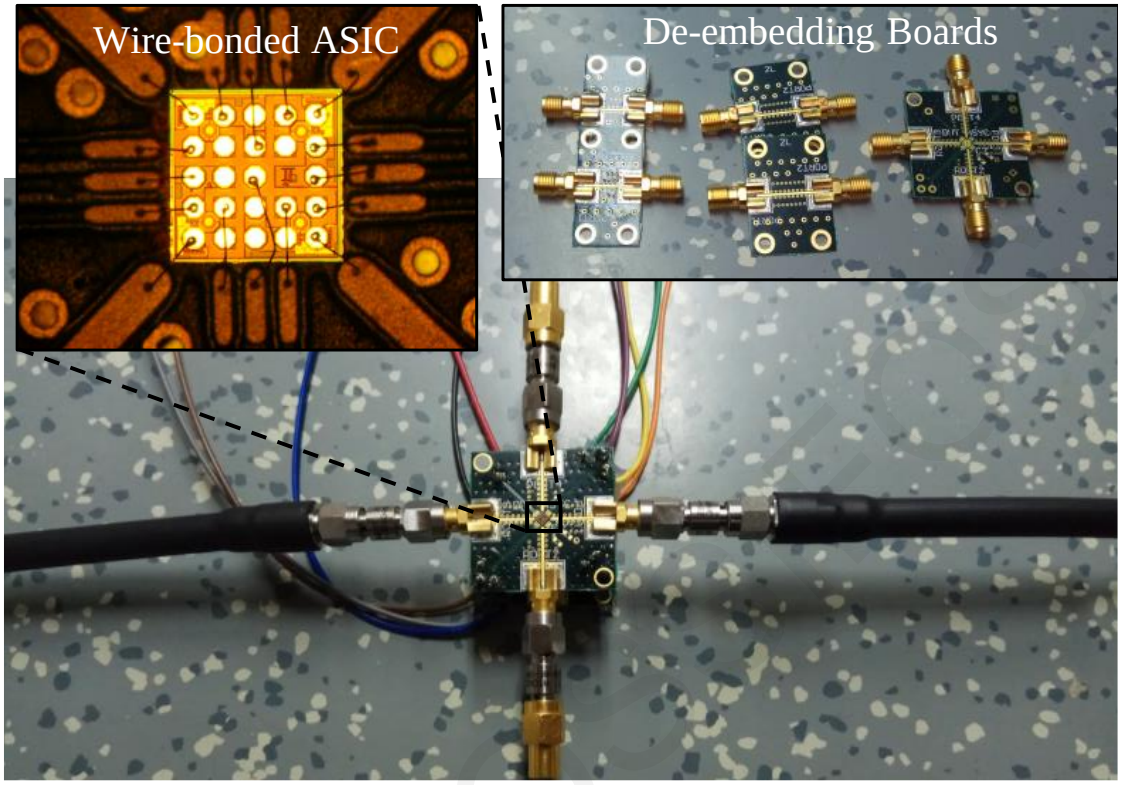


Figure 5.16: PCB for connecting the ASIC with wire bonds. The wire-bonded ASIC close-up micro-photograph can be seen in top left corner, while the L, 2L and open de-embedding boards can be seen in the top right corner.

MΩ range. In order to measure the functionality of the ASICs, another set of PCBs were designed and were populated with the bare-dies without any solder bumping (Fig. 5.16). The ASIC pads were wire-bonded to the TLs and other exposed tracks, as can be seen in the close-up micro-photograph in the top-left corner of Fig. 5.16.

The measurements were performed using the ASIC with the shift register version controller. This would mean instead of manually biasing each LE V_R and V_C node, a series 64 bits were fed in the ASIC's shift register to set the DACs input digital values, which will subsequently biased the LEs. The measured S-parameter were de-embedded and the effect of the wire bond was removed by considering it a series resistance of 0.50 Ω and a series inductance equal to 7 nH. The measured series and parallel RC ranges can be seen in Fig. 5.17. The series resistance and capacitance for the LE_1 (CA_S and RA_S) and LE_3 (CC_S and RC_S) can be seen in Fig. 5.17(a) and Fig. 5.17(c), respectively. The parallel resistance and capacitance for the LE_1 (CA_P and RA_P) and LE_3 (CC_P and RC_P) can be seen in Fig. 5.17(b) and Fig. 5.17(d), respectively. Even though in this design all LEs are identical, the ranges in the measurements don't match. There is a small, approximately 0.5 Ω resistance and a 0.25 pF capaci-

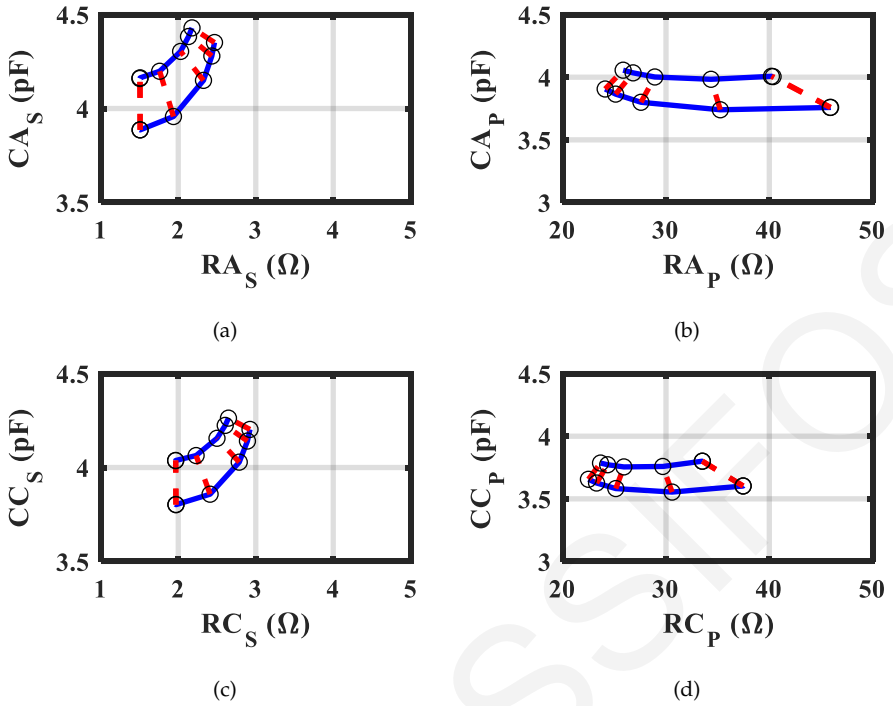


Figure 5.17: Measured resistance and capacitance ranges for the shift register version controller ASIC (Fig. 5.16). Series *RC* ranges for (a) load connected to T_1, and (c) connected to T_3. Parallel *RC* ranges for (b) load connected to T_1, and (d) connected to T_3.

tance difference in the series *RC* ranges. This discrepancy is caused by the wire-bond arch having different length and slightly different geometry. Furthermore, the die placed off-center on the PCB, could cause such a shift.

It is apparent that the *RC* measured range of the LE are not accurate, but even so a significant step was taken in this intermediate step. For one, the simplified ASIC version was measured for the first time. The measurements showed the operation of the DAC and the shift register. Without measuring accurately the *RC* range of the design, there are significant risk that the MSF will shift its operation frequency and even the angular perfect absorption range would degrade. For the design in Chapter 4 this would mean further degradation in the other synthesis functions.

The networking capabilities of the ASIC, the control circuit shown in Fig. 5.1(a), still had not been manufactured and held the highest risk. A shift in the *RC* range of the LEs would cause a performance degradation of the MSF and could be compensated for by an alternative MSF design. A failure in the control circuit on the other hand, would render the MSF non-operational. These events, lead to a risk mitigation plan and the formation of the first family of ASICs for MSFs, which is described in the next section.

5.3 The Design of the First Family of Metamaterial and Metasurface ASICs

The ASICs described in this section are a family of mixed-signal ICs optimized for the control of MTMs and MSFs. They are specifically designed to meet the needs of high volume, cost-sensitive, low-consumption and low EM noise applications that are required in MTM and MSF applications. As described in the previous section, performance and complete failure risks were identified. Initially, the individual sub-components (LEs, DACs and control circuit), were going to be tested separately, ensuring their operation and performance before a full wafer manufacturing step was taken. Due to many interdependencies, these subcomponents were not tested and characterised in the first two intermediate MPW steps described in Section 3.3.7 and Section 5.2. A risk assessment was performed, and two critical risks were identified.

- Firstly, the asynchronous digital network control circuit might fail. This will lead to a failed programmability of the LEs, and subsequently a complete PMSF failure. This is due to the high risk involved in asynchronous digital network control circuits. The asynchronous control circuit with the networking capabilities of Section 3.3.5 had not been tested yet. This component was the most complex component in the ASIC, and carried the highest risk of failure.
- Secondly, the LE's range might deviate from the simulated range due to inaccurate models supplied by the foundry at the frequency of interest and even from some unforeseen parasitics. As was identified in the technology validation step (Section 3.3.7) the measured quality factor of the MiM capacitors and MOS varactors were significantly lower compared to the simulated quality factor. This lower quality factor reduced the measured parallel capacitance range to half compared to the simulated range. This reduction was needed to be quantified also in the final LE to adapt the MSF before the PCB fabrication.

To mitigate the first risk, the simple asynchronous shift-register styled control circuit scheme that was designed in Section 5.2.1 was adopted as a fallback solution, in case the more complex Manhattan network control scheme failed. To mitigate a shift or reduction in the LE's range, two variations (version 1 and version 2) of the LE were designed with slightly different ranges. With these risk mitigating actions,

Table 5.2: Summary of first family of ASICs for MSFs.

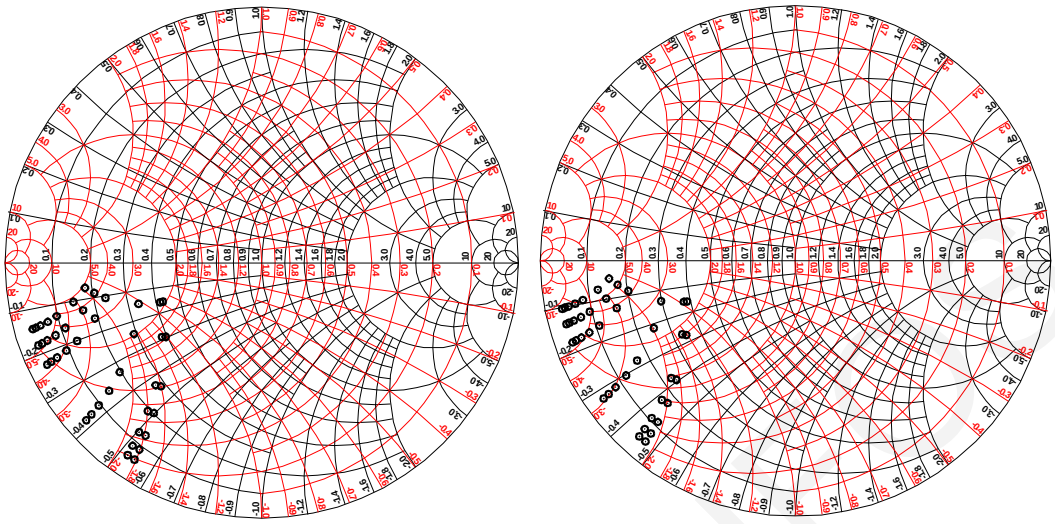
Design No.	System Con. Cir.	System DACs	System LEs	Centre Freq. (GHz)	LE Type
1	SR	8	4(V1)	5	A
2	SR	8	4(V2)	5	A
3	SR	8	4(V1)	3.6	B
4	SR	8	4(V2)	3.6	B
5	SR	8	4(V1)	5	B
6	SR	8	4(V2)	5	B
7	N	8	4(V1)	5	A
8	N	8	4(V2)	5	A

four versions of the ASICs were formed. These four version can be seen in Table 5.2 as Designs 1, 2, 7 and 8, where in the control circuit column the Manhatan network control scheme is identified with the letter *N* and the shift register with the letters *SR*.

The shift register control circuit version had less pin requirement compared to the Manhatan network control scheme ASIC. This freed some pins which could be utilized by the LEs and increase their *RC* range. As such, a second LE layout (LE connection-B in Table 5.2) was designed with an increased range. This LE was adapted in the shift register control circuit scheme ASIC. Two LE connection-B versions were designed with slightly different *RC* ranges to accommodate any possible range shift. Further redundancy was also incorporated into these designs by designing the designs at a lower frequency of 3.6 GHz. These second footprint LEs can be found in Table 5.2 as Designs 3, 4, 5 and 6.

5.3.1 Loading Element Connection Types

In this section, the LEs designs are presented. Two different LE layouts were designed. In the first layout, the four LEs form a cross-like connection and have the type-A LE connection, as initially designed in Section 5.2.3. In the second layout, each LE is surrounded by its own local ground terminals forming an isolated footprint that resembles a GSG connection. This layout is placed in each corner of the ASIC, leading to the type-B LEs layout. Two different type-A layouts ASICs designs were



(a) (b)

Figure 5.18: Simulated results for the type-A LE. (a) Design 1 and 7, Version 1 and (b) Design 2 and 8, Version 2.

manufactured and two type-B layouts designs were adapted with slightly different *RC* ranges in each footprint type.

5.3.1.1 Loading Element Connection Type-A

Two versions of the LE with connection type-A were designed, the design layout forms a cross-like connection as was shown in Fig. 5.9. The location of the four LE terminals (T_1 to T_4) are located at the edge pins of the ASIC, while the ground is located at the centre pin. The type-A LEs design is adapted for both the shift register version of the ASIC (Design 1 and 2) and the network version of the ASIC (Design 7 and 8). The shift register type-A ASIC (design 1 and 2) footprint can be seen in Fig. 5.20(a), and a short description of the pin functions can be found in Table 5.3, while the network type-A ASIC (design 7 and 8) footprint pin's description can be found in Fig. 5.1(b) and Table 5.1, respectively.

The type-A LE layout was simulated in Keysight ADS using its built-in method of moments electromagnetic solver, Momentum. The simulated results can be seen in Fig. 5.18. In Fig. 5.18(a) the results of the first version of the LE are plotted for multiple biasing voltages V_R and V_C on a Smith Chart. The second version of the type-A loading element is plotted in Fig. 5.18(b). The two versions occupy slightly different areas on the Smith Chart, where Version 1 (Fig. 5.18(a)) is slightly less capacitive than Version 2 (Fig. 5.18(b)).

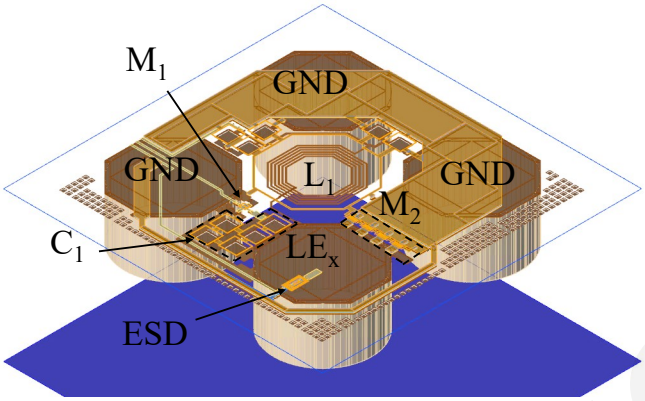
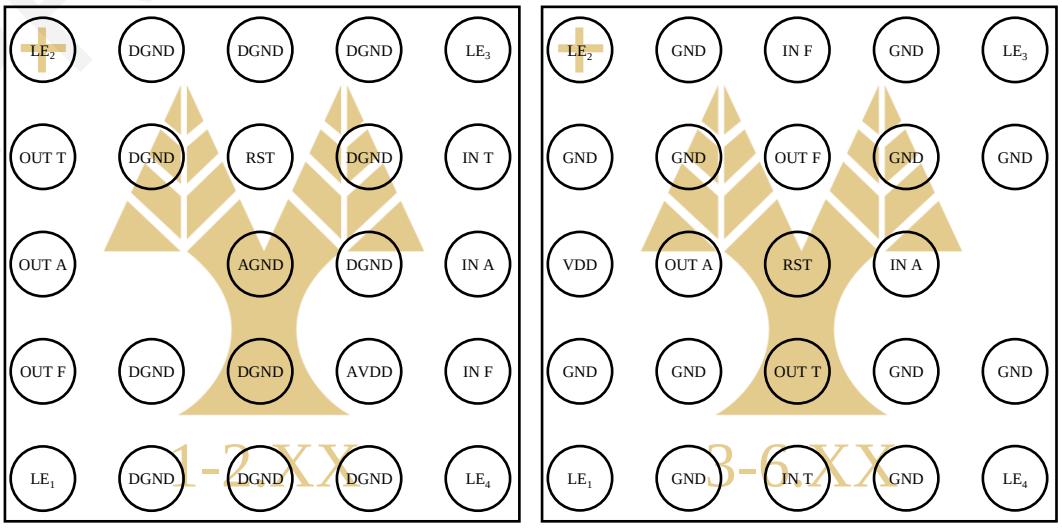


Figure 5.19: Type-B metasurface LE. The individual circuit element locations, the ground and LE pins are indicated.

5.3.1.2 Loading Element Connection Type-B

A second layout variation was also designed that has advanced performance. A three-dimensional view of the layout of a single type-B loading element can be seen in Fig. 5.19. The LE is configured to connect to TLs like a CPWG and load them like a GSG load. This load type is more common in RF and MW designs.

The 3D structure of the type-B LE is positioned at the four corners of the ASIC, as can be seen in Fig. 5.20(b). As can be seen in Fig. 5.19, the ground pins (GND) form a ring around the LE terminal of the LE. With this, the expected parasitics are reduced since the connection distance between the signal and ground pins are reduced from $2\sqrt{2}$P to P, where P is the ASIC's pitch. This is more clear by comparing the ASIC's



(a) (b)

Figure 5.20: Footprints of the family of ASICs for the view of the logo facing up. (a), Footprint for designs 1 and 2 and (b), Footprint for designs 3 to 6.

Table 5.3: Pin Description of ASICs Designs 1 to 6.

Pin Name	Description
LE_x	Loading Element x Terminal
IN T	Input True Signal
IN A	Input Ack Signal
IN F	Input False Signal
OUT T	Output True Signal
OUT A	Output Ack Signal
OUT F	Output False Signal
DVDD	Digital Power
AVDD	Analog Power
GND	Common Digital and RF Ground
DGND	Digital Ground
AGND	RF Ground
RST	Negative Trigger Reset (or $\overline{RST}$)

footprints in Fig. 5.20(a) and Fig. 5.20(b). The inductor (L_1), the varactor ($M2$), the varistor (M_1) and the DC-block capacitor (C_1) location, can be seen in Fig. 5.19. Low capacitance ESD protection devices ([102]) were used in the type-B LE, and their location can be seen in the same figure.

Furthermore, in the type-B LE layout, the connection from the signal to ground doesn't overlap with any digital circuits that could potentially couple and affect the LE's impedance. In the type-A version, the LE connects to ground through the top-layer thick metal that almost occupies the complete layer. It should be noted that even though rigorous simulations were performed, there is the possibility that the RF signal can be coupled to a digital circuit in the type-A version, but there is no possibility in the type-B LE layout.

Four variations of the type-B layout were adapted to introduce some *RC* variability. Two versions were designed to operate at 5 GHz and another two versions to operate at 3.6 GHz. Each frequency variant is further subdivided into two other variations, where for each design the tunable capacitance is centred at a different value. The type-B LE layout was simulated using the Keysight's ADS using its built-in method-of-moments electromagnetic solver, Momentum. Simulated results

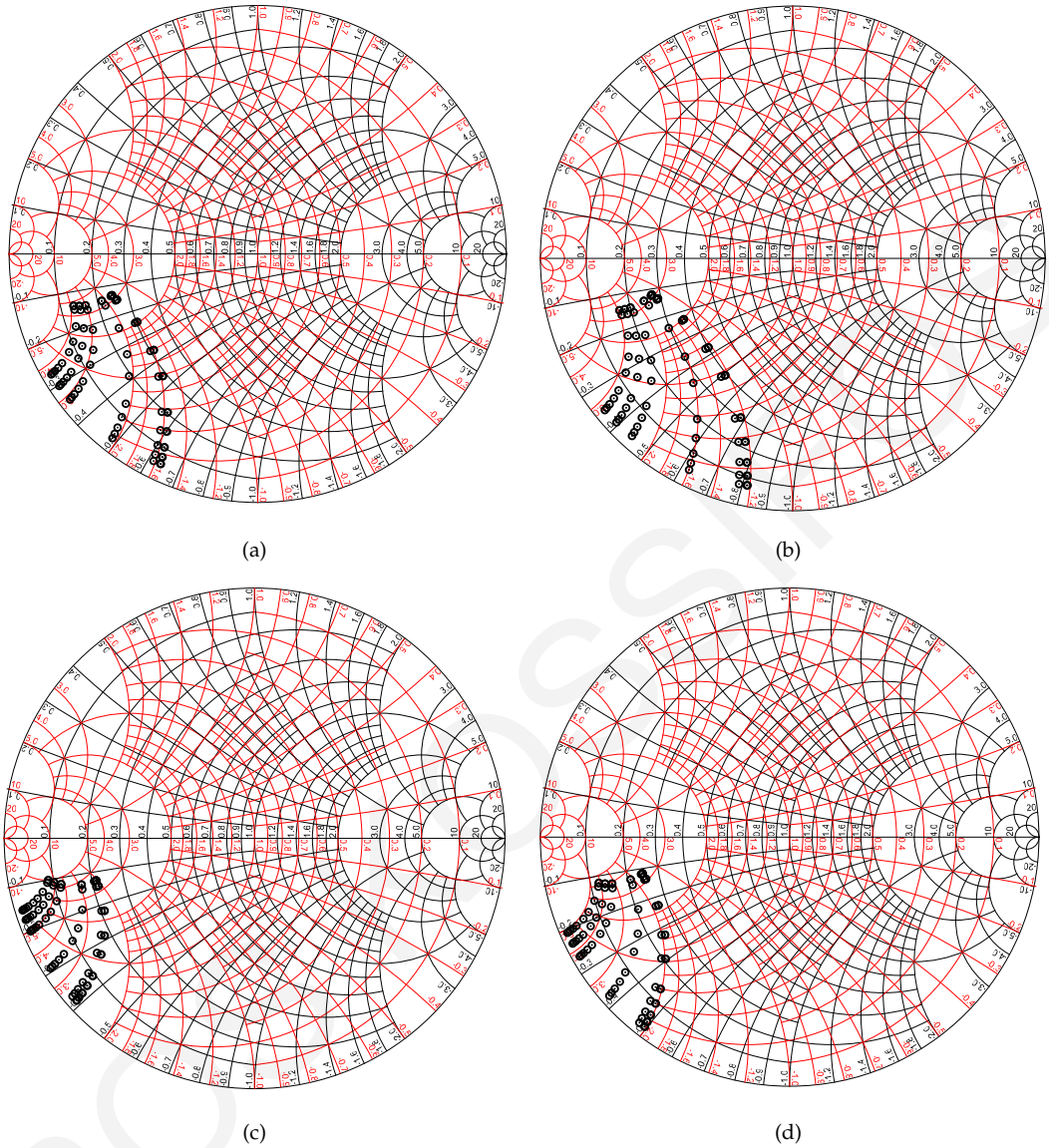
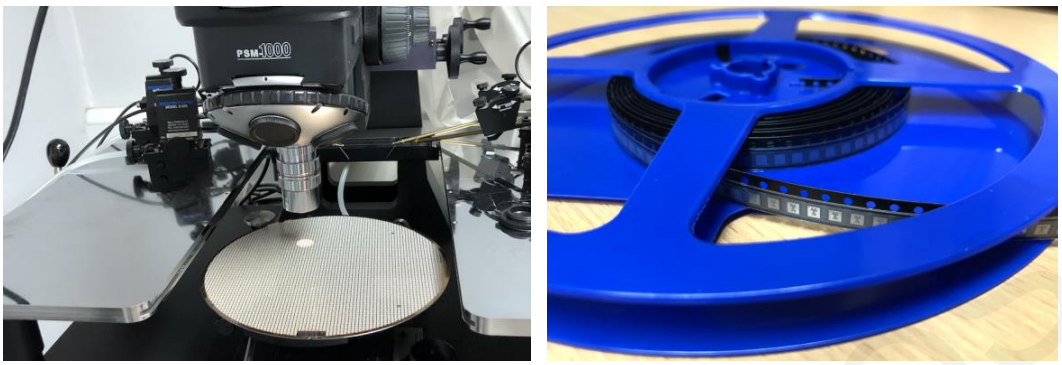


Figure 5.21: Simulated results for the type-B loading element. (a) Design 3 at 3.6 GHz, (b) Design 4 at 3.6 GHz, (c) Design 5 at 5 GHz, and (d) Design 6 at 5 GHz.

for the type-B layout LEs can be seen in Fig. 5.21. In Fig. 5.21(a) and Fig. 5.21(b), the impedance of the LEs is plotted for the two versions which have a design frequency of 3.6 GHz. In Fig. 5.21(c) and Fig. 5.21(d), the impedance of the two versions is plotted for the two designs that have a design frequency of 5 GHz. Version 1 in both operating frequencies (5 GHz or 3.6 GHz) is slightly more capacitive compared to Version 2 in the same operating frequency.

The type-B LE (Fig. 5.21) compared to the type-A LE layout (Fig. 5.18) can provide a range closer to the perimeter of the smith chart. This is true for both 3.6 GHz versions and 5 GHz, and will translate to a smaller minimum series resistance or larger maximum parallel resistance (5.1). This is due to the reduction in the layout



(a) (b)

Figure 5.22: In (a), a bumped wafer placed on the probe station to be inspected can be seen and in (b) ASICs on tape and reel are shown.

parasitics that the type-B layout can provide. This is highly desirable for the PMSF designs in Chapter 3 and Chapter 4.

Concluding, contingency designs have been presented, with two variations in capacitance range, two variations in layout and two designs with a lower design frequency.

5.3.2 Wafer Level Packaging and Tape and Reel

The packaging steps of the eight ASICs chips, from full wafer to WLCSP is briefly discussed in this section. The designs were manufactured on 8-inch wafers using the selected 180 nm technology as shown in Fig. 5.22(a). The eight designs were placed in a reticle which was repeated on the wafer. Post wafer processing was performed by a third-party company, which placed the UBM layer and the solder balls at the wafer level. Wafer lapping, marking the back side was also done, and wafer dicing. The eight designs were sorted based on the provided reticule and placed in tape and reels, as can be seen in Fig. 5.22(b).

The manufactured ASICs are shown in Fig. 5.23. The ASIC family is formed by the ASICs in Table 5.2. Out of the eight designs, only six designs functioned, Designs 1 to 6. Designs 7 and 8 which had the networking control circuit, and held the highest risk couldn't get programmed. The six remaining, mixed-signal designs, initially formed as a contingency plan, now can provide additional flexibility and cater to various MSF designs. This is because each ASIC version is optimized for a nominal center frequency and with a different tunable impedance range. The chips' footprint and pin allocation can be found in the Fig. 5.20. At the top side of the

chips, the numbers indicate the design (1-6) (Fig. 5.23(a) to Fig. 5.23(f)) and the wafer number (01-12). Fig. 5.23 shows chips from wafer number 02.

5.4 Experimental Results

The performance and properties of the ASICs are divided into two parts, since the RF circuits and asynchronous digital circuits require different test-setups and experiments to extract their performances. The performance achieved from the RF LEs is described and then the performance achieved from the asynchronous digital control circuit and the DACs is presented.

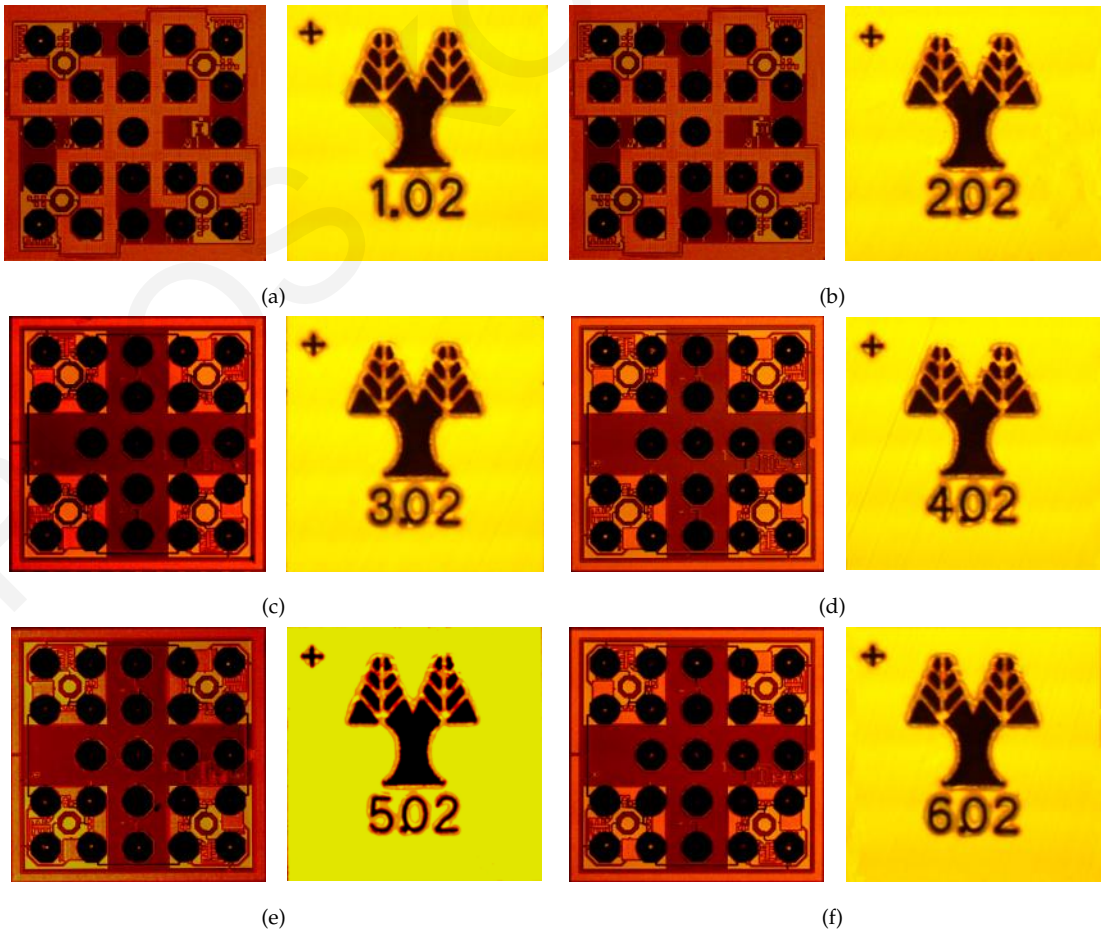


Figure 5.23: Microphotographs of the ASIC chip family for PMSFs, showing both top and bottom sides. The ASICs use wafer-level-chip-scale package (WLCSP) [132] technology, where the solder-bumps (seen on the bottom side) are directly placed on the I/O pads of a redistribution layer beneath the wafer.

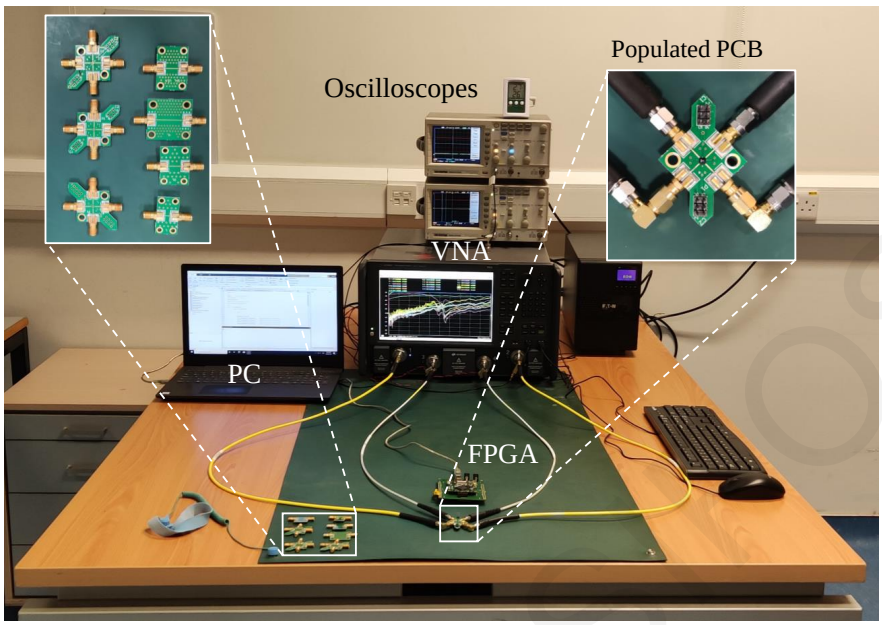


Figure 5.24: Loading element (LE) measurement setup. The PC on the left side of the image, calculates and sends the configuration settings to the populated PCB, which includes the ASIC under test, through an FPGA interface board. To extract the RF characteristics of the chip, as shown on the populated board in the top right inset, the de-embedding boards, shown in the top left inset, are used to characterize and eliminate the effects of all lines leading up to the chip's solder bumps. The S-parameters are captured on the 4-port VNA and afterwards the real and imaginary part of the impedance is calculated.

5.4.1 RF Characteristics

The performance of the RF LEs was evaluated with the test-setup shown in Fig. 5.24 and the results are presented in Fig. 5.25. The ASICs were populated on PCBs with a high frequency substrate (Rogers RO4350) and 50 Ω CPWG TLs connect the LEs to the coaxial connectors at the edge of the PCB. A Keysight N5227B four port VNA was used to acquire the scattering parameters in touchstone file format. A MATLAB script was used to control the VNA and to simultaneously program the ASIC through a field programmable gate array Opal Kelly XEM6010. The measurements were performed at room temperature. The touchstone files are de-embedded with the TRL technique described in Section 2.3.1.5. The de-embedded measured data can be seen in Fig. 5.25 for all six functioning designs. In the same figure, for all the designs the perimeter of the loading element range can be seen in dashed red at the design frequency and sample points are plotted with black dots inside the perimeter. Furthermore, measurements for the four corners of the range are plotted from 2 to 6 GHz.

The LE design methodology was reported in Section 3.3.1([22]), but these measurements were taken by directly probing the structures on-chip, and do not include the parasitics of routing to the chip corners as well as the WLCSP parasitics. Furthermore, the previously presented measurements used external supplies to bias the LEs whereas in Fig. 5.25 the adaptive bias is generated from on-chip DACs, with no external supply. The resistance and capacitance values of the LEs are tuned with the DAC output voltages V_R (real impedance bias) and V_C (imaginary impedance bias), respectively, as shown in the ASIC architecture of Fig. 5.2. The measured impedance responses of the LEs for the entire family of chips are shown in Fig. 5.25 on Smith charts. Note that each chip was optimized for a different operating regime. The designs have a wide operating frequency from 2 to 6 GHz, and in this work, representative results are presented for five frequencies within this frequency range. Designs 1,2,5 and 6 have a center frequency of 5 GHz, while Designs 3 and 4 have a center frequency of 3 GHz. At the center frequency, an area on the Smith chart is outlined, where the loading element can be operated. This area is formed by controlling the input code of the two DACs that bias the loading element at the V_R and V_C nodes. The measured perimeter is plotted with a dashed red line at the center frequency. Sample points are also plotted at the center frequency to illustrate the ability to obtain intermediate states in the plotted area.

5.4.2 Digital Control Circuitry Characteristics

Although the author didn't contribute to the design nor the characterisation of the digital control circuitry and the DACs, a summary of the characterisation is added for completion in this section. The key measurements can be found in Table 5.4. For more information on the characterisation of the control circuit one can see [114, 135].

The configuration of the ASICs can be achieved using an external digital device e.g. an FPGA or microprocessor. However, the digital device can either be removed or entered into sleep mode once the configuration of the ASICs is completed, since the data are stored in the memory cells of the control circuit, in this case the 64 bit shift register. Thus, the power consumption of the digital device is not considered part of the static consumption of a PMSF system that utilizes the proposed ASIC architecture.

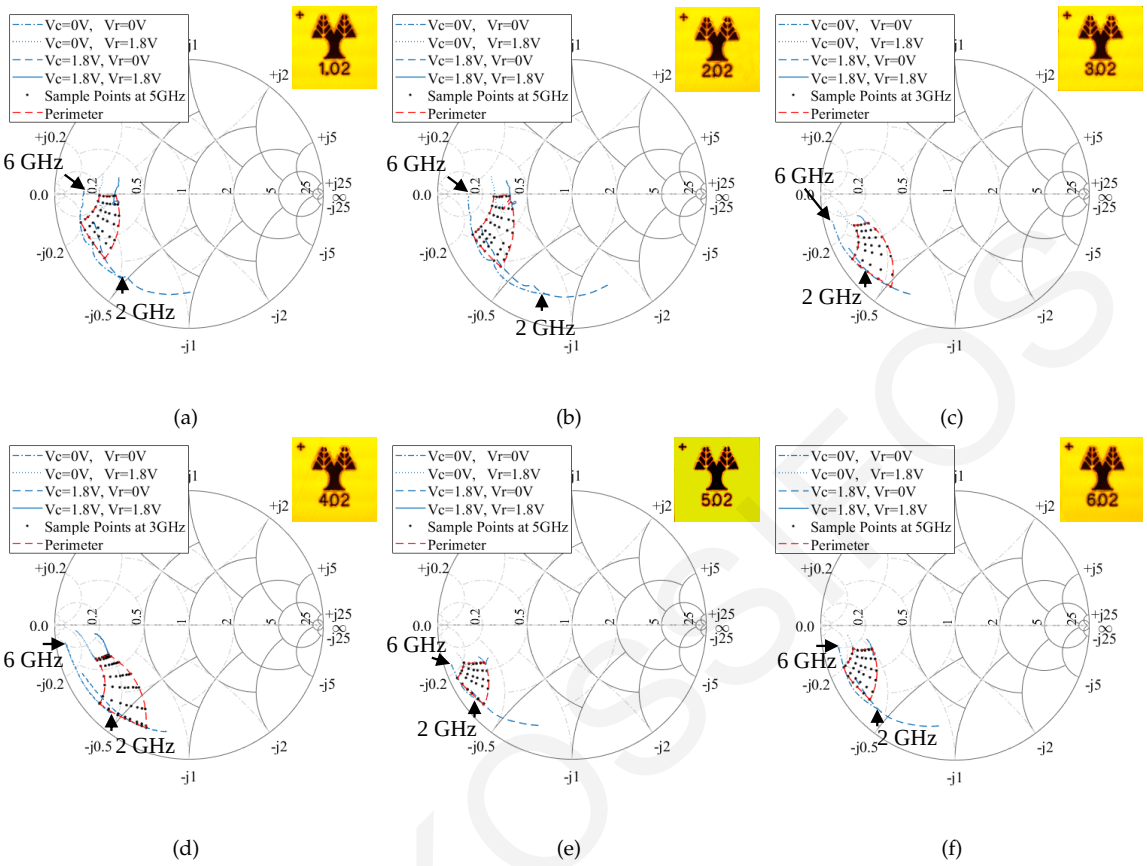


Figure 5.25: Smith chart plots of the de-embedded measured impedance responses of the LEs for each of the six ASIC designs. The different ranges of impedances for each ASIC can be observed for bias voltages ranging from $0 < V_C < 1.8$ V and $0 < V_R < 1.8$ V. The red dashed line delineates the perimeter of the measured impedances at the design frequency for all bias levels, indicating wide and varying realized impedance ranges.

The test-setup consists of a PC and an FPGA to prepare and send the data-packets to the chips, and an oscilloscope to visualize the results. The chips are powered using a reliable source-measure-unit (SMU) device, to facilitate average power consumption measurements. Each control circuit has sixty-four memory cells connected in a series configuration, and has eight cells allocated per DAC. Thus, the packet length is sixty-four bits and the total number of individual states available per chip is 2^{64}. Neighbouring chips communicate via handshake and respect the 4-phase dual-rail asynchronous protocol, whereby each bit is represented by two signals ('data.true' and 'data.false') and there is also the acknowledge signal ('data.ack') which declares the end of each cycle. A detailed explanation of the 4-phase dual-rail protocol can be found in [99, 114]. Due to the 4-phase dual-rail asynchronous nature of the circuits, the ASIC's configuration time is not dependent on the data packet content, i.e. the cycle time is independent of the binary sequence

Table 5.4: Characteristics for the proposed MSF ASICs.

Technology	180 nm CMOS Mixed-Signal RF 1P6M
Supply Voltage (core and IO)	1.8 V
Die Size	4.84 mm^2
Package Type	WLCSP
Number of memory cells	64
Bit Rate	68 MBits/s
Energy Consumption per Bit	79 pJ/bit
Packet Frequency	1 MHz
Energy Consumption per Packet	5.1 nJ/packet
Static Power Consumption	328 μW
DAC range	0-1.793V
DAC resolution	7 mV/bit

transmitted or received. The average configuration time per chip is measured to be 1 μs. During this time, in the channel, 64 bits are exchanged between the sender circuit and the receiver circuit and both circuits are ready for the next packet. To exchange one bit between two ASICs, the average required time is 14 ns, thus the bit rate of the ASIC is 68 MBits/s. The static power consumption of the ASIC is 328 μW. The energy per bit consumed by one ASIC is 79 pJ/bit and the energy consumed per ASIC reconfiguration is 5.1 nJ/packet considering the delays of the buffer stages and the PCB tracks between the chips. Note that the power consumption could have been less but the ASIC design consists of four impedance LEs with eight DACs (main power contributors) and thus it can set the impedance of up to four unit cells. Our DAC design is based on a two-stage resistor string architecture, with a resolution of eight bits. The advantages of this DAC type are its accuracy, monotonicity, and its small layout. Also, it can be directly connected to the LEs since its output impedance is much lower than the controlling input impedance of the varistors and varactors. The ASIC's measured performance and characteristics are summarized in Table 5.4. The static power consumption is mainly attributed to the DACs, whereas the dynamic consumption is dependent on the reconfiguration frequency, hence characterised as energy consumption per packet.

5.5 Discussion

The presented family of ASICs is expected to drive a new generation of PMSFs that can be incorporated into future telecommunications systems, but which can also be retrofitted into current systems. In the programmable telecommunication environment presented in [38], MSFs are used to improve the throughput and the security of indoor telecommunication systems. Outdoor telecommunication systems can be improved in multi-user environments by incorporating MSFs within base stations, thus improving their adaptive multibeam capabilities. The family of ASICs presented in this work is a key component in future MSF-enabled telecommunications systems. Multifunctional performance has been demonstrated by incorporating the proposed ASICs in unit cell structures illustrating their performance in combination with various MSFs [22, 43, 44]. With the advanced capability of tuning both the amplitude and phase of the reflection coefficient, the representative designs are able to perfectly absorb an incident wave up to oblique angles of incidence for both transverse electric and transverse magnetic polarizations. This has been further extended [22] to absorb both polarizations simultaneously and independently. Anomalous reflection and polarization rotation were also demonstrated [95, 107], but even as is, these functionalities are only a fraction of what the ASIC-equipped programmable MSF can achieve. By controlling the amplitude and phase of each unit cell at a subwavelength scale, more complex functions of the MSF design can be achieved, such as multi-beam patterns, absorption from one direction while reflecting in another, fine control of polarization, and non-linear reflection. For example, multi-beam or even arbitrary beam shaping to suit the needs of a telecommunication system in a multi-user and multi-objective environment could be achieved. Also, the advanced functionalities of such MSFs can be adopted in reduced RCS applications, stealth technology, and even cloaking. Furthermore, PMSFs find applications in holography, which use the amplitude and phase programmability which they can provide.

The functionalities described in the literature, control the MSF in two dimensions, engaging only amplitude and phase control with a slow or static operation. The family of ASICs presented herein utilizes fast asynchronous control circuits, which is also robust and reliable. Thus, the PMSFs that use these ASICs can quickly and accurately reconfigure their amplitude and phase response in time. For example, for a series of 100 chips used in a typical MSF, the programming time would

be approximately 100 μs, which also incorporates the time delay of the high-speed communication lines that connect the ASICs. Assuming there are four patches connected to each chip, this time can be translated into the time required to configure 400 metal-patches of a MSF, each with individual settings. This ability is particularly useful, since modulation of arbitrary beam-shaping can be obtained, and thus the MSF can control not only the propagation of electromagnetic energy within its environment, but also the information that the electromagnetic wave contains.

Programmable MSFs are expected to reciprocally co-evolve with telecommunication systems in the near future. Similarly, the ASICs presented are expected to evolve to satisfy the growing need for low-power and low-cost electronics tailored for PMSFs. The MSF trend will require that future ASICs operate even faster and with wider programmable loading element ranges. Thus, technologies with smaller features are expected to be used in order to reduce the size of the chips and to increase their speed. Additionally, more exotic technologies that include memristors and/or micro-electromechanical switches will be utilized in the LEs to increase their range. Furthermore, as SiGe and GaAs technologies become more affordable they will find their way into future ASICs for MSFs.

5.6 Conclusion

A family of low-cost, low-power, high-speed and scalable ASICs for complex impedance adaptation at microwave frequencies has been developed. The ASICs can communicate on MSFs and can be programmed via software to control the complex impedance of each loading element in time and in space. This can be translated into a variation of the amplitude and phase response of both the reflected and transmitted waves, for both TE and TM polarizations on a MSF, due to the multi-bit resolution of the LEs in each ASIC. Furthermore, each unit cell can be individually addressed, without interfering with the incoming electromagnetic waves because of the asynchronous operation of the control circuit, which leads to low electromagnetic noise emissions. Even with these additional functionalities, each member of the ASIC family consumes only microwatts in its static operation. The performance of the chips highlights the potential of using ASICs for realizing PMSFs. This work is a step towards the development of real-time PMSFs that can be integrated into indoor/outdoor telecommunication systems. It also paves the way for the development

of MSFs for use in extraordinary applications that previously seemed infeasible, such as cloaking of not only static but also moving objects, moving holograms, dynamic manipulation of incoming signals and many more.

Chapter 6

ASIC Enabled Programmable Metasurfaces: Design and Characterization

A multifunctional and reconfigurable PMSF is presented in this chapter that is enabled by an ASIC. The enabling ASIC integrates control, digital-to-analog converters (DACs) and loading elements (LEs) to programmatically alter the response of the PMSF unit cells, while minimizing power consumption and cost. These programmable unit cells subsequently comprise a larger PMSF, which provides control of the reflected magnitude and phase for a given incident wave for both transverse electric (TE) and transverse magnetic (TM) polarizations. With this ability, the reflected wave can be set to zero, and both polarizations can be perfectly absorbed simultaneously and independently up to oblique angles of incidence of 60° for TE polarization, and 70° for TM polarization. The PMSF builds upon the work in Chapter 4 and uses the ASICs presented in Chapter 5 to realise a PMSF that finds applications in smart wireless environments by providing the capability to redirect incident waves in a programmable manner, while also enabling the perfect absorption of incident interfering waves and programmatically synthesizing complex and polarization agile wavefronts. The next chapter (Chapter 7) focuses on the wavefront synthesis and performance of this design while here, in this chapter, the design and characterization are presented.

6.1 Introduction

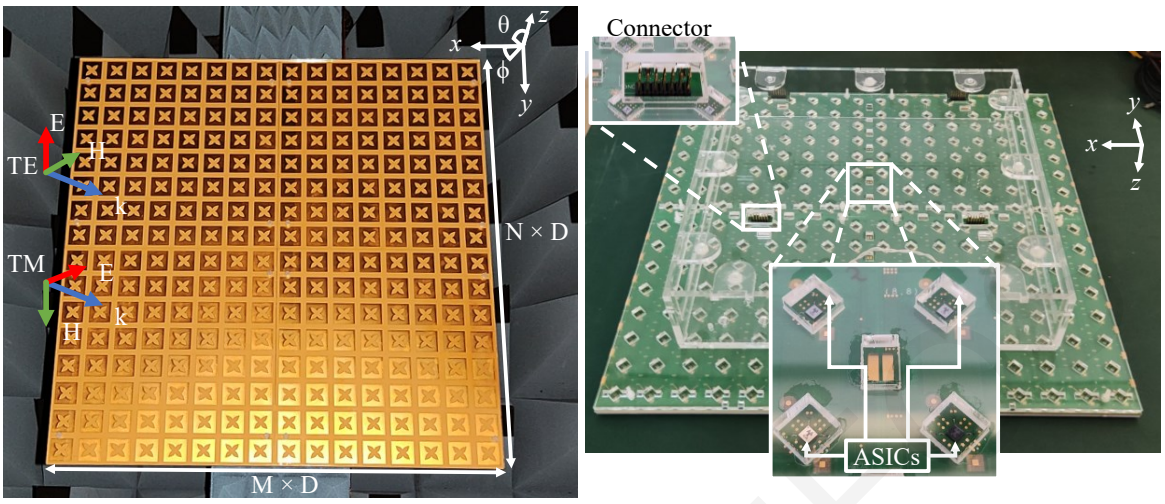
MSFs, which are two-dimensional versions of metamaterials (MTMs) have been gaining attention recently due to their novel abilities and low profiles, which make them an attractive solution for many wireless applications. The two main novel abilities that MSFs have demonstrated are perfect absorption [85,123] and anomalous reflection [12, 83, 124].

Perfect absorption is obtained by matching the surface impedance of the MSF to the incident wave's impedance. The surface impedance for perfect absorption in this case should be equal in all the unit cells. Anomalous reflection is obtained by creating a gradient of surface impedances along the MSF. Similar to anomalous-reflection MSFs, coding MSFs set the individual surface impedance of each unit cell to obtain multiple reflected beams with different polarization [89] and spin [112] control.

In order to introduce a tunable response, MSF designs have incorporated tunable elements in the unit cell. Numerous electrically-tunable MSFs have been shown, including the use of varactors [20, 21, 87], complex impedance tunable integrated elements [22], liquid crystals [23], piezo-electric actuators [136], and more recently utilizing graphene [24–26]. Numerous means of obtaining a tunable MSF behaviour have been shown in [27], while magnetic tunability has been shown in [28], and optically tunable behaviour has been shown in [29]. Optically tunable behaviour has also been shown by utilizing the optical properties of PDR1A [30], which has been shown to possess a memory effect [31].

By controlling the MSF through software, PMSFs have been demonstrated in [32–37]. Using this control method, each unit cell has been programmed to obtain multiple reconfigurable functions, such as polarization, scattering and focusing control [32], holography [33, 34], non-linear harmonics control [35], machine learning imaging [36], and frequency recognition for self-adaptivity [37].

These PMSFs are often found in the literature as reconfigurable intelligent surfaces (RISs) or intelligent reflective surfaces (IRSs). PMSFs and their aforementioned advanced electromagnetic manipulation capabilities, have provided the potential to greatly improve wireless telecommunications through the smart radio environment reconfiguration paradigms [38–42] and have increased the capabilities and agility of antenna applications [43–47].



(a) (b)

Figure 6.1: Manufactured programmable metasurface (PMSF) prototype with a design frequency of 3.6 GHz. (a) Top view, and (b) bottom view showing the application-specific integrated circuits (ASICs) populated on the PMSF.

The employment of PMSFs in a radio environment finds contrast with traditional wireless telecommunications systems, where the effect of the terrain or structural environment is simply accounted for by the transmitter and receiver. By operating a PMSF in a radio environment the parameters of the channel can also be partially controlled. PMSFs operated in this manner have shown promise in improving multiple aspects of wireless telecommunications, such as increased reliability, energy efficiency and security [38–42, 48–50].

A PMSF can be retrofitted in current telecommunication systems by illuminating it within the Fraunhofer region from a passive directive antenna, such as a rectangular horn antenna. This combination of passive antenna and PMSF now can programmatically alter the overall radiating pattern [43–45, 50, 51]. Even though that this concept is not new and has been implemented previously using traditional transmit-arrays and reflect-arrays [52, 53, 137], PMSFs offer in this scenario greater control over the reflected or transmitted wavefront due to their sub-wavelength unit cell size.

The current state of PMSFs, which don't utilize the architecture presented in Chapter 3 and Chapter 4, rely COTS components, such as varactor diodes, PIN diodes and external FPGAs. Subsequently their cost and power consumption is impacted [32–37]. Each unit cell of these PMSF is equipped with a minimum of one lumped diode which enables their tunability. Due to the large number of unit

cells the power requirements are significant to bias all the diodes, not to mention the power required to bias the FPGA. DACs are used to provide more discrete states to each unit cell, with the compromise of further increased power consumption. The implementation of the feeding networks to each unit cell is a challenging process and requires additional FPGAs as the size is scaled up. Furthermore, the programmable approaches outlined in [32–37] only control the phase response of the unit cell for a single polarization. Controlling the phase and magnitude of the unit cell for both polarizations with off-the-shelf components such as FPGAs, diodes and DACs increases further the complexity of the feeding networks, power consumption and overall cost of the PMSF [54].

In this chapter, the limitations of the past PMSF architectures are tackled with a new architecture that finds contrast to conventional FPGA-based PMSFs [32–37, 54, 137, 138], since it integrates complex impedance MSF LEs, DACs and digital control locally within each unit cell. This is done by co-engineering the ASIC with the electromagnetic response of the unit cell. This work uses the ASICs reported in [114] while refining the ASIC's measurements, and significantly expands the initial PMSF design reported in [22], to produce a low power, low cost, reliable, and scalable standalone unit that doesn't require external costly and power hungry FPGAs and DAC modules. The ASICs were populated on the back of the PMSF and were used to provide a complex impedance in a programmable manner, for the independent absorption of both TE and TM polarized waves. This enabled the PMSF to perfectly absorb waves with multiple polarizations at both normal and oblique angles of incidence. In this work, it is further demonstrated how this PMSF design can perform additional multiple functions that aim to target future programmable wireless environment applications, programmable antennas, multi-user base-station, holography, imaging and wireless applications [92, 94, 139, 140].

This work is broken into two self-contained chapters, this first chapter (Chapter 6,[141]) which focuses on the design and characterization of the PMSF, and a second chapter, (Chapter 7,[142]), which focuses on the applications of the presented PMSF. This chapter is organized into the following four sections. In Section 6.2 the PMSF architecture and the unit cell geometry are presented. In Section 6.2.2 the RF performance of the ASIC is experimentally verified with an innovative de-embedding method. Finally, the PMSF performance and experimental verification that it can control the magnitude and phase of both TE and TM polarizations is

summarized in Section 6.4, which is followed by the Conclusion.

6.2 Metasurface Design

The design in this work consists of a PMSF with M × N unit cells, as shown in Fig. 6.1. The unit cell design was introduced in [22] and Chapter 4. The design consists of four exponentially tapered lines that form a cross shape. The corners of the exponential tapers have been merged to form a square ring. The thin edges of the exponential tapers are loaded with an ASIC on the bottom layer of the PCB as shown in Fig. 6.1(b). The ASIC consists of four LEs, and can programmatically load each unit cell with a variable complex impedance in order to achieve independent and simultaneous control of the absorption for both TE and TM polarizations. Perfect absorption was demonstrated in simulation for angles of incidence up to 60° [22]. This current design is optimized to control the magnitude and phase of the reflection coefficient of both polarizations (TE and TM) for a wide range of incidence angles θ in the elevation plane, while keeping the azimuthal angle ϕ fixed at $\phi = 0°$ (see Fig. 6.1(a)). Additionally, the design takes into account the physical layout of the ASIC, its measured response, and all the PCB metallization details.

6.2.1 Unit Cell Geometry

The details of the unit cell geometry can be seen in Fig. 6.2, while the geometric parameters of the unit cell can be found in Table 6.1. In Fig. 6.2(a) a three-dimensional view of the unit cell is shown. The four exponential tapers are located on the top layer (L_1) and are at a distance H_1 from the ground-plane layer (L_2). The insert of Fig. 6.2(a) shows a side view, which illustrates all four layers of the unit cell. The bottom layer (L_4) is where the ASIC is positioned, while an additional layer (L_3) is used for signal routing. The top layer (L_1) is connected to the bottom layer (L_4) with through-vias, as shown in Fig. 6.2(a). The unit cell was built on a Panasonic Megtron 6 substrate with a nominal dielectric constant (ε_r) equal to 3.49 and a loss tangent (tan δ) equal to 0.003. The four exponential tapers extend from a metallic square ring with a width of W_A, located at the perimeter of the unit cell at a distance G from the unit cell's edge. The terminating width of the exponential taper is equal to T_B. The unit cell was simulated in primary/secondary boundary conditions, and

excited with a Floquet port in ANSYS's HFSS software. The unit cell's geometric parameters were optimized for wide angle perfect absorption, as well as magnitude and phase control, at the design frequency of 3.6 GHz. The design frequency was chosen within the sub-6 GHz 5G band, as to permit later experimentation with 5G signals.

The bottom view of the unit cell is shown in Fig. 6.2(b). Around the ASIC, a ground metallization with a width of S_W was placed on L_4 and L_3. This metallization is connected using vias to L_2, which serve as a ground and shield to the RF terminals at the edges of the ASIC. Openings on this metallization were placed to allow routing of the global biasing and communication lines, which are connected to the corresponding pins at the center of the ASIC. The global 1.8 V biasing line in the manufactured prototype is connected to an L_3 metallic layer layer which is poured in the layout. The ASIC's communication lines use an asynchronous scheme and are routed on L_4. The communication connectivity of the ASICs enables them to connect with each other and occupy any arbitrary shape by routing the communication between ASICs. More information can be found in Chapter 5 ([114, 135]).

A close-up view of the ASIC's footprint is shown in the top-right insert of Fig. 6.2(b). The ASIC has a pitch of IC_P, and each pad has a diameter of IC_B. Each exponential taper was terminated through a GSG connection to the four corners of

Table 6.1: Unit cell's geometric parameters.

Geometric Parameter	Dimension (mm)	Description
H_1	1.86	Top substrate thickness
H_2	0.20	Bottom substrate thickness
D	25.25	Period of the unit cell
W_A	4.0	Width of square ring
T_B	1.0	Taper width
T_G	6.5	Distance between tapers
G	2.65	Taper gap
G_W	0.2	Ground cut width
S_W	7.5	Shield width
IC_P	0.4	ASIC pitch
IC_B	0.25	ASIC pad diameter

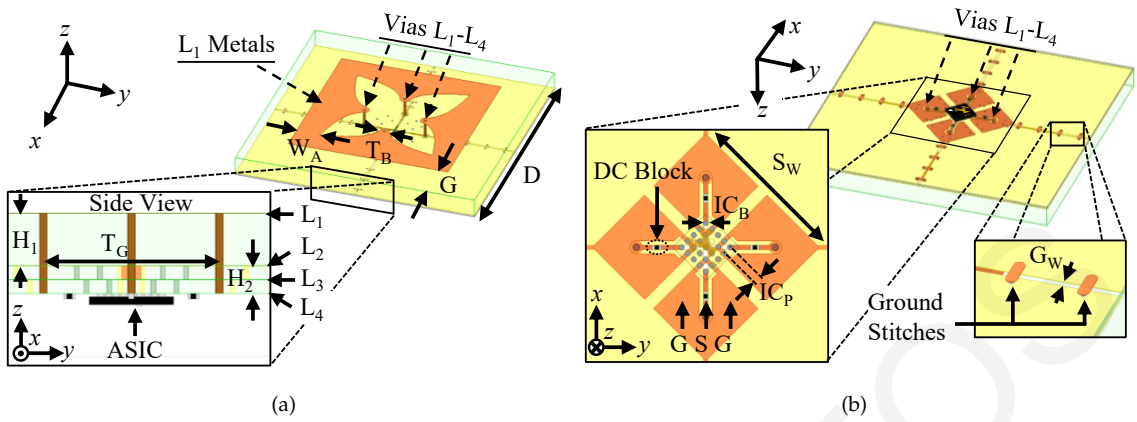


Figure 6.2: PMSF unit cell geometry. (a) 3D view with side-view insert, indicating the PCB layers and ASIC location. (b) Bottom view with two inserts, one showing the ASIC footprint and the second showing the ground stitches.

the ASIC. The GSG connection offers a reflection-less termination to the internal LEs of the ASICs. High quality-factor capacitors (Murata, GJM0225C1E100JB01) were placed on the signal track to DC-block the four LEs. In order to reduce the PCB warping from the different expansion coefficients of the substrate (Megtron 6) and the solid copper ground layer (L_2), a cut (G_W) was inserted on L_2. To ensure that L_2 functions effectively as a ground plane, ground stitches were added across the cut G_W, as shown in the bottom-right insert of Fig. 6.2(b). Even though a minimum of three ground stitches was found to have identical simulated results with a solid ground plane, four stitches were used to ensure a good ground connection.

6.2.2 Metasurface Loading ASIC

The PMSF loading ASIC architecture was first reported in Chapter 3 [107] and was used to obtain a family of different footprints and complex impedance ranges in Chapter 5 [114]. The ASIC's microphotograph is overlaid with its architecture and can be found in Fig. 6.3. The architecture consists of asynchronous control circuits [135] and eight DAC that are used to bias all four LEs within the ASIC. The control circuit is essentially an asynchronous shift register. This shift register is 64 bits in length, and provides the inputs to all eight DAC, which are 8-bits each ([107, 114, 135]).

The four LEs (LE_1-LE_4) shown in the architecture diagram in Fig. 6.3, are identical but can be programmatically biased independently. This means that the biasing voltages (V_{R1}, V_{C1}) of LE_1 and any other LE can be set to any value between ground

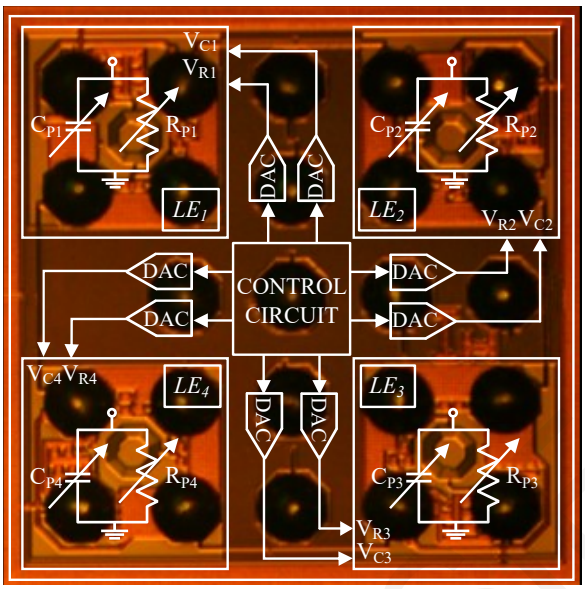


Figure 6.3: Microphotograph of the bottom side of ASIC Design 4.02 with the overlaid architecture. Large top-metal structures of the chip, such as inductors, can be seen between solder-bumps. The digital control circuitry is hidden behind metal-shielding layers.

and the supply voltage with an 8-bit resolution. The circuit schematic of the LEs is represented in Fig. 6.3 as a simple tunable parallel *RC* connection. The layout of the LEs reported in [22] was specifically designed for on-wafer measurements, while in this work the layout of the LEs was adapted to the footprint of the Design 4 ASIC (see Fig. 5.20). Layouts of all the designs (Design 1-6) in Chapter 5 [114], including Design 4, were adapted for a WLCSP with the pitch and ASIC pad dimensions shown in Table 6.1. WLCSP minimizes layout parasitics, while reducing the cost. Small additional package and layout parasitics attributed to the WLCSP process were adjusted by small modifications to the LE varactors. In Fig. 6.4 the orientation of the LEs is shown along with a close-up view of the Design 4 layout in the inset. In the inset the inductor can be clearly seen, as it is placed within a wide ground metal and the solder balls that surround the LE, indicated in the figure by the letter G. The varactor and varistor are placed in close proximity to the signal pad, indicated by the letter S.

The LE layout was designed in CADENCE VIRTUOSO using a commercially available 180 nm technology. The layout was imported into Keysight's ADS to be simulated in Momentum. All passive components' responses were validated with the models of the process design kit (PDK), and the active components' models were exported using a Touchstone file format, which were used in a co-simulation with the passive components.

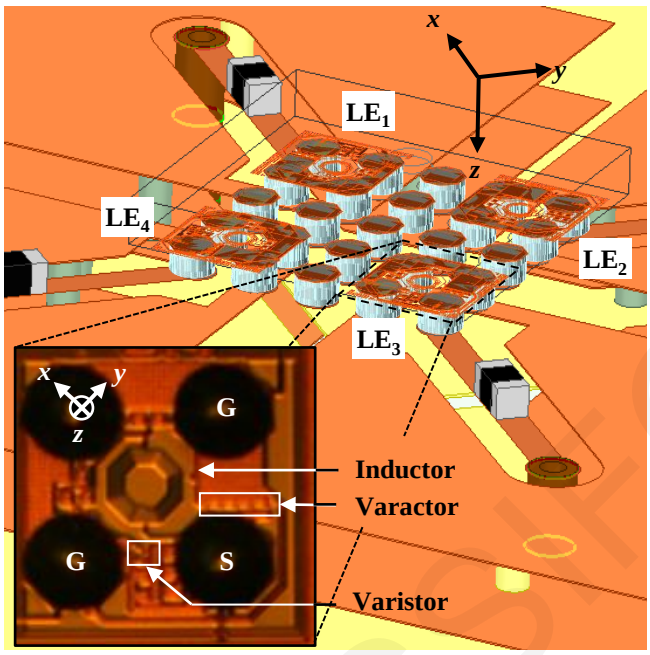


Figure 6.4: 3D view of the application specific integrated circuit (ASIC) located on L_4. The ASIC contains four loading elements (LEs). Silicon removed for clarity. The inset microphotograph shows the bottom view of one of the LEs, indicating the locations of the main components.

6.2.3 ASIC Measurement

As described in Chapter 5, the ASIC was manufactured using a commercially available 180 nm technology, which was post-processed with extra layers at a wafer-level, so as to place solder balls with diameter 240 μm on the actual die, i.e. WLCSP. In order to measure the performance of the WLCSP ASICs, these were populated on custom-designed PCBs consisting of four high frequency substrates (Rogers 4350B). On each PCB four 50 Ω CPWG transmission lines connect the four SMA connectors to the four RF terminals of the ASIC. The populated PCB can be seen in the top-right inset of Fig. 6.5. In this figure the microwave measurement set-up for the ASIC is shown. The measurements were automated using a MATLAB script that controlled the ASIC though the use of an FPGA board, and the VNA that collected the S-parameter files. Two oscilloscopes were used to monitor the voltages that bias the varactors of the four LEs through four bias tees.

6.2.4 De-embedding method

The equivalent circuit of the populated PCB can be seen in Fig. 6.6. In order to remove the connector (Con.) and transmission line (TL) effects, both are characterized using the two-length method and are de-embedded (Section 2.3.1.4, [64]).

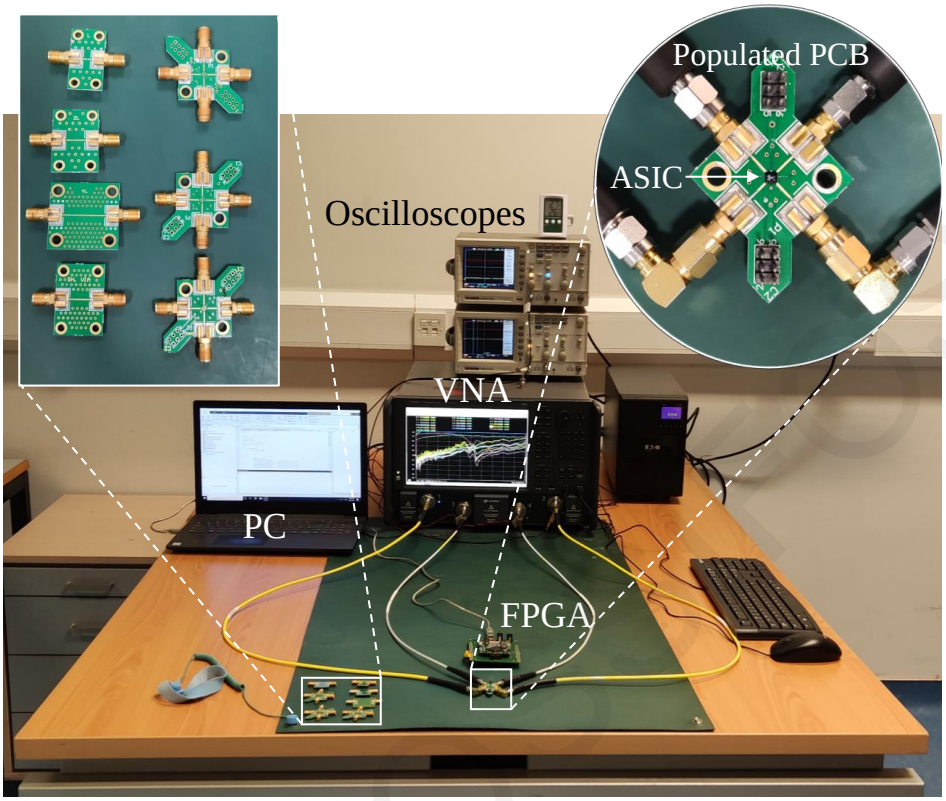


Figure 6.5: Measurement set-up for ASIC's *RC* range.

All the de-embedding structures can be seen in the top-left inset of Fig. 6.5. The shunt Y_a matrix around the ASIC is measured using an open de-embedding board and removed. The series Z_a components are primarily caused by the vias leading to ground below the ground pads of the ASIC. These ground connections, are measured and de-embedded using a short de-embedding board. It should be noted that the solder balls of the ASIC are not de-embedded in this procedure.

The ASIC was sequentially controlled to obtain the measured S-parameter files for a range of varactor and varistor biasing voltages. Then, the measured S-parameter files were de-embedded. The de-embedded results were converted from S-parameters to a parallel-connection *RC* (resistance, capacitance) area [22] at the frequency of 3.6 GHz. The dash-dot line in Fig. 6.7 outlines the *RC* area's perimeter that was obtained. It can be observed that the *RC* area covers a capacitance range from 1.5 pF to 2.8 pF and a resistance range from 15 Ω to 120 Ω. The output power of the VNA was set up to -30dBm, which is significantly higher than the expected power in typical PMSF applications, such as programmable wireless environments and antenna reconfiguration applications. Even so, no degradation of the LE response or heating of the ASIC was observed.

The DACs that bias each varactor and varistor have an 8-bit resolution, which

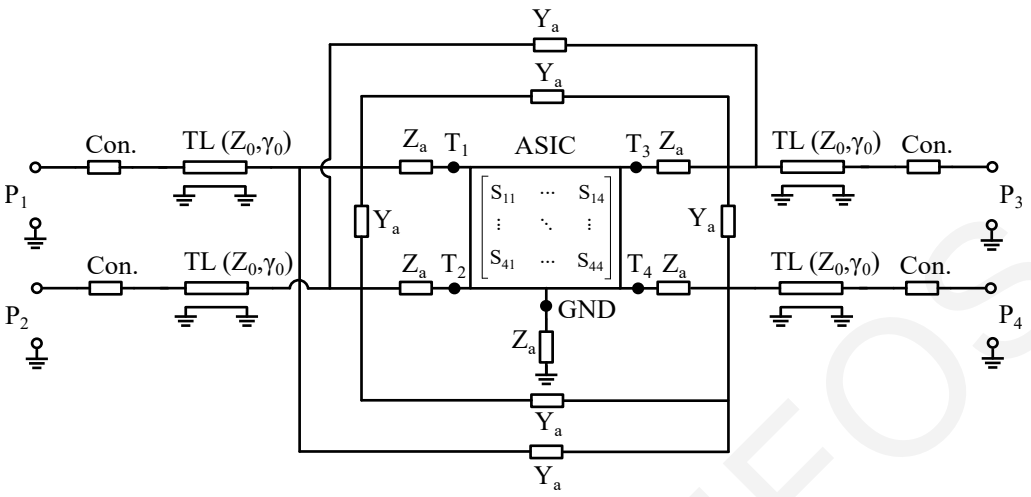


Figure 6.6: Equivalent circuit of the populated PCB. The ASIC is located at the center. The ASIC's response at the frequency of interest is obtained after the response of the connectors (Con.), transmission lines (TLs) and discontinuity effects are de-embedded.

results in the LE having 2^{16} discrete states [107, 114]. This large resolution enables the ASIC to seamlessly program all resistance and capacitance combination values within the *RC* area perimeter. In Fig. 6.7 the optimal *RC* values required to obtain perfect absorption ($|r| \leq$ -30dB) for TM and TE polarizations are plotted for normal and oblique angles of incidence. By optimizing both the *R* and *C* values, the unit cell's surface impedance can perfectly match the incident wave's impedance and obtain a reflection coefficient of at least -60dB in simulation. It can be seen that the *RC* combinations that are needed to obtain perfect absorption fall within the *RC* area that the ASIC can produce from normal incidence up to 70° for TM polarization and

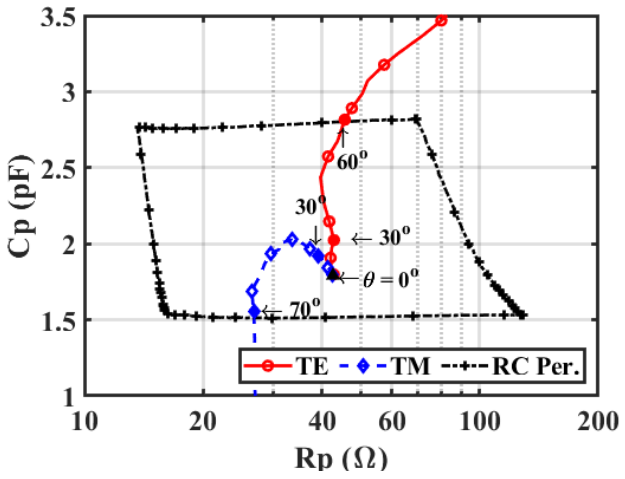


Figure 6.7: Measured parallel-connection *RC* area perimeter for the LEs shown in Fig. 6.4. Optimized LE values for perfect absorption ($|r| \leq$ -30dB) are plotted for both TE and TM polarizations.

Material	Via Through	Blind	Buried	Micro Via	Thick. (µm)	ε_r (4 GHz)	tan(δ)	Resin Contain (%)	Cloth	Layer
Galvanic Cu					25					L_1
Copper					9					
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
68 PPE-R5670(G)					68	3.22	0.003	73	1035	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
250 Megtron 6 R-5675(G)					250	3.63	0.003	54	2116	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
250 Megtron 6 R-5675(G)					250	3.63	0.003	54	2116	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	H_1
250 Megtron 6 R-5675(G)					250	3.63	0.003	54	2116	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
250 Megtron 6 R-5675(G)					250	3.63	0.003	54	2116	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
250 Megtron 6 R-5675(G)					250	3.63	0.003	54	2116	
Copper					17					L_2
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
Galvanic Cu					25					L_3
Copper					9					H_2
68 PPE-R5670(G)					68	3.22	0.003	73	1035	
49 PPE-R5670(G)					49	3.2	0.003	75	1027	
Copper					9					L_4
Galvanic Cu					25					
Bottom Solder Mask										
Bottom Overlay										

Figure 6.8: Detailed PCB stack. The stack also list the dielectric constant (ε_r), dissipation factor (tan(δ)), cloth type and description of each layer.

60° for TE polarization.

6.3 PCB Manufacturability

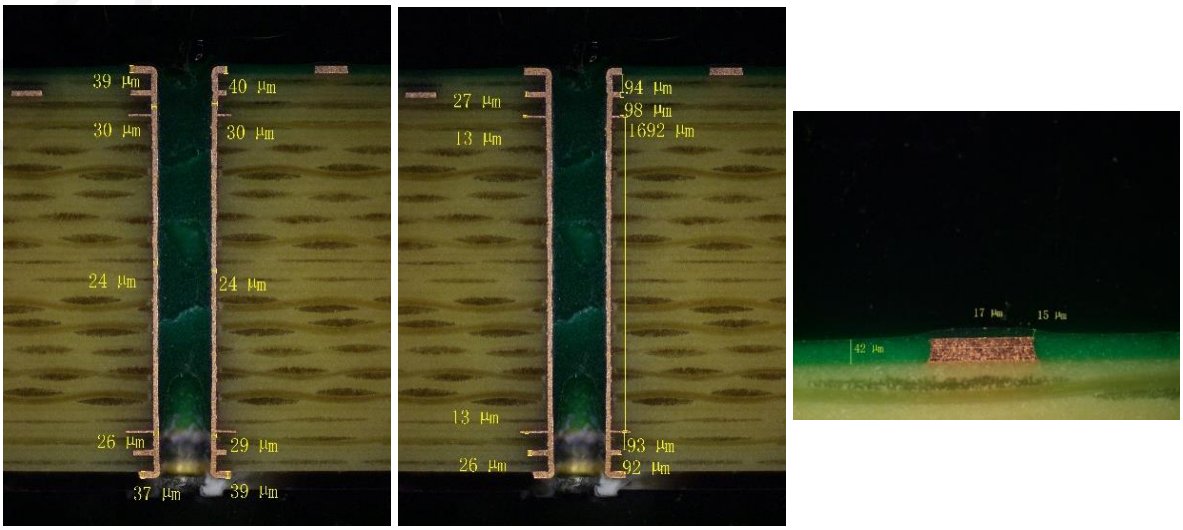
This section describes the PCB production processes. The PCB production aimed toward large scale manufacturing of PMSFs. The PCB stack was demanding, and involved significant difficulties. The PCB's asymmetric layers would have produced warping or twisting due to their different material compossition with different thermal expansion coefficients. These asymmetric layers couldn't be avoided in the produced PMSF design. The PCB stack shown in Fig. 6.8 was chosen which is symmetrically layered but still asymmetric in terms of its metallization. In Fig. 6.8 the stack is shown in detail, each layer's material is shown with its thickness, dielectric constant (ε_r), dissipation factor (tan(δ)), cloth type and description.

Megtron 6 material was used in the PCB, R5675(G) laminate was chosen and stacked with prepreg R5670(G). The distances H_1 and H_2 are shown in Fig. 6.8 as to correlate with the unit cell geometry in Fig. 6.2(a). Each prepreg's cloth style will require different resin percentage, subsequently this combination produces a slightly

different dielectric constant. These layers could be added separately in simulation or be considered a homogeneous material with an average dielectric constant to save simulation time. The average dielectric constant for the dielectric between L_1 and L_2 was calculated to be 3.49 and for L_2 to L_4 3.21.

A cross-sectioned cut of the fabricated PCB was performed, and its dimensions were measured using a microscope. A cross-section of a through via is shown in Fig. 6.9(a) and Fig. 6.9(b), and the measured dimensions are shown in the micro-photographs. In Fig. 6.9(a) the wall thickness of the through via is shown in various locations, demonstrating that they were successfully electroplated. The dielectric thickness of the same through via micro-photograph is shown in Fig. 6.9(b). H_1 was measured to be slightly thicker than expected, 1884 μm (1692+98+94 μm) instead of 1857 μm, which translates into only a 1.5% difference to the nominal H_1 thickness. In Fig. 6.9(c) the solder mask thickness is shown to be 42 μm.

The structural dimensions in this section are useful not only for reassurance that the PCB manufacturing was correct, but also to isolate the cause of a discrepancy between simulations and measurements in the experimental part. As will be presented in the next section, a small frequency shift was found in the measurement which couldn't be justified by a minor PCB geometric variation.



(a) (b) (c)

Figure 6.9: A cross-sections of the fabricated PCB. In (a), a through via conductor wall cross-section is shown. (b) shows measurements of the dielectric thickness and (c) solder mask thickness measurements in a micro-photograph.

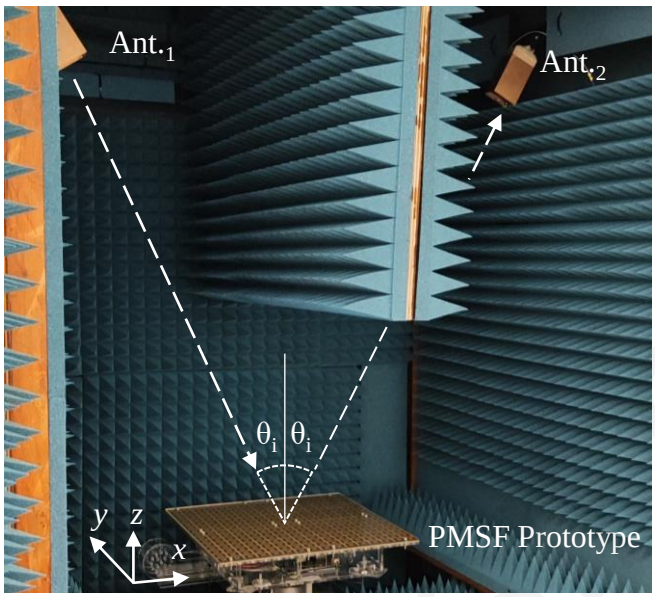
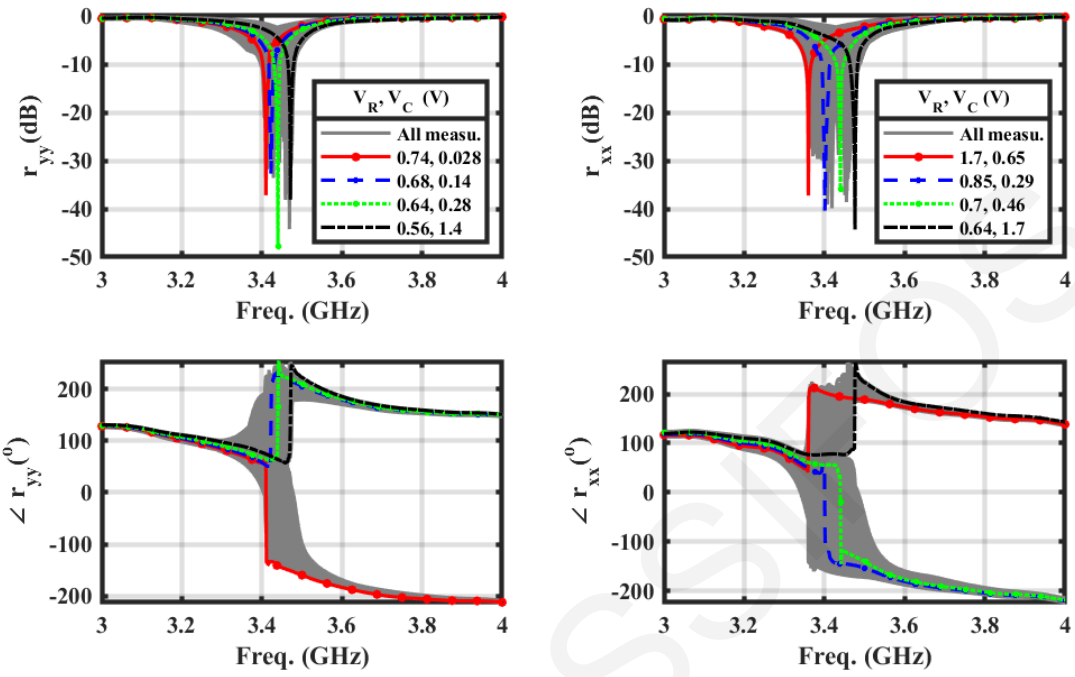


Figure 6.10: PMSF bistatic measurement set-up. Two antennas (Ant.$_1$ and Ant.$_2$) are placed at an angle, while the two ports of a VNA are connected to the antennas. The antennas can be rotated for both TE and TM measurement.

6.4 Experimental Verification

Four 8×8 unit-cell PMSF prototypes were manufactured and assembled to construct a 16×16 unit-cell PMSF, shown in Fig. 6.1. The prototypes occupied a total area of 40.4×40.4 cm^2, i.e. 4.85×4.85 wavelengths^2 at 3.6 GHz. This size was chosen as to be easily measured in free space conditions. The design's total static and dynamic power consumption was measured to be 84 mW, which translates into a power consumption by each unit cell of 328 μW. The reconfiguration data to each one of the 8×8 unit-cell PMSF prototypes are serially supplied to their connectors. 64 bits are needed for each ASIC located in each unit cell of the prototype, therefore a total of 4096 bits are needed. In order to convert the serial data from a PC to the asynchronous 1.8 V protocol required by the ASICs, a low power microcontroller was used with a 16 MHz crystal oscillator and bi-directional level shifters. The four 8×8 unit-cell PMSF prototypes can be sequentially connected, as shown in [135], and can occupy arbitrarily large areas, something that can't be achieved with FPGA-based PMSFs. Alternatively, the PMSF prototype can be connected in parallel to be programmed simultaneously. Parallel connectivity was chosen to reduce the total reconfiguration time and to expedite the measurements. The four 8×8 unit-cell PMSF prototypes were connected directly to the low power microcontroller unit and the total reconfiguration time (T_{Tot}) was measured to be approximately equal to



(a) (b)

Figure 6.11: Measured reflection coefficients for an angle of incidence $\theta_i = 27.5°$. (a) TE and (b) TM polarization. Representative measurements are overlaid with their V_R and V_C voltages indicated in the legends.

800 μs. The limiting factor in the reconfiguration time in this scenario is the microcontroller's clock, since the ASIC's minimum reconfiguration time is less than 1 μs when left to operate without a clock, asynchronously in a ring topology [114]. The microcontroller can be set to sleep mode, or it can be even disconnected once the PMSF is reconfigured, and therefore its power consumption can be neglected in the total static power consumption.

The measurement set-up is shown in Fig. 6.10. The PMSF was illuminated at a distance greater than 1 m (11.5 wavelengths) from a transmitting antenna (Ant.$_1$) placed at an angle (θ_i), while the reflected signal was received at the same angle by a receiving antenna (Ant.$_2$). The direct path between the two antennas was blocked with the use of pyramidal absorbers.

The measured S_{21} from the measurement set-up was obtained while sweeping all the varactor and varistor biasing voltages (V_{C1-4} and V_{R1-4}). All the measurements were then compensated using a metallic plate that was placed at the position where the PMSF is measured. After the compensation using the metallic plate the measured S_{21} can be converted to the reflection coefficient for TE (r_{yy}) polarization. All the

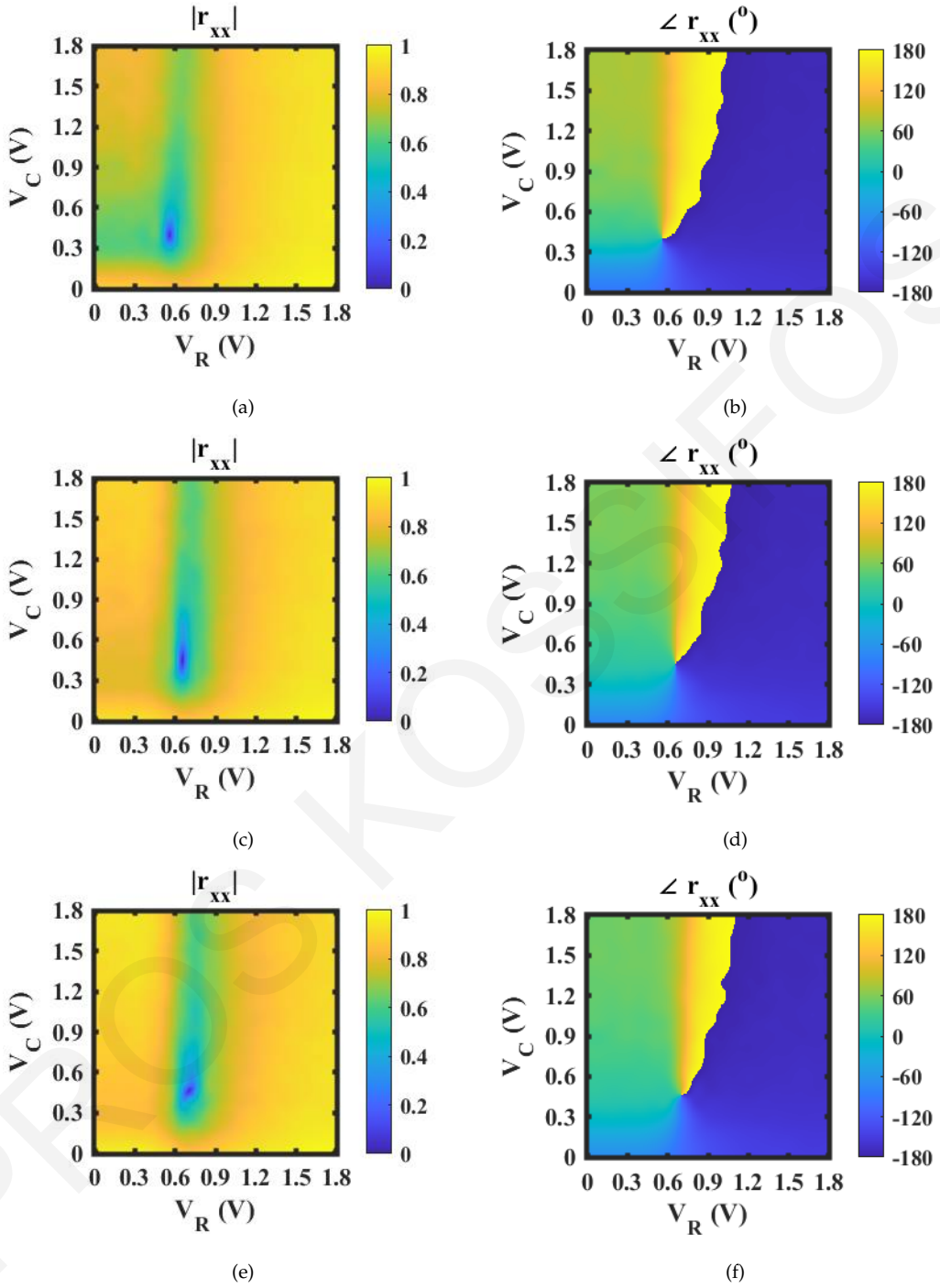


Figure 6.12: Measured TM reflection coefficient magnitude ($|r_{xx}|$) and phase ($\angle r_{xx}$), at 3.44 GHz, for incident angles ranging from $\theta_i = 15°$ to $\theta_i = 27.5°$. (a) magnitude and (b) phase for $\theta_i = 15°$. (c) magnitude and (d) phase for $\theta_i = 20°$. (e) magnitude and (f) phase for $\theta_i = 27.5°$.

measured reflection coefficients for an angle $\theta_i = 27.5°$ can be seen in Fig. 6.11(a), plotted in grey for a frequency bandwidth extending from 3 GHz to 4 GHz. Four representative measurements are also overlaid with different colours, and their V_C and V_R voltages are indicated in the figure's legend.

By rotating the antennas (Ant.$_{1-2}$) by 90° the measurement can be repeated to

obtain the reflection coefficients for TM polarization (r_{xx}). Representative TM polarization reflection coefficient measurements can be seen in Fig. 6.11(b) for a frequency bandwidth also extending from 3 GHz to 4 GHz. From Fig. 6.11(a) and Fig. 6.11(b) one can observe that there is a shift in the operating frequency of the PMSF of roughly 5%. This shift can be attributed to numerous manufacturing and fabrication reasons. The most probable reasons are variations in the electrical properties (dielectric constant and loss tangent) of Megtron 6 rather than its thickness. It is also possible that the acrylic frame that supports the PMSF could also cause this shift, since it is in close proximity to the active metallic structures. Nevertheless, the PMSF can achieve in measurement a reflection coefficient less than −30dB, and therefore can achieve perfect absorption for the TE polarization from 3.41 to 3.48 GHz, while perfect absorption can be achieved for the TM polarization from 3.36 to 3.47 GHz.

For both polarizations, a fine sweep of varistor and varactor voltages was performed for a range of incident angles. In order to speed up the measurement time, not all 2^{16} states of the ASIC were measured, but they were interpolated using the "interp2" MATLAB function. Contour plots of the reflection coefficients are plotted in Fig. 6.12 (TM) and Fig. 6.13 (TE) at 3.44 GHz for every DAC input for angles of incidence (θ_i) equal to 15°, 20° and 27.5°. As can be seen in Fig. 6.12 and Fig. 6.13, for every incident angle, perfect absorption can be achieved for a different V_R and V_C voltage combination, which translates to an RC value implemented by the LEs. For example, for an angle of incidence equal to 27.5° these are V_R = 0.7 V and V_C = 0.46 V (Fig. 6.12(e)) for TM polarization, while for TE polarization these are equal to V_R = 0.64 V and V_C = 0.28 V (Fig. 6.13(e)). Around the perfect absorption point (V_R and V_C), any other V_R and V_C combination will produce a different RC combination implemented by the LEs, which will partially reflect the incident wave with a magnitude and phase difference. This mechanism is what grants the unit cell its magnitude and phase control. The contour plots for both TE and TM show a near perfect magnitude and phase coverage for this angle range, with fine resolution that can be exploited for dual-polarization magnitude and phase wavefront synthesis.

In [22], it was shown that the LEs which are placed along the x axis ($LE_{1,3}$) will tune only the r_{xx} reflection coefficient and the LEs that are placed along the y axis ($LE_{2,4}$), will tune only the r_{yy} reflection coefficient. This ability allows the decomposition of an incident wave which contains both x and y polarized components into its orthogonal polarization components, which can each be addressed separately. By

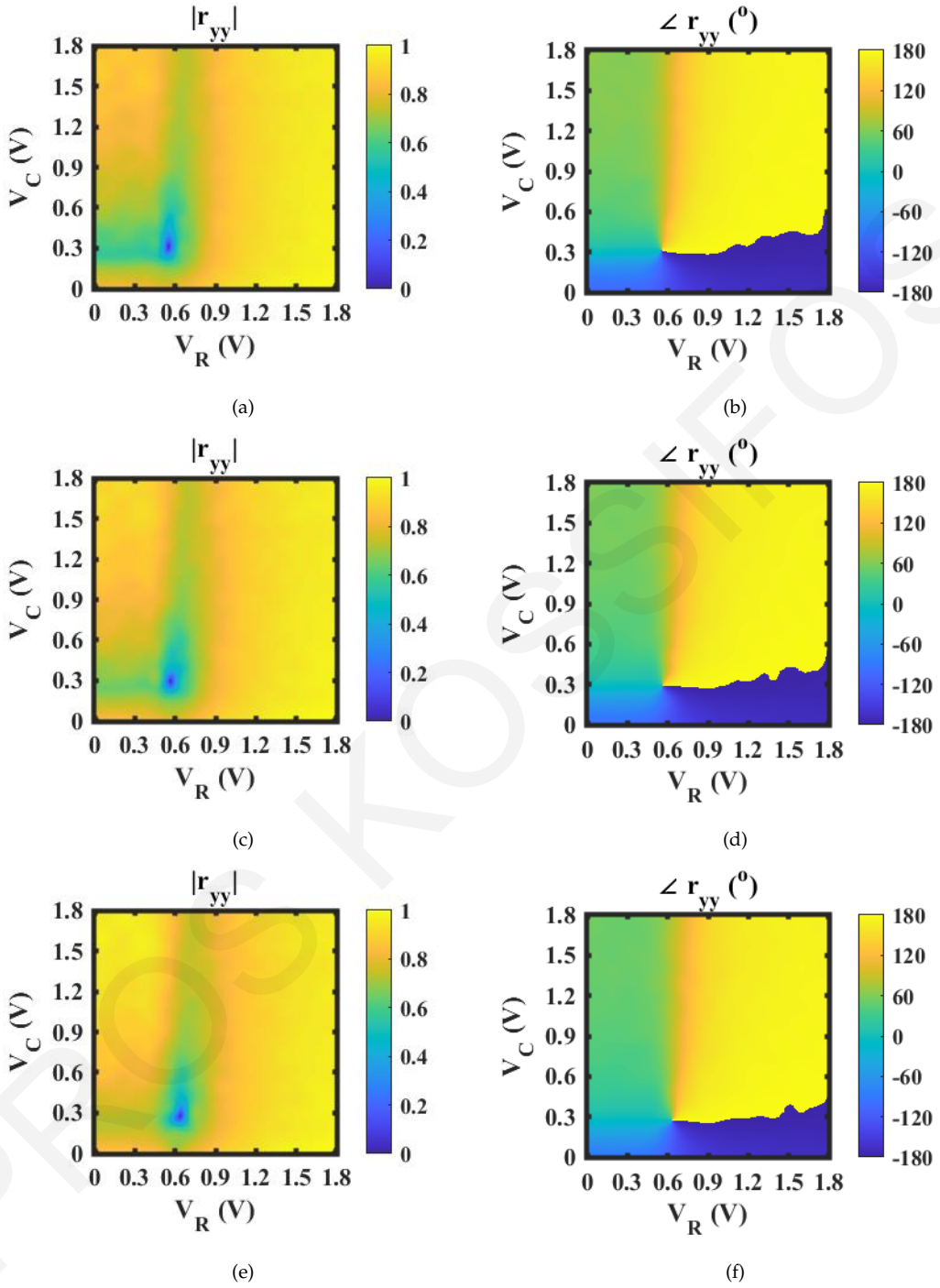


Figure 6.13: Measured TE reflection coefficient magnitude ($|r_{yy}|$) and phase ($\angle r_{yy}$), at 3.44 GHz, for incident angles ranging from $\theta_i = 15°$ to $\theta = 27.5°$. (a) magnitude and (b) phase for $\theta_i = 15°$. (c) magnitude and (d) phase for $\theta_i = 20°$. (e) magnitude and (f) phase for $\theta_i = 27.5°$.

decomposing a wave into its x and y polarized components, one may set r_{xx} or r_{yy} to zero, and perform independent or simultaneous x and y polarization perfect absorption. Furthermore, polarization conversion of an incident wave from LP to CP or vice versa can be achieved together with conversion from LHCP to RHCP. These are just some basic examples of dual polarization magnitude and phase programmability of

the PMSF.

In this chapter, the design methodology of an ASIC-equipped PMSF has been presented and experimentally verified. The experimental verification in this chapter is limited to the global PMSF settings, meaning that all PMSF unit cells are set to the same state. With this PMSF global state, the characterization and operation of the PMSF's unit cells are obtained. The PMSF design can address each unit cell independently and produce complex wavefront patterns. The fully-characterized measured PMSF unit cell's reflection coefficients presented in this work are subsequently used for complex pattern synthesis in Chapter 7. In Chapter 7, the computation time required for multibeam synthesis is also addressed and improved with an innovative synthesis method [142].

Table 6.2: Comparison with dual-polarised reconfigurable PMSFs.

Parameter	**This work**	**[137]**	**[54]**	**[138]**
Total static power consumption (P_T)	**84 mW**	1.9 W	7.2 W	2.5 W
Unit cell static power consumption ($P_U = P_T/NoU$)	328 μW	19 mW	18 mW	9.8 mW
Control	Local	FPGA, DACs	FPGA	FPGA, DACs, Amplifiers
Operating frequency (GHz)	3.6	28	7.5	3.7
Scalability	Very High	Medium	High	Medium
LE technology	Si MOSFET	Liquid Crystal	PIN diode	Varactor diode
Unit cell reconfiguration time	1 μs [114]	3 s	NR	NR
States per unit cell	2^{64}	2^{16}	4	4
Unit cell control	**Magnitude & Phase**	Phase	Phase	Phase

NR: Not Reported.

6.5 Discussion

The presented design methodology reduces power requirements, cost and addresses scalability and reliability whilst also increasing the functionality of the design. This is made clear in Table 6.2, where a comparison is made with dual polarization FPGA-based PMSFs found in the literature. Dual polarization FPGA-based PMSFs can be found in the literature that use switching diodes (PIN diodes) [54], varactor diodes [138], and even liquid crystals [137]. Generally, the static power requirements for switching diodes, varactor diodes and liquid crystals are in the order of tens of mW, nW, and pW, respectively. Switching diodes require a forward bias current to be switched, therefore they can be significantly power hungry. For example, a PMSF which consist of 20×20 unit cells, as the design in [54], will have at any instance half of its diodes switched on, this translates to a total 6.8 W power consumption, just consumed by the PMSF, without taking into account the FPGA's and any other peripheral's power consumption. Varactor diodes and liquid crystals require significantly less static power requirements but require power hungry external DAC and amplifier models to be biased. This biasing implementation with relatively higher voltages will introduce an increased dynamic power requirements, which are in the order of some mW. This dynamic power is consumed by the DACs that are driving long PCB tracks which connect the varactors diodes or the liquid crystal on each unit cell. The dynamic power requirement is proportional to the reconfiguration time and the geometry of the PCB tracks, and the varactor diode/liquid crystal capacitance. Different length PCB tracks are used in FPGA-based PMSF designs [137,138] therefore, the dynamic power consumption is different for each unit cell. Furthermore, the power requirements for the FPGA module is not negligible, it depends on the FPGA model, its clock frequency, and the function its performing. Generally, FPGAs require 0.5 to 1 W when idle which increases the power requirements for FPGA-based PMSFs ([32–37, 54, 137, 138]). Ideally, the unit cell's static power consumption (P_U) should include the FPGA and any other peripheral power consumption by $P_U = P_T/NoU$, where P_T is the total static power and NoU is the number of unit cells. Unfortunately, the total power consumption is not reported in any FPGA-based PMSFs ([32–37,54,137,138]), and therefore in the comparison in Table 6.2 we consider an optimistic FPGA power consumption equal to 0.5 W. The implementation in [137] seven DAC modules with a typical 0.53 W power consump-

tion, for which we consider an optimistic static power consumption of only 0.2 W. This will bring its total static power consumption to 1.9 W. Similarly, in [138], DACs and amplifier modules are used, but their models are not reported, for which we consider an optimistic 2 W static power consumed by these modules, bringing the total static power to 2.5 W.

FPGA-based PMSFs scalability is restricted by the implementation of the feeding network from the central FPGA to the LEs located on each unit cell, and will require additional FPGAs to scale up. By incorporating the DACs, and the control circuit in a single small ASIC, scalability is addressed since the feeding network is greatly reduced, power consumption is reduced since no FPGA are utilized, and the DACs are locally placed with zero dynamic power requirements. Furthermore, the DACs's direct connection to the LEs eliminates the need of an output buffer (amplifier), since they drive MOSFET gates, which further reduces the power consumption.

Cost is reduced in this PMSF architecture through the integration of all the subcomponents (LEs, control circuit and DACs) into a single die, the ASIC, which can be mass-produced. The commercial cost of the ASIC can be on the order of a similar size varactor or switching diodes. More importantly, by loading each unit cell with complex impedance LEs, the proposed architecture also incorporates dual-polarization magnitude and phase control in the produced PMSF, which hasn't been reported yet.

6.6 Conclusion

A multifunctional and reconfigurable programmable metasurface (PMSF) has been presented that is enabled with an application-specific integrated circuit (ASIC). The design of this PMSF involves the co-development of an ASIC. The ASIC addresses power, cost and scalability limitations found in PMSF designs while offering four complex impedance LEs which can tune their resistance and capacitance values with 8-bit resolution each. The ASIC response in its wafer-level-chip-scale package (WLCSP) was obtained using an innovative de-embedding method. Using the measured ASIC's response, the reflection coefficient responses (magnitude and phase) of the proposed PMSF were optimized for both TE and TM polarization over a wide range of incident angles. The proposed PMSF design with the fine resolution in *RC* can programmatically alter the magnitude and phase of both polarization's reflection

coefficients of each pixel for a wide-angle range. This was experimentally verified near the design frequency of 3.6 GHz. By setting the reflection coefficient to zero for a given incident wave, both TM and TE can be perfectly absorbed.

The PMSF design finds applications in holography, imaging, programmable wireless environments, but also in programmable arbitrary wavefront synthesis antennas. Its operating frequency falls within the currently deployed 5G sub-6GHz band, but the design methodology can be expanded for future sixth generation (6G) telecommunication networks in the millimeter waveband.

Chapter 7

ASIC Enabled Programmable Metasurfaces: Synthesis and Performance

A multifunctional and reconfigurable PMSF enabled by an ASIC is presented in this chapter, that targets smart wireless environment applications. The PMSF design showed multifunctional capabilities in Chapter 4 and Chapter 6, and realised the design by significantly expanding the work by utilizing the produced ASICs that were presented in Chapter 5. In Chapter 6, the PMSF design experimentally demonstrated the ability to control independently the magnitude and phase of the reflection coefficients for both orthogonal polarizations. Here, in this chapter, this ability is exploited to demonstrate programmable electromagnetic wavefront manipulation. A fast and accurate synthesis method using a two-dimensional single-iteration discrete Fourier transform (DFT) for producing multiple pencil beams, each with different polarizations, is presented. Each pencil beam can have a linear, right-handed circular, left-hand circular or even elliptical polarization. The synthesis method is ideal for wireless reconfigurable environments enabled by the PMSF, where the number of unit cells is very large. The PMSF aims to be a single component, installed not only in the surrounding walls to reconfigure the wireless environment, but also at the transmitting antennas. The design is experimentally verified by producing a mixture of linearly polarized and circularly polarized wavefronts, and single, dual and simultaneous OAM pencil beams are experimentally shown.

7.1 Introduction

Programmable metasurfaces (PMSFs) are the two dimensional counterparts of metamaterials which are electronically controlled through software [33, 35–37]. These surfaces have demonstrated great control over the electromagnetic environment. Their sub-wavelength composition gives rise to new physical properties that are not found in nature. PMSFs can also be found in the literature as RISs and they offer the possibility to improve wireless telecommunications [38, 40–42, 143].

Due to the low profile that PMSFs offer, they can be seamlessly installed within wireless environments in order to electromagnetically manipulate them. Manipulate them in a manner to improve multiple aspects of the wireless communications, such as increased reliability, energy efficiency and security [38, 40–42, 48–50, 143].

These reprogrammable approaches outlined in [32–36] control the unit cell only through discrete states. Furthermore, the unit cell reflection phase response is only programmed with the use of varactors. Varactors can be used for phase-only programmability, which could satisfy anomalous reflections applications, or in more simple terms the redirection of an impinging wave. More complex functionalities may be desired when the PMSF is used as part of the antenna. Similar to traditional reflectarrays and transmitarrays [52, 53, 137], PMSFs can be illuminated by a static antenna and tailor the far-field pattern [50, 51, 144]. In this manner, a new antenna is formed by the two, the passive illuminator antenna and the active PMSF.

In order to generate a more complex wavefront, phase-only synthesis methods can be employed, such as genetic algorithms [32]. Particle swarm optimization algorithms [145] can also be applied like in any other antenna synthesis problem, however these methods all require repetitive time-consuming calculations.

Machine learning is promising in achieving fast and accurate computation [36, 146] by using precomputing or training algorithms. This method was used in [146] to code an MSF and the predicted results were 94% accurate compared to the measurements, with a computation time of 5 ms.

Analytical or open loop solutions to synthesis problems exist if the restriction to control only the phase is eliminated. For this reason, more complex unit cell structures are required to control both the magnitude and phase of the reflected or transmitted wave. Unit cells with this control have been shown to generate multiple beams simultaneously [15], and can even control the power level of each beam

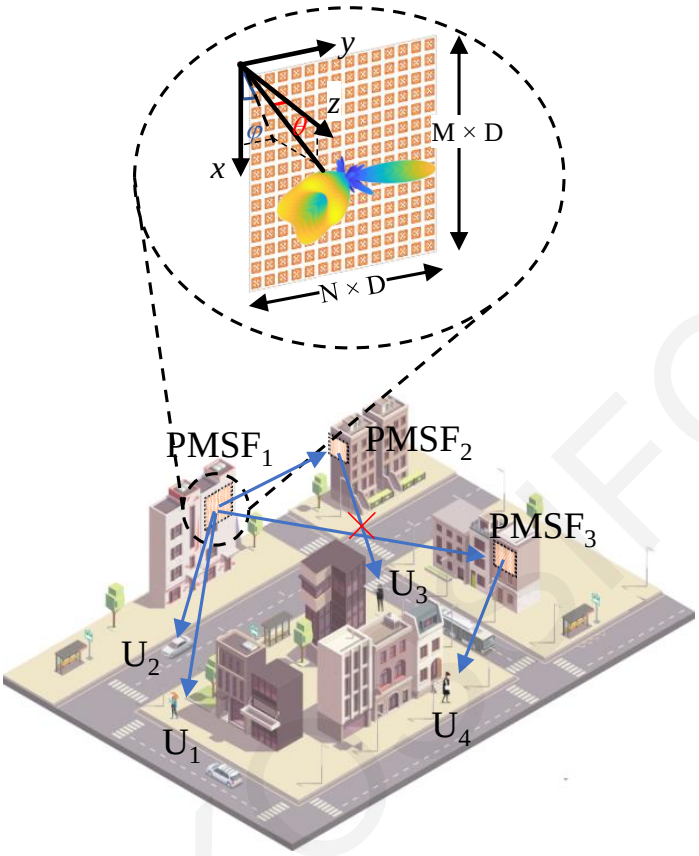


Figure 7.1: Illustration of PMSF installed in a terrestrial environment. Three PMSFs are positioned at strategic positions to synthesize a complex wavefront ($PMSF_1$) and facilitate communication with slow (U_1) and fast moving users (U_2), redirect ($PMSF_3$) towards a user (U_4) but also absorb ($PMSF_2$) an incident wave to block a user (U_3).

independently [17]. Holographic MSFs have also been demonstrated by controlling both the magnitude and phase of the transmitted wave [19, 147]. The designs in [15, 17, 19, 147] are static, limited to one polarization control and don't report the computational time needed to calculate the unit cell responses.

The capabilities of the PMSF design reported in Chapter 6 [141] are presented. In summary, in [141] the details of the PMSF design were presented. The ASIC in its WLCSP was measured, and its response was presented. The ASIC was populated on the back of the PMSF and was used to provide the programmable control of both magnitude and phase for both TE and TM polarized waves. This control enables the PMSF to perfectly absorb waves with multiple polarizations at both normal and oblique angles of incidence [22], but also enables the PMSF to generate dual-polarization complex wavefronts, which is presented here in this chapter.

The PMSF's primary application can be seen in Fig. 7.1, where PMSFs are installed in strategic locations to programmatically generate wavefronts and control

the wireless environment. Three PMSFs are installed in this example. $PMSF_1$ is illuminated by a passive antenna and it synthesizes the reflected wavefront to produce a multibeam pattern or any complex wavefront. In this manner, $PMSF_1$ is functioning as a reconfigurable basestation antenna that aims to satisfy communication between multiple users (U_1-U_4). Although the scenario is much more complex in reality, in this simplified scenario we consider the location of the users to be known. With this information, and the urban environment's geometry it can deduced that there is no line-of-sight between $PMSF_1$ and U_4, and for this reason $PMSF_3$ is being utilized as an anomalous reflector to establish a wireless communication path. In the case where a user may act maliciously (U_2) a PMSF (e.g. $PMSF_2$) can absorb its radiation and block it from accessing the network, as was demonstrated in the previous chapter, Chapter 6 [141] as part of the PMSF capabilities. Users in this scenario might be moving in the environment at different angular speeds relative to the PMSF. In this example, U_2 is moving at a relatively fast speed and therefore needs a rapid refresh rate of the PMSF reconfiguration. In this case, the PMSF reconfiguration speed needs to be able to track a fast-moving user.

The reconfiguration speed consists of the computational time needed to derive each unit cell's state and also the electronic programming of each ASIC populated on each unit cell. The ASICs programming speed is limited by the ASIC's asynchronous control circuit speed [114]. The computation time to calculate each unit cells state is not negligible when complex wavefronts are needed.

In this chapter, the capabilities of the PMSF are presented. Multiple pencil beams are computed with agile polarization control [43–45, 107], while taking into account the computational time. A fast and accurate method to synthesize multiple pencil beams while controlling their magnitude and polarization is presented. The PMSF design methodology can perform multiple functions and aims to target future multi-user basestation and wireless applications [40, 92, 94, 95, 107]. Furthermore, the dual polarization magnitude and phase control that the PMSFs possess make it an attractive solution for holographic and imaging applications.

This chapter is organized into the following sections. In Section 7.2 a multiple pencil beam synthesis method is presented, and in Section 7.4 the synthesis method's implementation is described. The PMSF's single-pencil beam (or anomalous reflection), multiple pencil beam and other wavefront control capabilities are presented in Section 7.5. The design is experimentally validated using a 16×16 unit cell PMSF

prototype, and its measured results can be found in Section 7.6, followed by the Conclusion.

7.2 DFT Synthesis

A fast synthesis method that addresses the computational time required for obtaining the reflection coefficients of an arbitrary size (N×M) PMSF is presented in this section. The reflected far field, F in the spherical coordinate system to be can be expressed as:

$$F(\theta,\phi) = EF(\theta,\phi)\sum_{m=0}^{M-1}\sum_{n=0}^{N-1} i_{mn} r_{mn} e^{j2\pi\left[\frac{mD}{\lambda}\sin\theta\ \cos\phi + \frac{nD}{\lambda}\sin\theta\ \sin\phi\right]}. \tag{7.1}$$

Here, EF is the element factor [17], i_{mn} and r_{mn} are complex incidence and reflection coefficients, respectively. The multiplication of these two components results in the analogous complex excitation used in traditional array factor analysis. The wavelength is denoted by λ and D [141] is the physical dimension or the periodicity of the unit cell. i_{mn} is given by:

$$i_{mn} = \frac{\lambda}{(4\pi d_{uc})^2} e^{-j2\pi\frac{d_{uc}}{\lambda}}. \tag{7.2}$$

Here, d_{uc} is the distance of each unit cell from the source. The first term of the equation can be easily identified as Friis' equation, used to calculate the magnitude of the incident wave, while the second exponent term is used to calculate the phase. Even though (7.1) is best suited for a plane-wave excitation, the work can be easily adapted to a spherical-wave excitation located in the near field, with the use of i_{mn}, taking into account the different magnitudes and phases of the incident wave on each unit cell. This can be expanded by using measured incidence coefficients from a realized antenna illuminating the PMSF. The reflection coefficient r_{mn} is extracted from a unit cell simulation with periodic boundary conditions or through measurements [141]. From the results, it was identified that the reflection coefficient has the following form:

$$r_{mn} = \begin{bmatrix} r_{xx}^{mn} & r_{xy}^{mn} \\ r_{yx}^{mn} & r_{yy}^{mn} \end{bmatrix} = \begin{bmatrix} A^{mn}\, e^{j\phi_{xx}^{mn}} & 0 \\ 0 & B^{mn}\, e^{j\phi_{yy}^{mn}} \end{bmatrix}. \tag{7.3}$$

Here, r_{xx}^{mn} and r_{yy}^{mn} are complex reflection coefficients with a finite reflection (magnitude and phase) range. The unit cell is lossy, therefore the ranges of A^{mn} and B^{mn} do not extend from 0 to 1 and the phase responses (ϕ_{xx}^{mn}, ϕ_{yy}^{mn}) do not cover the range from $-\pi$ to π. The phase response can be satisfied though by relaxing the A and B terms to a smaller value and normalizing the calculation to that value. The terms r_{yx}^{mn} and r_{xy}^{mn} are equal to zero, indicating that there is no cross-polarization conversion in the unit cell. For this reason, the incident wave should contain both polarizations if a dual-polarization synthesis is desired.

For this topology where the PMSF is on the xy plane (Fig. 7.1), the far field can be expressed in the uv coordinate system:

$$F(u,v) = EF(u,v) \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} i_{mn} r_{mn} e^{j2\pi \left[m\frac{D}{\lambda}u + n\frac{D}{\lambda}v \right]}. \tag{7.4}$$

where:

$$u = \sin\theta\ \cos\phi,\ v = \sin\theta\ \sin\phi. \tag{7.5}$$

It was shown in [148] that the relationship between F and the $M{\times}N$ 2D inverse fast Fourier transform on the excitation (IF) is :

$$F(u,v) = M\,N\,IF(l,k). \tag{7.6}$$

where the lk indices are related to the uv coordinate system by:

$$u = \frac{\lambda}{D}\left(\frac{k}{M} - \frac{1}{2}\right),\ v = \frac{\lambda}{D}\left(\frac{l}{N} - \frac{1}{2}\right). \tag{7.7}$$

Therefore, one can sample the far field at the points shown in (7.7) and perform a 2D DFT to obtain the element-to-element multiplication of $i_{mn}{\times}r_{mn}$. Since i_{mn} is geometrically calculated, the reflection coefficients (r_{mn}) can then be easily calculated by simply dividing $i_{mn}{\times}r_{mn}$ by i_{mn}. Similarly, in an M×N matrix values that are associated with a uv direction can be set equal to a complex number. A 2D DFT of the array will yield the $i_{mn}{\times}r_{mn}$ that would produce a beam in the set uv direction. In this work, two input matrices are used, one for the x component (In_x) and one for the y component (In_y), which are independently set since independent control of the reflection coefficients for both the x and y polarization components (r_{xx} and r_{yy}) can be performed.

$$In_x = \begin{bmatrix} In_x(1,1) & \cdots & In_x(1,M) \\ \vdots & \ddots & \vdots \\ In_x(N,1) & \cdots & In_x(N,M) \end{bmatrix},\ In_y = \begin{bmatrix} In_y(1,1) & \cdots & In_y(1,M) \\ \vdots & \ddots & \vdots \\ In_y(N,1) & \cdots & In_y(N,M) \end{bmatrix}. \tag{7.8}$$

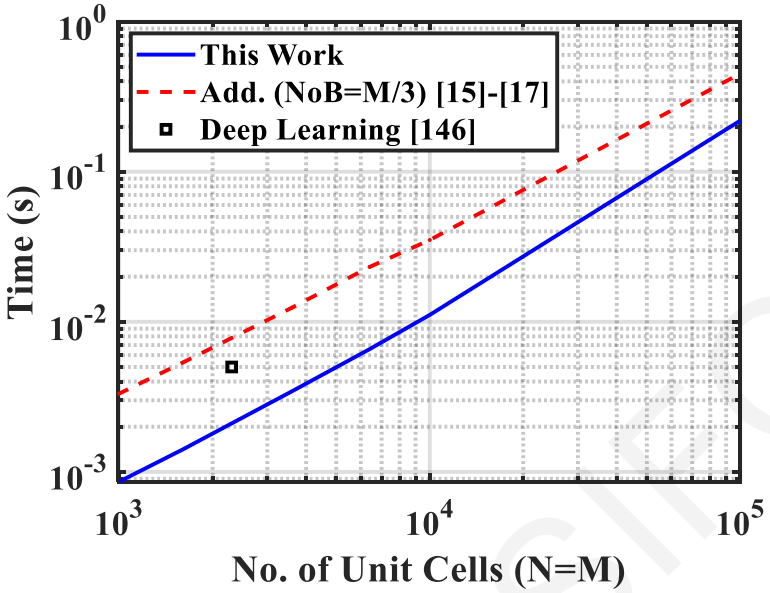


Figure 7.2: Calculation time needed to compute each unit cell's magnitude and phase versus the number of unit cells. The number of unit cells along both the x and y directions were equal (N = M).

These input matrices are computed using a 2D DFT to obtain the reflection coefficients (r_{xx} and r_{yy}). An important advantage of having the input entries equal to a complex number is that one can control not only the magnitude but also the phase of a pencil beam for both x and y polarizations. This is particularly useful, since it allows the flexibility to set pencil beams to have LP, RHCP, LHCP or even elliptical polarization.

The above calculations for obtaining the element reflection coefficients were performed for a random number of entries in the input matrices and for an $M \times N$ number of unit cells, while keeping the number of unit cells along the x axis equal to the number of unit cells along the y axis (N=M). The code was implemented in MATLAB, executed on an average laptop running on Windows 10, using 8 GB RAM and an intel core i5 CPU. The time elapsed on the calculations was measured with the use of timer functions (tic and toc functions) for 600 iterations and was averaged out. The plot of the calculation time versus the number of unit cells can be seen in Fig. 7.2.

The calculation time of a random number of pencil beams is significantly shorter than the calculation time reported in [146] using a deep-learning algorithm, even though more complex beams are calculated and it is executed on a typical laptop. Compared to the addition theorem used in [15–17], the calculation time was found to be significantly lower. The calculation time in [15–17] will be affected not only

by the number of unit cells but more importantly by the number of beams (NoBs). The calculation times used to calculate a NoBs equal to $^{M}/_{3}$ are plotted in Fig. 7.2 for comparison.

7.3 Directivity, Gain and Efficiency

In this section the directivity, the gain and th efficiency of PMSFs is briefly presented. The directivity of a PMSF design can be easily calculated with the well known equation [74, 149]:

$$D(\theta,\phi) = \frac{|F(\theta,\phi)|^2}{\frac{1}{4\pi}\int_0^{2\pi}\int_0^{\pi}|F(\theta,\phi)|^2 \sin\theta \, d\theta d\phi}. \tag{7.9}$$

Similarly to traditional reflect arrays, a planar PMSF's can be illuminated by a passive antenna and its gain (G) can be calculated with:

$$G(\theta,\phi) = D(\theta,\phi)\varepsilon_{ap}, \tag{7.10}$$

where ε_{ap} is the overall efficiency of the combine passive antenna and PMSF. This is generally referred to as aperture efficiency, and it is a product of other factors. Some of the most common factors are listed below.

- Feed efficiency (ε_f): This is the efficiency of the reflectarray feed system, the passive antenna. For a horn antenna feed or a open-ended rectangular waveguide (ORWG) feed, this efficiency is reduce from Ohmic losses.
- Spillover efficiency (ε_s): The passive antenna can illuminate the PMSF in such a way that part of energy is not intercepted by the PMSF. Spillover efficiency is the fraction of the total power that is radiated, intercepted by the reflecting aperture, in this case the PMSF, and collimated relative to the radiated feed power.
- Blockage efficiency (ε_b): The feed antenna can potentially block part of the radiation. The fraction of the power that is not blocked and the total reflected power is named as blockage efficiency.
- Illumination efficiency (ε_i): An aperture will obtained its maximum directivity when it is illuminated uniformly, a taper illumination will reduce the directivity. This efficiency is also know as taper efficiency.

- Material loss (ε_Ω): Material loss are common in traditional reflectarrays such as patch reflectarrays. These losses will arise from substrate and conductor losses and will result in an overall reduction of the antenna gain. This efficiency (ε_Ω), is the fraction of the total radiated power and an ideal case where the materials like the conductors and the dielectrics are lossless.

- Phase efficiency (ε_φ): Spacial quantization of the reflection coefficients, which are implemented by the unit cells, opposed to a smooth reflector aperture, can potentially reduce the overall gain. This gain is often called phase efficiency (ε_φ).

- Polarization efficiency (ε_p): The feed can couple power to the cross-polarized wavefront. This power will reduce the gain in the co-polarized wavefront. This efficiency, polarization efficiency (ε_p), is the fraction of that amount.

Therefore, from the above factors the aperture efficiency reads:

$$\varepsilon_{ap} = \varepsilon_f \varepsilon_s \varepsilon_b \varepsilon_i \varepsilon_\Omega \varepsilon_\varphi. \tag{7.11}$$

The improvement of all the efficiency terms in (7.11) is important in order to increase the overall gain of the PMSF when illuminated by a passive antenna or in more simple terms in a reflectarray antenna operation. In this scenario this should be done with a relatively small size PMSF (or reflectarray). Spillover efficiency, blockage efficiency and illumination efficiency, can be adjusted by carefully positioning of the feed [74, 149]. Phase efficiency and polarization efficiency, can be improved by the unit cell implementation. A smaller unit cell will generally produce smaller phase errors and a dual polarized unit cell can eliminate polarization errors. Material loss efficiency is embedded in the reflection coefficients in PMSF designs, since the reflection coefficient amplitude will get reduced by the material losses in the unit cell or even by losses in a complex load. One can improve this in traditional reflectarrays as also in PMSFs by using high frequency low-loss substrates.

In the scenario of programmable wireless environments, the PMSF's size is significantly larger than traditional reflectarrays, and there is not no fix position feed. Due to the PMSF's main redirection operation the gain is expressed as a fraction between the scenario where the signal would had undergoes free space loss and redirected by a perfectly conductive spherical object. This is well known as

bistatic radar cross section (BRCS), and it depends on the polarization and in its matrix form reads:

$$\begin{bmatrix} BRCS_{\theta\theta} & BRCS_{\theta\phi} \\ BRCS_{\phi\theta} & BRCS_{\phi\phi} \end{bmatrix} = \lim_{r\to\infty} 4\pi r^2 \begin{bmatrix} \frac{|E^s_\theta|^2}{|E^i_\theta|^2} & \frac{|E^s_\theta|^2}{|E^i_\phi|^2} \\ \frac{|E^s_\phi|^2}{|E^i_\theta|^2} & \frac{|E^s_\phi|^2}{|E^i_\phi|^2} \end{bmatrix}, \tag{7.12}$$

where the subscript letters θ and ϕ in the BRCS and in the electric field (E) indicate the polarization, and the superscript letters indicate the direction of the electric field, s stands for scattered and i stands for incident. The illumination of the PMSF in this case is implemented from a distance larger than the Fraunhofer distance, therefore it can be considered in the far field and the wave incident upon the surface can be considered a plane wave. When the PMSF is illuminated within the Fraunhofer distance the gain obtain from the PMSF can be calculated with:

$$G(\theta,\phi) = 4\pi \frac{U(\theta,\phi)}{P_i}, \tag{7.13}$$

where P_i is the total incident power upon the PMSF and $U(\theta,\phi)$ is the radiation intensity which is defined as:

$$U(\theta,\phi) = \frac{r^2}{2\eta}|E(\theta,\phi)|^2. \tag{7.14}$$

The scattered efficiency of the PMSF when controlling both magnitude and phase can be approximated with the average of the magnitude of reflection coefficients:

$$\varepsilon_{sc} = \frac{1}{N\,M}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}|r_{mn}|^2. \tag{7.15}$$

When a single beam is scattered from the PMSF all the calculated reflection coefficients have the same magnitude. For this case, if it is required to scatter only half of the incident power ($\varepsilon_{ref} = 0.5$), the reflection coefficients can be normalized to $\sqrt{0.5}$. When multiple beams are produced or a taper is applied to adjust the beams half-power beamwidth (HPBW), the total scattered power can be approximated with $P_i\varepsilon_{sc}$.

7.4 Metasurface Synthesis Implementation

In this section, the steps taken to generate a reflected beam at a set direction are described. The unit cell geometry reported in [141] is considered and a PMSF consisting of N×M unit cells, as shown in Fig. 7.1. These steps are as follows:

7.4.1 Set Direction

The first step is to set a direction of the pencil beam or beams. This is done by setting the entry values of both In_x and In_y. The entry values In_x and In_y for a given lk direction are each a complex number with a maximum magnitude equal to one. The rest of the (In_x and In_y) matrix entries where a pencil beam is not desired are set to be equal to zero. For example, $|In_x(l,k)| = |In_y(l,k)| = 1$ while the phase difference is set to be 90° ($\angle In_x(l,k) - \angle In_y(l,k) = 90°$). This combination will yield a RHCP pencil beam at the set direction. A LHCP pencil beam can also be generated by simply switching the sign of the phase difference ($\angle In_x(l,k) - \angle In_y(l,k) = $ -90°), while keeping the magnitude equal ($|In_x(l,k)| = |In_y(l,k)|$).

7.4.2 Computation and Realization of the Unit Cell Reflection Coefficients

For any given In_x and In_y and the incident wave direction, the computed magnitude and phase for both x and y polarization reflection coefficients (r_{xx}, r_{yy}) are calculated according to the procedure described in Section 7.2. The magnitudes of the reflection coefficients are not equal to unity, since the computation described in Section 7.2 takes into account the free space losses with the use of the term i_{mn}.

The realization of the calculated reflection coefficients, is implemented by loading each unit cell with the appropriate RC combinations. These RC combinations are found by using Fig. 7.3 as a look-up table to map values of r_{xx} and r_{yy} to specific values of R and C. The reflection coefficient r_{xx} is translated into the RC values to be implemented by the loading elements LE_1 and LE_3 through the simulated results of the x-polarized wave using Fig. 7.3(a) and Fig. 7.3(b). Analogously, the reflection coefficient r_{yy} is translated into the RC values implemented by LE_2 and LE_4 through the simulated results of the y-polarized wave using Fig. 7.3(c) and Fig. 7.3(d).

The RC combination for all LEs doesn't cover the complete RC range plotted in Fig. 7.3. Instead, it only covers an area around the optimal perfect absorption RC combination point.

Similarly, the realization of the calculated reflection coefficients (r_{xx} and r_{yy}) in the manufactured prototype is implemented by programming each ASIC to bias the corresponding LE with the appropriate biasing voltages. The correlation of the reflection coefficient to biasing voltages is done by using the measured reflection

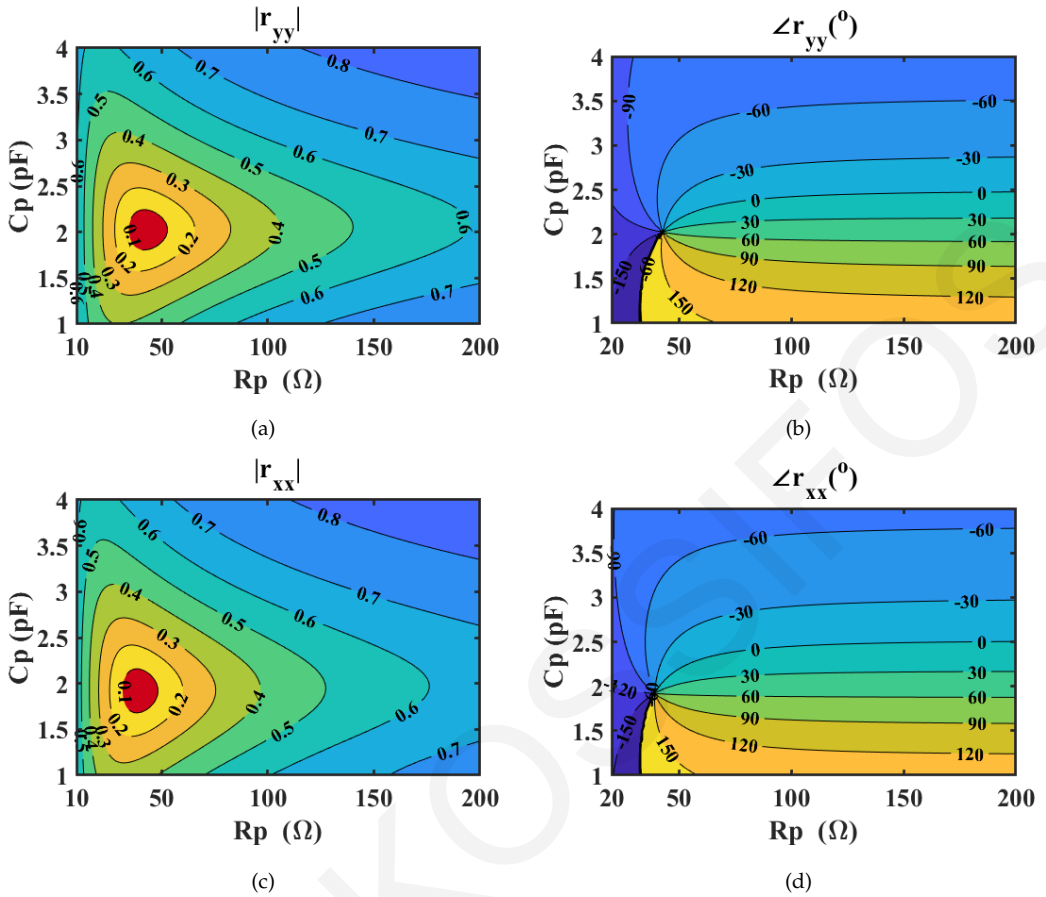


Figure 7.3: Reflection coefficient magnitude and phase for LEs *RC* area for an incident angle of $\theta = 30°$. (a) Reflection coefficient magnitude, and (b) reflection coefficient phase for the x-polarized incident wave (TM). (c) Reflection coefficient magnitude, and (d) reflection coefficient phase for the y-polarized incident wave (TE).

coefficients as a look-up table to map values of r_{xx} to $V_{R1,3}$, $V_{C1,3}$ Fig. 6.12, and r_{yy} to $V_{R2,4}$, $V_{C2,4}$ Fig. 6.13.

7.4.3 Metasurface Assembly

In the manufactured prototype the biasing voltages (V_R, V_C) are programmed in the ASICs by converting them into their binary form and serially programming them in each ASIC's control circuit using the ASIC's asynchronous protocol. In simulation, the PMSF is assembled in ANSYS HFSS to be simulated. The complete PMSF is shown diagrammatically in Fig. 7.1, and is excited using a plane wave. The PMSF's unit cell details can be found in detail in Chapter 6 [141]. The LEs in simulation are replaced with *RLC* boundaries. The *RC* values are automatically updated in the defined *RLC* boundaries with the use of Visual Basic scripts.

7.5 Metasurface Capabilities

In this section, the capabilities of the PMSF design are demonstrated in simulations. In order to facilitate the simulations, the size of the PMSF is reduced to 14×14 unit cells, which is the size that could be effectively simulated using our available computational resources. With this 14×14 unit cells PMSF, it is firstly demonstrated that a single pencil beam can be generated in all the visible In_x and In_y entries. Then, multiple pencil beams are generated, where each beam possesses its own polarization, and finally an orbital angular momentum (OAM) beam and a single pencil beam pattern is generated simultaneously as an example of a complex wavefront.

7.5.1 Single Pencil Beam

Initially the normalization of A^{mn} and B^{mn} values described in Section 7.4, are determined. This is implemented by finding the maximum equal-amplitude reflection coefficient values (A and B) that can satisfy a phase variation from $-\pi$ to π so as to be able to perfectly satisfy the realization of the reflection coefficients without any quantization errors found in other FPGA-based PMSF implementations, and thus produce higher accuracy wavefronts. The accuracy of the produced wavefront ($F(\theta,\phi)$) compared to the calculated wavefront ($F(\theta,\phi)_{calc}$) in this work is considered as in [146]:

$$Acc = 1 - \frac{1}{NoP}\sum |F(\theta,\phi) - F(\theta,\phi)_{cal}|, \tag{7.16}$$

where NoP is the number of points. In Fig. 7.4 a broadside pencil beam is plotted for a range of normalization values (A and B) ranging from 0 to 0.8, while in the top-right insert of the same figure the BRCS in decibel per square meter (dBsm) and the accuracy (Acc) are plotted. These are obtained by sequentially repeating the procedure described in Section 7.4, by setting the values in the input matrices In_x and In_y to produce a broadside beam. Since the simulated size of the PMSF is 14×14, the broadside direction will correspond to the lk entries in the input matrices, both being equal to 7 ($In_x(7,7) = 1$, $In_y(7,7) = 1$). The obtained reflection coefficients will be subsequently normalized to A and B ($A \times r_{xx}^{mn}$, $B \times r_{yy}^{mn}$) and in these settings we consider an incident wave at $\theta = 30°$, $\phi = 0°$. As can be seen in Fig. 7.4, by increasing the normalization values (A, B) there is an increase in the BRCS gain. This is true up to a normalization value of 0.7, where a phase variation from $-\pi$ to π can be satisfied.

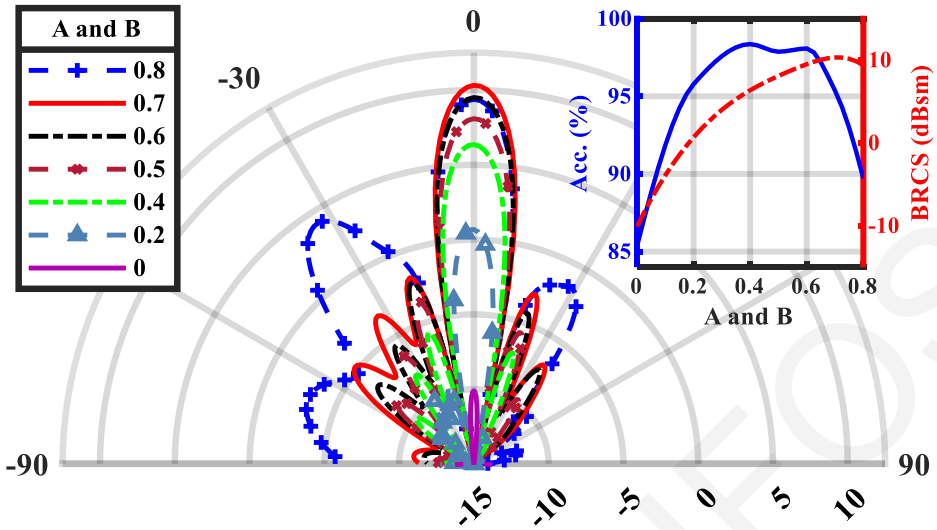


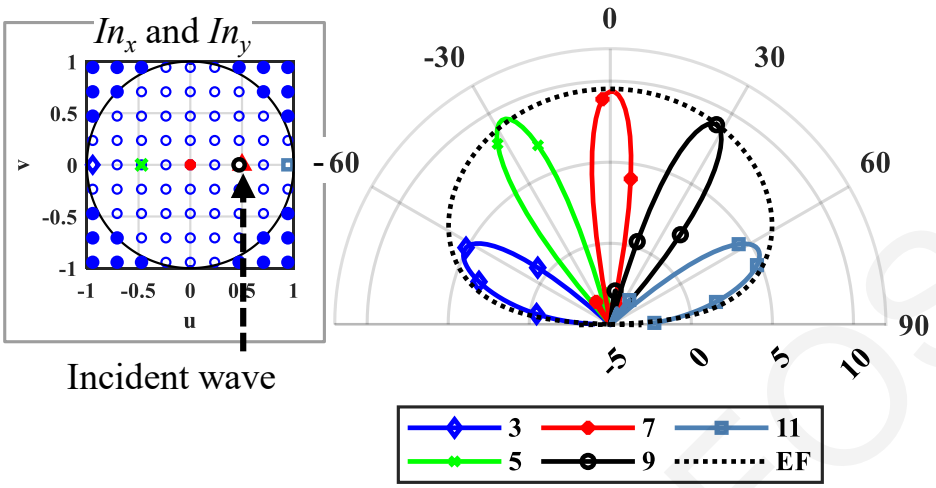
Figure 7.4: Total bistatic radar cross section gain (in dBsm) for a single pencil beam at broadside generated for various normalizations values (A and B).

Beyond this, for example for a normalization value of 0.8, which is plotted with a dashed dot blue line with '+' markers in Fig. 7.4, the realized reflection coefficient errors will result in a decreased BRCS gain in the broadside direction, and partial specular reflection at approx. $\theta = -30°$.

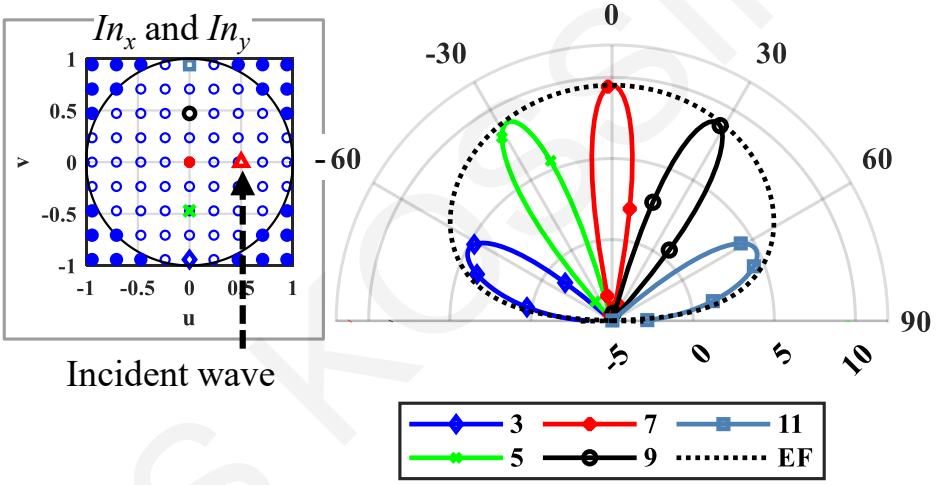
For this simulated size of 14×14 unit cell PMSF, as can be seen in the top right insert of Fig. 7.4, BRCS gain control can be obtained from 10.5 to -10dBsm and a peak accuracy (*Acc*) of 98.5% at 0.4 normalization. Naturally, higher gain can be obtained for a normal angle of incidence, and since the presented architecture can be scaled to N×M unit cells, higher gain can be achieved by implementing a larger PMSF. The accuracy in Fig. 7.4 increases from 85% to 98.5% for normalization values ranging from 0 to 0.4. This increase is attributed to the main beam being proportionally larger than the unwanted fields produced by the edge effects. For larger normalization values from 0.4 to 0.6 the accuracy reduces as the increase in reflection coefficient realization errors produces higher side lobes. Eventually, the accuracy drops to 90% at a normalization of 0.8 when a partial specular reflection is produced.

Table 7.1: Efficiency (ε_{sc}) for various normalization values of PMSF settings in Fig. 7.4.

A and B	0.8	0.7	0.6	0.4	0.2	0
Simulated efficiency (ε_{sc}, %)	49.9	41.3	33.3	15.4	4.3	0.4
Calculated efficiency (ε_{sc}, %))	48.1	39.5	36.3	16.1	4.0	0



(a)



(b)

Figure 7.5: Produced pattern in dBsm for five separate reflected beams, together with the graphical representation of the input matrices In_x and In_y in the uv coordinates in the top left inset, for five entries in the two orthogonal planes of (a) $\phi = 0°$ and (b) $\phi = 90°$.

The simulated scattered efficiency (ε_{sc}) for various normalization values was compared with calculated values using (7.15). In simulation these values were obtained by integrating the real part of the Poynting vector that is normal over the whole PMSF area in HFSS. These values can be found in Table 7.1 and they are in good agreement with the calculated values. As it can be seen the larger implemented reflection coefficients will result into a larger efficiency.

A single beam was produced for other directions and a normalization of 0.6 was subsequently chosen as a compromise between accuracy and gain. The reflected beam direction was sequentially set for k entries from 3 to 11 while keeping l constant and equal to 7 ($In_x(7, 3-11), In_y(7, 3-11)$). All single beams were set to possess an LP ($|In_x(7, 3-11)| = |In_y(7, 3-11)|$). These entries would translate into a single

beam scan along the u-axis. Similarly, a sweep along the v-axis was performed by sequentially setting l entries from 3 to 11 while keeping k constant and equal to 7 ($|In_x(3-11,7)| = |In_y(3-11,7)|$). The direction of the reflected beam in spherical coordinates (θ, ϕ) can be easily found by converting the lk indices direction using (7.5) and (7.7).

The simulated results of the total reflected electric field are plotted in the two orthogonal planes of $\phi = 0°$ and $\phi = 90°$ in Fig. 7.5(a) and Fig. 7.5(b), respectively. In Fig. 7.5(a) five overlaid pencil beams that are set on the u-axis (ϕ =0 °) are plotted. The In_x and In_y entries are graphically plotted in the same figure's top-left inset in the uv coordinates. It should be noted that In_x and In_y extend outside the visible region, which is the circular area where the magnitude of uv is less or equal to 1 ($1 \leq \sqrt{u^2+v^2}$). The visible region is plotted in Fig. 7.5(a) and Fig. 7.5(b), the visible entries are indicated with empty blue circle markers, while the entries outside the visible region are plotted with filled blue circle markers. The entry with k=3 is plotted with the diamond shaped marker labelled 3 in the legend of Fig. 7.5(a), and corresponds to the beam reflected at $\theta = -70.5°$. The entries with k=5, 7, 9 and 11 are labelled 5-11 respectively, and correspond to beams reflected at $\theta = -28.1°$, 0°, 28.1° and 70.5°, respectively. The results show that the beams can scan from θ = -70.5° to +70.5°, and that the magnitude of the beams follows the element factor EF curve along θ, which is approximated with a cosine function, as shown by the black dashed line in Fig. 7.5(a) and Fig. 7.5(b). Similarly, five entries along the v-axis ($\phi = 90°$) are set to demonstrate the beam scanning capabilities of the design in this orthogonal plane. The set entries ($|In_x(3-11,7)| = |In_y(3-11,7)|$) and the scattered fields are plotted in Fig. 7.5(b). More importantly it should be noted that the accuracy (Acc) for all the In_x and In_y entries was higher than 97.6%.

This demonstration and the calculations to create a single pencil beam can also be used as a metric on the anomalous reflection capabilities of this PMSF design when used with this synthesis method. The procedure is similar to the redirection of an incident wave at an angle which doesn't follow Snell's law in the quantized uv coordinates. Alternatively to this procedure, optimization on the LEs' RC values can be performed in order to obtain higher anomalous reflection efficiency (or lower scanning losses) when the calculation time restrictions are extenuated ([95]). Lower scanning losses can also be obtained when the size of the unit cell D is reduced, ([17]) as can be calculated by the EF term in (7.1). This unit cell size reduction will come

with an added power requirement and cost per PMSF area.

An increase of PMSF area, assuming a constant unit cell size, would not only provide higher directivity, but also provide more entries in the *uv* visible region. More entries would provide smaller scanning angle steps that can be performed when scanning with the presented DFT method. This can be identified in (7.7), where M and N are in the denominator. Similarly, a smaller unit cell size will increase the number of entries in the *uv* visible region. It is apparent that there is a compromise when choosing the size and unit cell size in PMSFs when operating with the presented DFT method. The presented method's advantage lies in the calculation speed when multiple pencil beams are computed, as demonstrated in Section 7.2. Multiple pencil beam generation is demonstrated in the next subsection.

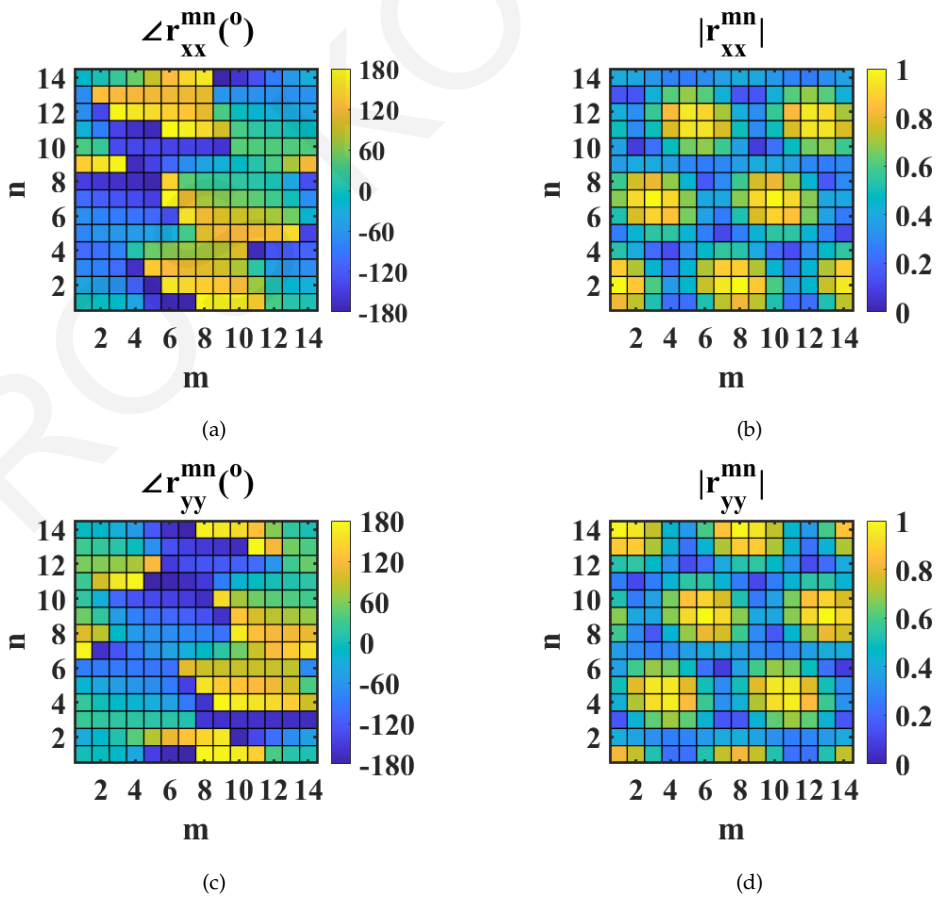


Figure 7.6: Reflection coefficients for both x-polarization (r_{xx}) and y-polarization (r_{yy}), calculated for the example input matrices In_x and In_y and incident angle shown in Fig. 7.9. (a) Phase of the reflection coefficient for the x-polarization $\angle r_{xx}$ in degrees, (b) magnitude of the reflection coefficient for the x-polarization, $|r_{xx}|$, (c) Phase of the reflection coefficient for the y-polarization $\angle r_{yy}$ in degrees, and (d) magnitude of the reflection coefficient for the y-polarization $|r_{yy}|$.

7.5.2 Multiple Pencil Beams

More than one entry can be set in the In_x and In_y matrices, and each can be set to its own polarization. In this example, three pencil beams were set simultaneously. One pencil beam was set to be linearly polarized containing both x and y components ($|In_x(6,6)| = In_y(6,6)|$, $\angle In_x(6,6) - \angle In_y(6,6) = 0°, (u,v) \simeq (-0.24,-0.24), (\theta,\phi) \simeq (19.5°, 225°)$), the second was set to be LHCP ($|In_x(8,5)| = |In_y(8,5)|$, $\angle In_x(8,5) - \angle In_y(8,5) = -90°, (u,v) \simeq (-0.47, 0.24), (\theta,\phi) \simeq (31.8°, 153.4°)$) and the third pencil beam was set to be RHCP ($|In_x(8,8)| = |In_y(8,8)|$, $\angle In_x(8,8) - \angle In_y(8,8) = 90°, (u,v) \simeq (0.24, 0.24), (\theta,\phi) \simeq (19.5°, 45°)$). The combination of CP and LP beams is a particularly useful example, since it can demonstrate not only the accuracy of the direction and shape of the reflected beam, compared to the calculated reflected pattern, but also the phase in the far field with the use of the axial ratio (AR) of the reflected beam.

The calculated reflection coefficient for the x and y polarizations are plotted in Fig. 7.6(a)-Fig. 7.6(d). The translated loading RC values for LE_1 and LE_3 can be found in Fig. 7.7(a) and Fig. 7.7(b), while the RC values for LE_2 and LE_4 can be found in Fig. 7.7(c) and Fig. 7.7(d). The simulated pattern is shown in Fig. 7.8(a), which achieved an accuracy (Acc) equal to 98.2% and an efficiency (ε_{sc}) equal to 12.2%. On the same figure the set entries of the In_x and In_y matrices are overlaid to demonstrate that indeed three pencil beams were generated at the set direction.

In Fig. 7.8(b) and Fig. 7.8(c) polar plots of the simulated pattern are plotted for $\phi = 45°$ and $\phi = 153°$, respectively. In Fig. 7.8(b) the polar plot captures an LHCP pencil beam at $\theta = 19.5°$ and an LP pencil beam at $\theta = -19.5°$. At the angle where the LHCP beam is directed, the AR is below 3dB as expected. An RHCP pencil beam at $\theta = 31.8°$ is plotted in Fig. 7.8(c) overlaid with the AR which is also below 3dB.

7.5.3 OAM Wavefront Synthesis

The proposed PMSF design's ability to control both the reflection magnitude and phase for both polarizations can be also applied to tailor arbitrary wavefronts that are not computed with the proposed synthesis method described in Section 7.2. Orbital angular momentum (OAM) beams can be synthesized simultaneously with pencil beams. The reflection coefficients to generate an OAM beam at a particular direction can be calculated using the method shown in [18, 112], and similarly for

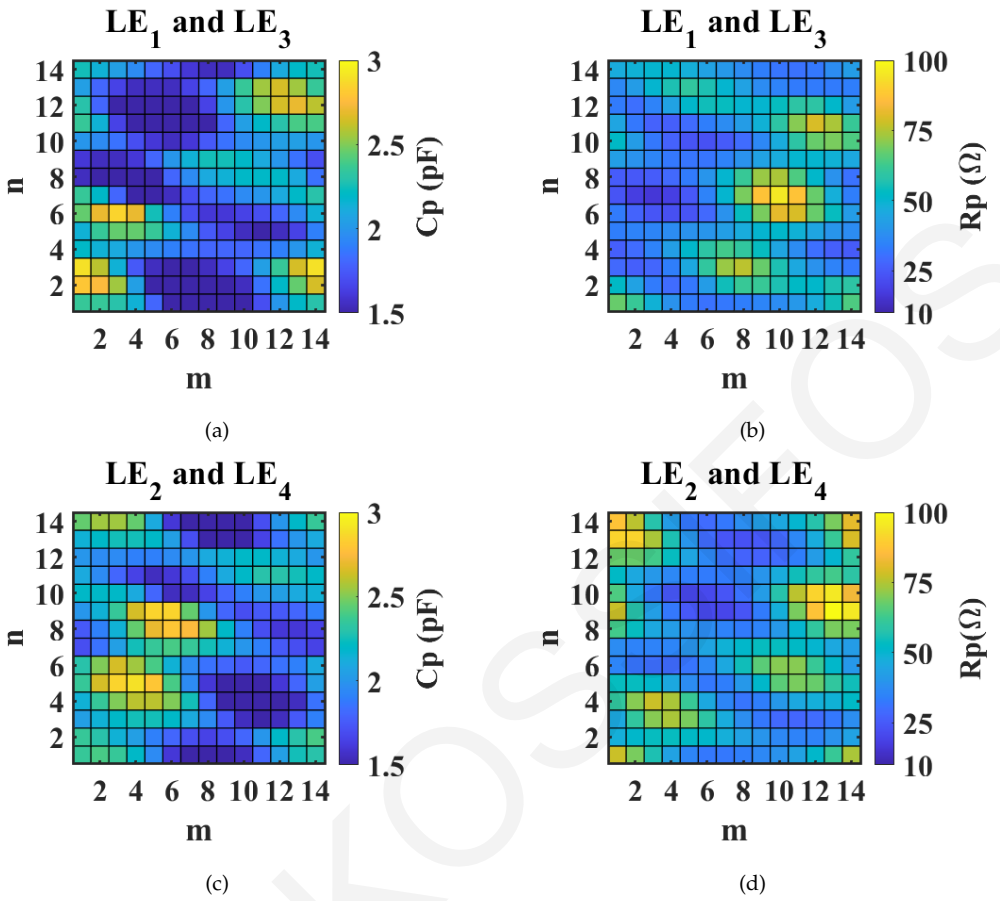


Figure 7.7: Translated LE's resistance and capacitance values to reproduce the reflection coefficients in Fig. 7.6. In (a) and (b) the capacitance and resistance values realized by LE_1 and LE_3, are plotted, respectively, and in (c) and (d) the capacitance and resistance values of LE_2 and LE_4, are plotted, respectively.

single beams. These calculated reflection coefficients to produce an OAM beam and a pencil beam are then added. These resulting reflection coefficients will produce the simultaneous pattern that contains a pencil beam and an OAM beam.

Here, an example is presented as a demonstration of arbitrary wavefront generation. An OAM beam that possesses mode equal to 1 (as in [18, 112]), and has LHCP at $\theta = 20°$ and $\phi = 150°$, is formed, together with a pencil beam at $\theta = 40°$ and $\phi = 270°$. A plane wave excitation at $\theta = 30°$ and $\phi = 0°$ is considered for demonstration.

The calculated reflection coefficients for both x and y polarizations and the translated RC values can be found in Fig. 7.9 and Fig. 7.10, respectively. The PMSF was simulated in Ansys HFSS and the obtained reflected pattern can be found in Fig. 7.11. In Fig. 7.11(a) the total BRCS is plotted in the uv coordinates, where an OAM beam and a pencil beam can be easily identified. In Fig. 7.11(b) a polar plot

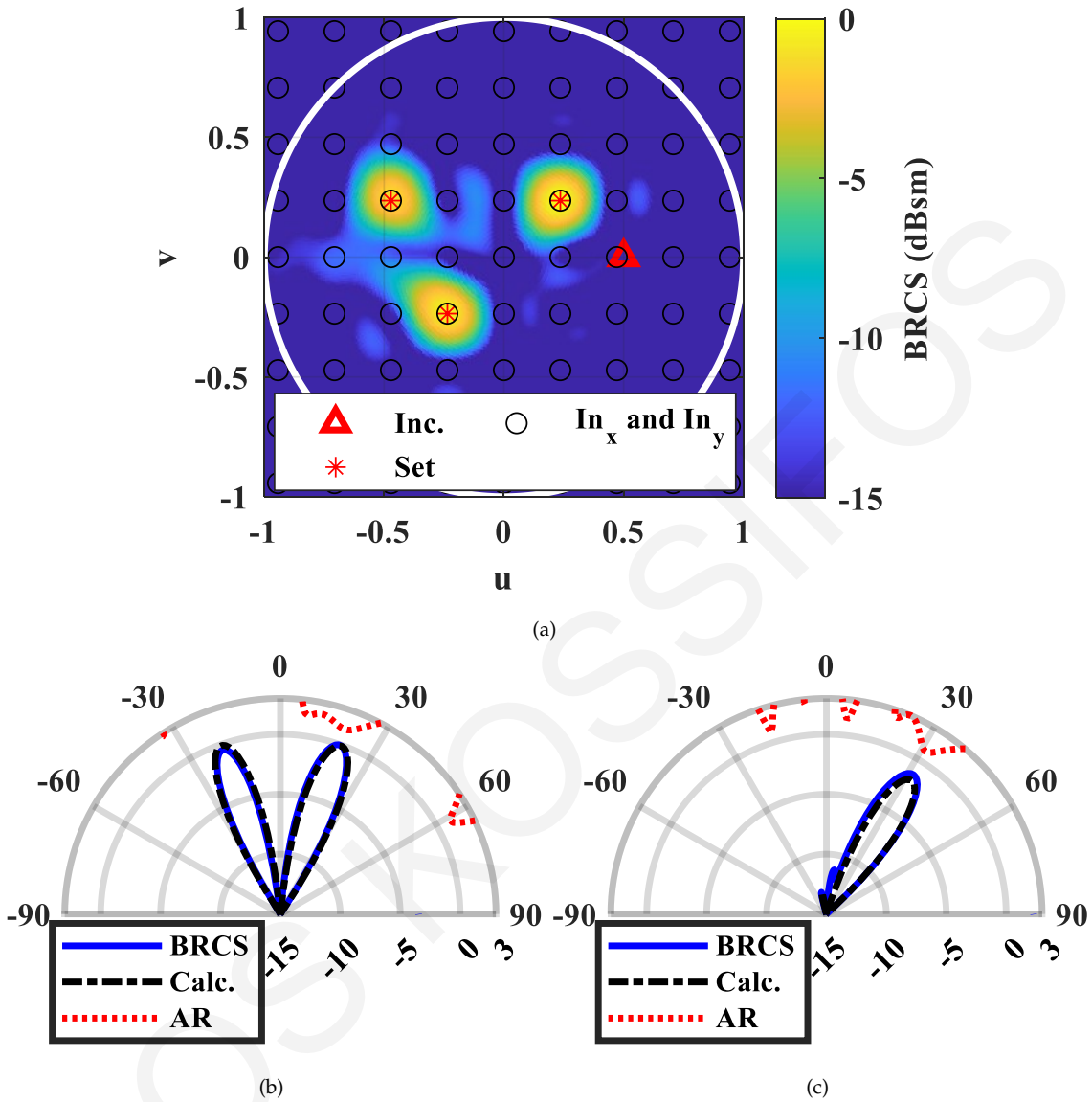


Figure 7.8: Simulated total BRCS in dBsm. (a) The results are overlaid with three In_x and In_y entries producing three pencil beams, together with the desired set direction and the incident wave direction. In (b) and (c) polar plots of the produced pattern shown in (a) overlaid with the axial ratio (AR) and the calculated far field for $\phi = 45°$, and for $\phi = 153°$, respectively.

of the total reflected electric field is plotted at $\phi = 150°$, overlaid with the calculated far field pattern using (7.1) and the simulated AR. The simulated pattern and the calculations are in good agreement, with an accuracy (Acc) over 98.6%, an efficiency (ε_{sc}) equal to 17.2%, and the AR of the OAM beam is below 3dB, demonstrating that indeed the OAM beam is circularly polarized.

7.5.4 Multibeam Half-Power Beamwidth Synthesis

In this section the wavefront synthesis capabilities of the proposed design are further demonstrated. This demonstration is done by not only adjusting the magni-

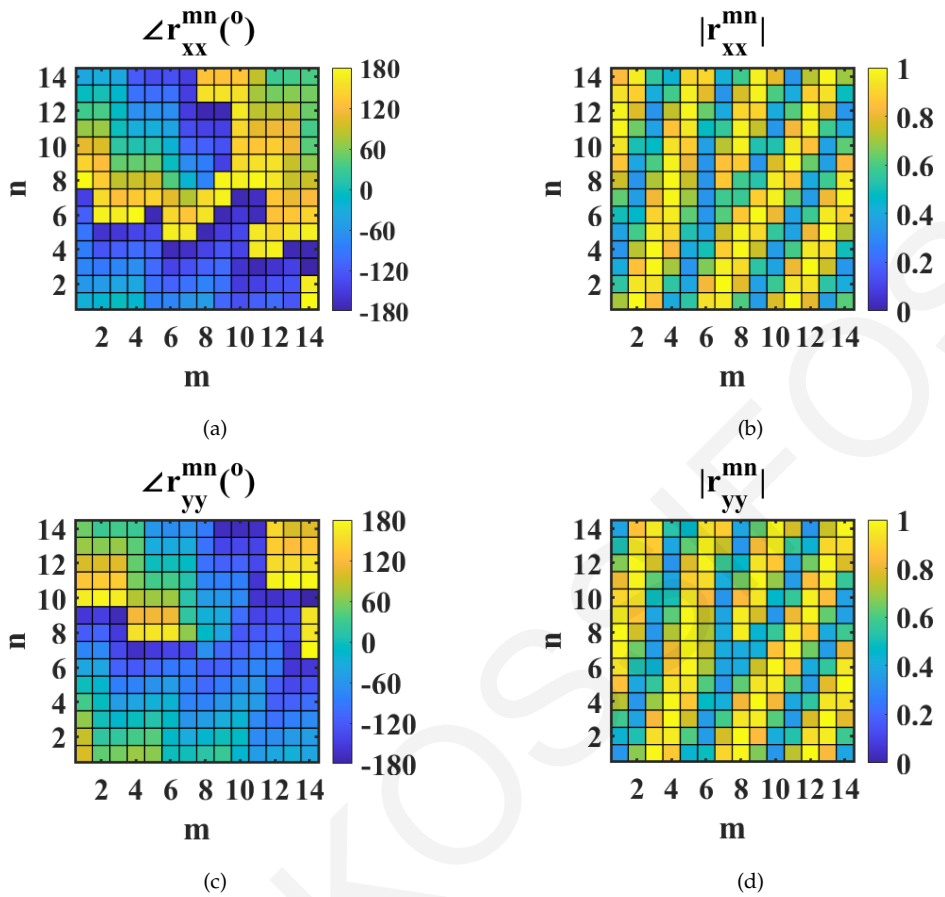


Figure 7.9: Reflection coefficients for both x-polarization (r_{xx}) and y-polarization (r_{yy}), calculated for the producing an OAM beam that possess mode equal to 1 and having LHCP at $\theta = 20°$, $\phi = 150°$ and a pencil beam at $\theta = 40°$, $\phi = 270°$ linear polarization. (a) Phase of the reflection coefficient for the x-polarization $\angle r_{xx}$ in degrees, (b) magnitude of the reflection coefficient for the x-polarization, $|r_{xx}|$, (c) Phase of the reflection coefficient for the y-polarization $\angle r_{yy}$ in degrees, and (d) magnitude of the reflection coefficient for the y-polarization $|r_{yy}|$.

tude and the polarization of multiple pencil beams but also by adjusting the HPBW of each beam. The HPBW for a Tshebycheff-error (Θ_{HPBW}) array is well known and can be calculated with [74]:

$$\Theta_{HPBW} \simeq 2 \arcsin\left(\frac{\lambda \sigma_T}{\pi\, D\, N}\sqrt{(\arccos R_0)^2 - \left(\arccos\frac{R_0}{\sqrt{2}}\right)^2}\right), \tag{7.17}$$

where the R_0 is the voltage ratio of the beam to the sidelobe level (SLL), and σ_T is the scaling factor:

$$\sigma_T = \frac{N}{\sqrt{A_c^2 + \left(N - \frac{1}{2}\right)^2}}. \tag{7.18}$$

The constant A_c is related to the voltage ratio with:

$$\cosh(\pi A_c) = R_0. \tag{7.19}$$

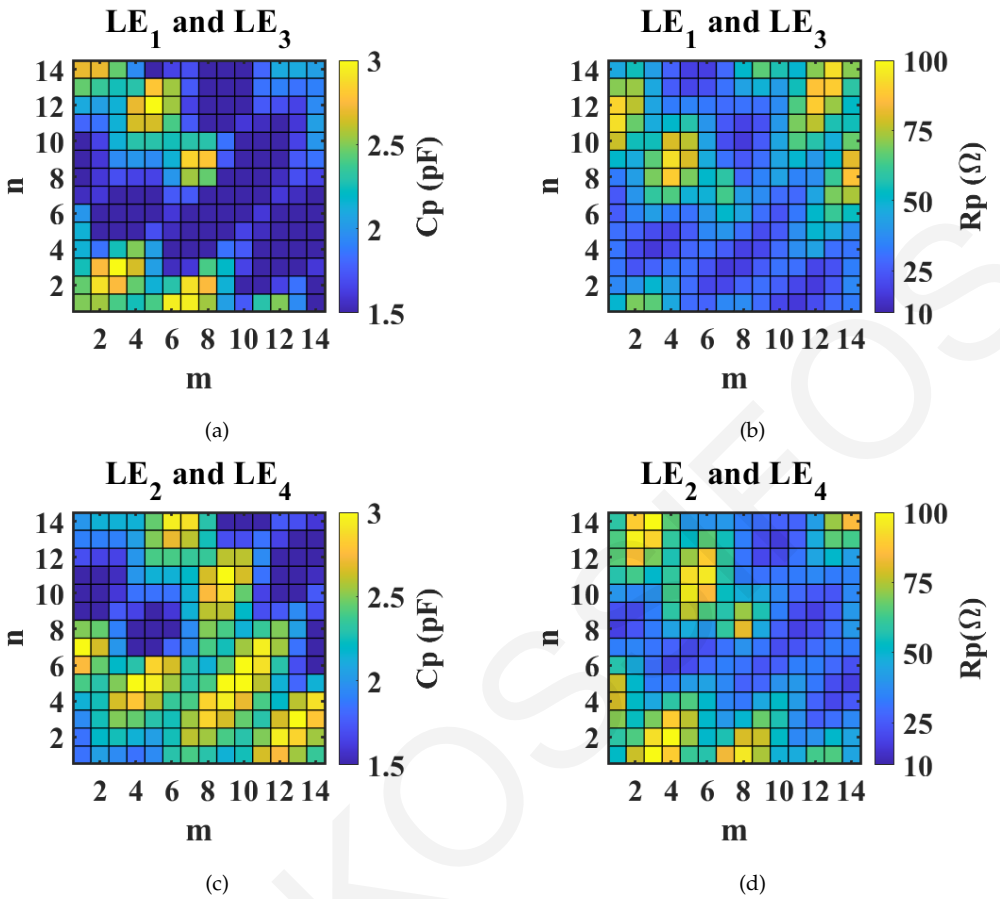


Figure 7.10: Translated loading element resistance and capacitance values to reproduce the reflection coefficients in Fig. 7.9. In (a) and (b) the capacitance and resistance values realized by LE_1 and LE_3, are plotted, respectively, and in (c) and (d) the capacitance and resistance values of LE_2 and LE_4, are plotted, respectively.

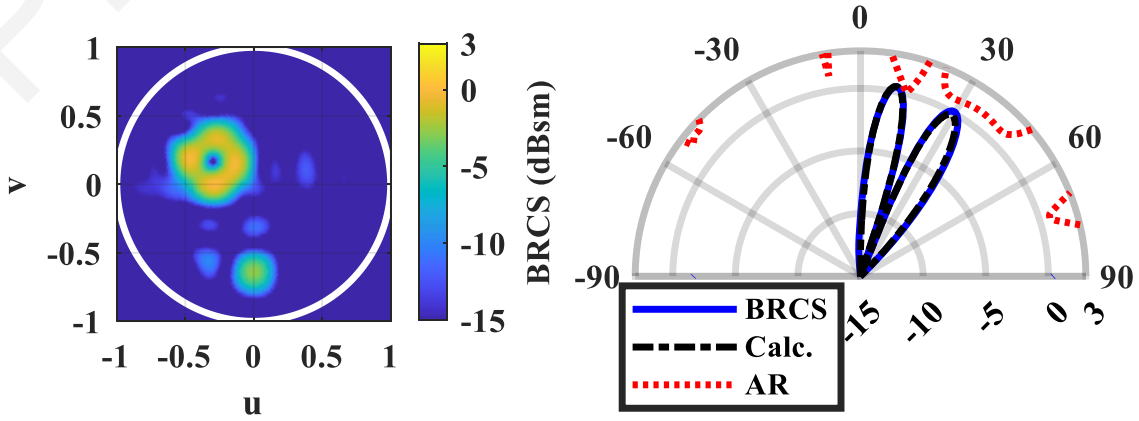


Figure 7.11: Simulated total BRCS in dBsm. In (a) the results are plotted in the uv coordinates. In (b) a polar plot at $\phi = 150°$ of the results is plotted overlaid with the axial ratio (AR) and the calculated far field.

The current excitations for a one-dimensional Tschebyscheff array are well known [150]. One can extend these excitations to a two-dimensional array, for an N×M array, by first computing the current excitations for the N number of elements (α_n), which can be rows or columns, and the current excitations for the M number of elements (α_m) which can be columns or rows. The two-dimensional array current excitations (C_{mn}) can be then computed by a simple outer product operation:

$$C_{mn} = \alpha_n \otimes \alpha_m. \tag{7.20}$$

For a total number of pencil beams equal to P, the current excitation can be different for each pencil beam produced and therefore the two dimensional array current excitation can be symbolised as C^p_{mn}. The element-wise product of the incident (i_{mn}) reflection (r_{mn}) coefficient matrices can be subsequently calculated using:

$$i_{mn}\, r_{mn} \;=\; \sum_{p=1}^{P=NoB} PB^p_{mn}\, C^p_{mn}, \tag{7.21}$$

where PB^p_{mn} is the single pencil beam's excitations. This can be easily calculated with [74] :

$$PB^p_{mn} = e^{-ik\rho_{mn}\Psi_{mn}}. \tag{7.22}$$

here k is the wavenumber and Ψ_{mn} can be calculated with:

$$\Psi_{mn} = \cos(\theta_{mn})\cos\left(\theta^p_0\right) + \sin(\theta_{mn})\sin\left(\theta^p_0\right)\cos\left(\phi^p_0 - \phi_{mn}\right). \tag{7.23}$$

here, the spherical direction of each p_{th} beam are written as θ^p_0 and ϕ^p_0 and the spherical coordinates of each unit are written with θ_{mn}, ϕ_{mn} and ρ_{mn}.

An example dual-beam pattern was produced where both beams' HPBW was set at 15°. The voltage ratio (R_0) was calculated to be equal to 25.15 (or 28dB). Here a plane wave excitation at 30° was considered, and the direction of the first beam was set at $\theta^1_0 = 25°$ and $\phi^1_0 = 90°$, and the second beam was set at $\theta^2_0 = 25°$ and $\phi^2_0 = 225°$. The magnitude of the first and second beam was set to be equal and their polarization was set to be LHCP and RHCP, respectively.

The calculated reflection coefficients are plotted in Fig. 7.12(a) to Fig. 7.12(d) and the correlated LEs' *RC* values are plotted in Fig. 7.12(e) to Fig. 7.12(h). The total BRCS is plotted in Fig. 7.12(i) and the simulated results show clearly two pencil beams at the desired directions. Since two individual pencil beams with an expected SLL equal to 28dB were produced the expected overall SLL should be at 25dB. This

is because the sidelobes of one beam are vectorially added to the second beam's sidelobes. This addition, in the worst case scenario where the sidelobe addition is constructive, this will result in the 25dB SLL.

For this 14×14 simulated PMSF the calculated SLL was not achieved, but the produced pattern obtained an accuracy (*Acc*) of 96.2%, and an efficiency (ε_{sc}) equal to 5.7%. The SLL degradation was most likely caused by the edge effects of the PMSF. Looking at the calculated reflection coefficients magnitude for both x and y-polarization in Fig. 7.12(b) and Fig. 7.12(d), respectively, the unit cells at the edge of the PMSF are set to produce a reflection coefficient of zero or a very small value. Naturally, this can't be achieved at edge unit cells which will cause a partial reflection and subsequently an SLL degradation. The LHCP beam's AR as can be seen in Fig. 7.12(j) at the direction of 25° was above 3dB, which indicates this could be affected by the edge effects also. The RHCP pencil beam plotted Fig. 7.12(k) achieved an AR which was also below 3dB. Fortunately, the desired HPBW was correctly set for both pencil beams, as can be seen from the polar plots in Fig. 7.12(j) and Fig. 7.12(k), a HPBW of 15° was achieved for both beams.

7.5.5 Discussion of PMSF's Capabilities

In all four examples shown above, and in general for all PMSF designs, small deviations between the calculated and simulated pattern can be attributed mainly to the PMSF's edge effects. The unit cells at the edge of the PMSF will not behave as expected with the set *RC* values implemented by the LEs, since they are no longer in a periodic environment. Furthermore, there could be small errors between the calculated reflection coefficients and the ones obtained from the loading elements. The *RC* combination might not perfectly satisfy each set reflection coefficient. Small deviations from the calculated reflection coefficients in this design will contribute to a partial specular reflection. Furthermore, simulation errors can be expected but due to the fine resolution of *R* and *C* round-off errors are eliminated and higher accuracy is obtained.

Looking closer to the simulated results in Fig. 7.5 and Fig. 7.8 it can be observed that when producing multiple beams with the presented DFT method there is a BRCS reduction, that is partially attributed to the energy being divided in various directions. An additional loss is caused by setting the reflection magnitude of

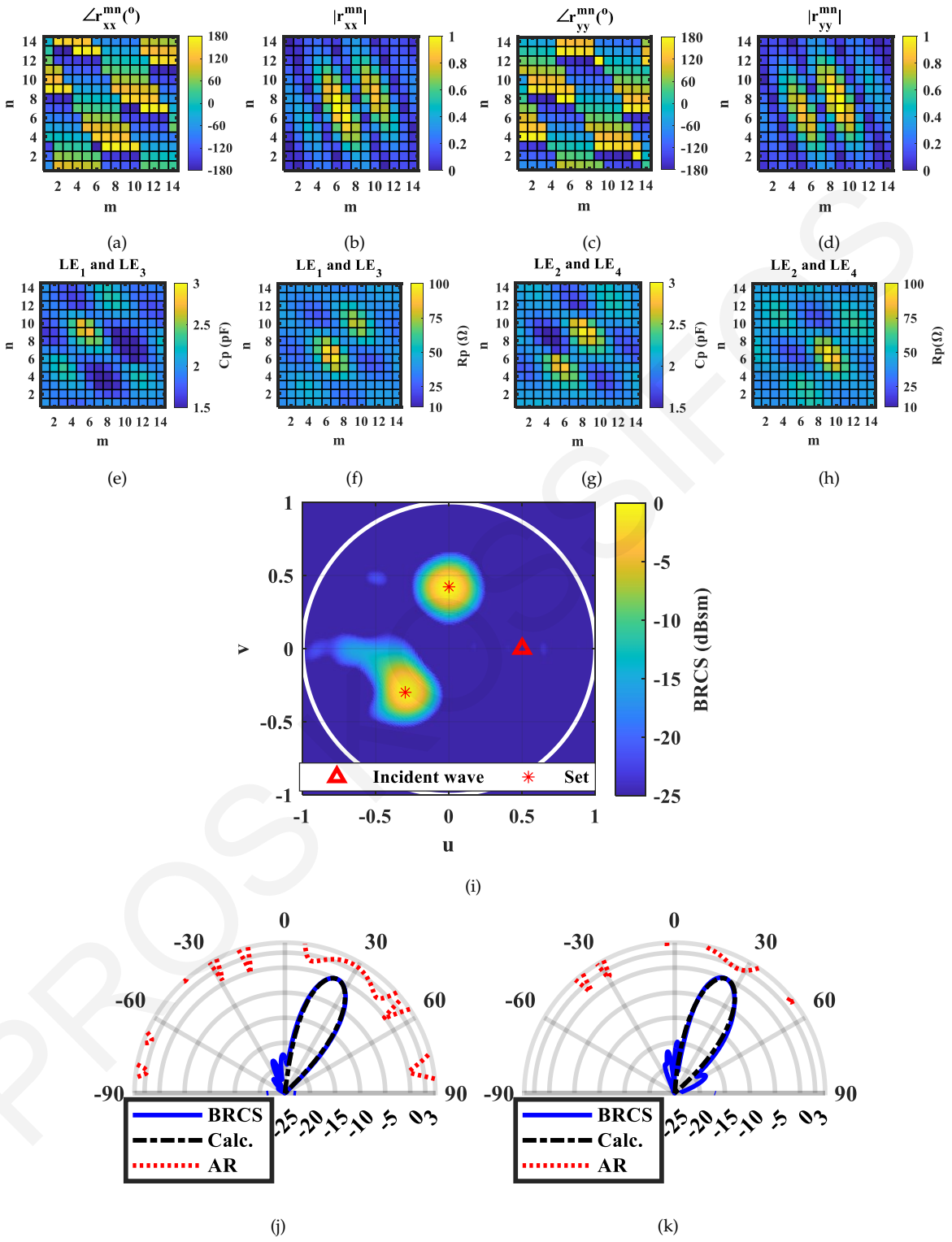


Figure 7.12: (a)-(d) Calculated reflection coefficients magnitude and phase to produce two pencil beams one at $\theta = 25°$, $\phi = 90°$, and the second beam at $\theta = 25°$, $\phi = 225°$, with LHCP and RHCP, respectively. The HPBW was set equal to 15°. The correlated LEs' *RC* values are plotted in (e)-(h). Simulated total BRCS in dBsm, can be found in (i)-(k). In (i) the results are plotted in the *uv* coordinates. In (j) and (k) polar plots comparison with calculated patterns and overlaid with the axial ratio (AR) for angles $\phi = 90°$ and $\phi = 225°$, respectively.

some unit cells to a smaller value, however this is a compromise in achieving the fastest computational times compared to other iterative methods [32, 36, 145, 146]. Alternatively, higher BRCS can be also achieved with this architecture by employing optimization on the LEs' *RC* values, albeit with the associated price of additional computation time. Fortunately, the scalability, low cost and low power achieved by the presented architecture allows one to scale up the PMSF size compensating for the BRCS reduction.

Larger PMSFs require higher power consumption and larger computation and reconfiguration time, but for this architecture this are not prohibitive. Assuming a large number of unit cells of 10,000, the presented architecture will require only 3.28 W, 10 ms to compute the reflection coefficients and 10 ms for reconfiguration Table 6.2, values which are sufficient for use in a realistic scenario, such as the one presented in Fig. 7.1.

7.6 Experimental Verifications

A 16×16 unit cell PMSF prototype design was manufactured, and its details can be found in Chapter 6 ([141]). The manufactured PMSF prototype can be seen in Fig. 7.13 in a planar near-field measurement system. The PMSF was illuminated via an ORWG probe, while an identical probe is used to sample the near field.

The incident electric field from the probe was measured by rotating it towards the measurement plane, and its effect on the reflected fields was compensated for in the calculations of the reflection coefficients (7.1). The reflection coefficients were calculated to produce a variety of far-field patterns containing pencil beams and OAM beams. The reflection coefficients were converted into DAC input values, which were then programmed to the individual ASICs of the PMSF.

The PMSF's raw near reflected field (rnE_r) was measured within a plane with dimensions of $0.775 \times 0.775\ m^2$, which is located at a distance of 0.57 m vertically above the PMSF, as shown in Fig. 7.13. In order to minimize any noise, reflections within the near field system and any back radiation from the illuminating ORWG, an absorber was placed above the PMSF and the plane was measured again. This measurement using the absorber (rnE_a) was subtracted from the near reflected field ($rnE = rnE_r - rnE_a$). The near field data (rnE) was transformed to the far field using a planar near-field to far-field method as described in Section 2.3.2.2 and [75]. Due to

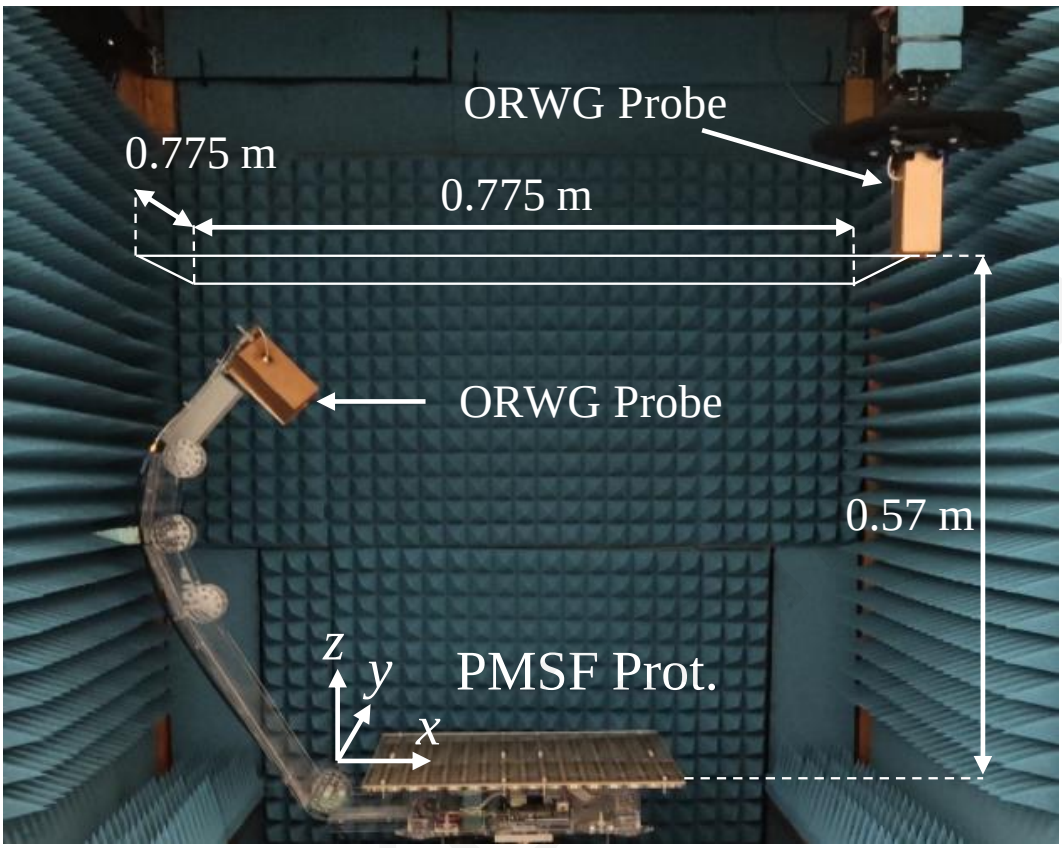


Figure 7.13: PMSF prototype in the planar near-field measurement system.

minor manufacturing imperfections the frequency of operation of the PMSF shifted from 3.6 GHz to 3.44 GHz, which translates to roughly a 5% frequency shift [141]. For this reason, all the following measurements were performed at 3.44 GHz.

The PMSF was configured to produce a single pencil beam, multiple pencil beams and a combination of OAM and pencil beams. The area of the near-field measurement plane and the distance from the PMSF limits the transformed far-field angular range to near-broadside angles [75], hence, the generated beams were set at angles near the broadside direction ($\theta \leq 20°$). The measurements can be seen in Fig. 7.14, plotted in the uv coordinates. An LP pencil beam was set at the broadside direction, and the measured gain and AR can be seen in Fig. 7.14(a) and Fig. 7.14(b) respectively. For this broadside configuration the results are also plotted in Fig. 7.14(c) and overlaid with the calculated pattern, the far field shows a clear pencil beam at the desired broadside direction (Fig. 7.14(a)) and an AR larger than 3 at the same direction (Fig. 7.14(b)), which are in good agreement with the calculations. Subsequently, two pencil beams were set, consisting of one CP beam at $\theta = 20°, \phi = 90°$ and one LP beam at $\theta = 20°, \phi = 315°$. The measured results for this configuration can be seen in Fig. 7.14(d) and in Fig. 7.14(e), where two pencil

beams can be easily identified at the set directions and with an AR below 2 for the CP pencil beam. The same measurements are overlaid with the calculated pattern in Fig. 7.14(f) and Fig. 7.14(g) for $\phi = 90°$ and $\phi = 315°$, respectively. Finally, in

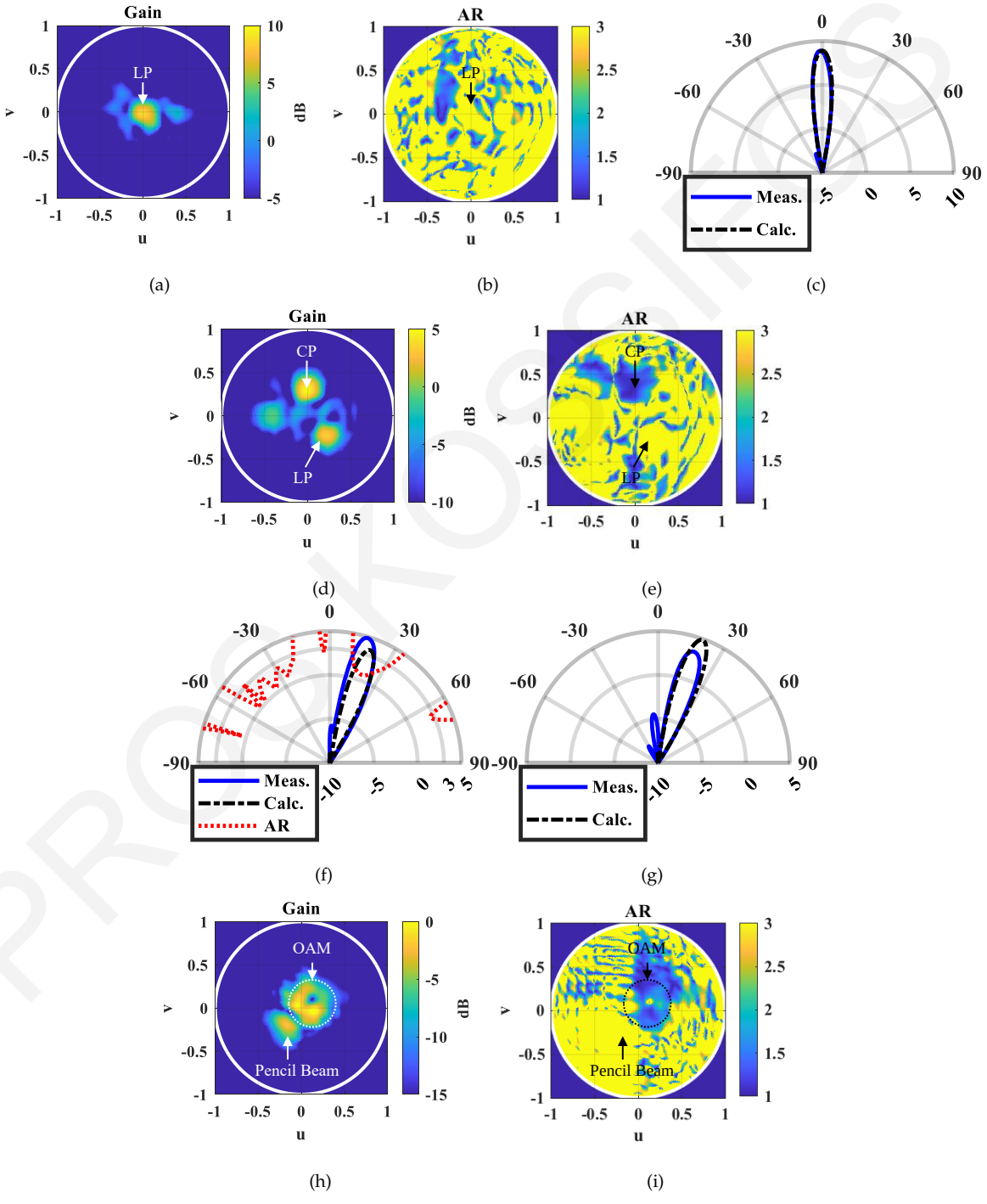


Figure 7.14: (a), (d), (h) Measured patterns in dB, and (b), (e), (i) axial ratio (AR) plotted over the *uv* coordinates for various PMSF configurations. In (a) and (b) an LP pencil beam was configured at broadside, in (c) this results are overlaid with the calculated pattern for comparison in dB. In (d) and (e) two pencil beams were configured, one LP and one CP, in (f) and (g) this results are overlaid with the calculated pattern for comparison in dB, for $\phi = 90°$ and $\phi = 315°$, respectively. In (h) and (i) one CP-OAM beam and an LP pencil beam were configured.

Fig. 7.14(h) and in Fig. 7.14(i) the far field pattern and the AR are plotted for a configuration of a CP-OAM beam with mode equal to 1 and an LP pencil beam. The OAM beam is set at the spherical direction $\theta = 10°, \phi = 45°$, while the LP pencil beam is set at $\theta = 20°, \phi = 215°$. The AR at the direction of the CP-OAM beam is below 2, indicating that the beam is indeed CP, while the AR at the direction of the pencil beam is larger than 3 indicating that the beam is LP.

The far-field patterns shown in Fig. 7.14, as all measurements, are subjected to experimental errors. Measurement errors in these far-field patterns arise from all the steps described in the measurement procedure. These include, errors from the reflection coefficient measurement described in Chapter 6, but also due to mechanical positioning errors in the near-field measurement system, and a misalignment of the illuminating ORWG probe. Despite these limitations, the abilities of the PMSF have been effectively proven with these representative experimental demonstrations.

7.7 Conclusion

A multifunctional and reconfigurable programmable metasurface (PMSF) design that involved the co-development of low power, low-cost application-specific integrated circuits (ASICs) has been presented. The ASICs offer an added flexibility to the PMSF design. Each ASIC integrates control circuits, digital-to-analog converters and four complex impedance loading elements. With this circuitry, the ASIC can provide four *RC* load in every unit cell with seemingly continuous tuning (2^{16} states) for all programmable resistance and capacitance elements within the LEs range. The design can perfectly absorb TE and TM polarized waves for wide angles of incidence, it can anomalously reflect an incident wave, and can create arbitrary wavefronts. With these capabilities, the design finds applications in future programmable wireless environments, where the PMSF can be installed in strategic locations in order to redirect an incident wave towards a user or absorb an interfering incident wave. Furthermore, the wavefront manipulation capabilities of the PMSF give it the ability to be incorporated into in the transmitting antenna. In this scenario, the antenna can create arbitrary wavefronts such as, OAM beams, and multiple pencil beams, while controlling the polarization of each pencil beam. The absorbing capabilities of the PMSF were presented and experimentally verified in Chapter 6 ([141]), by obtaining the reflection coefficient of both TE and TM polarizations. Here

in this chapter, the wavefront redirection and arbitrary wavefront generation capabilities were presented and experimentally verified. Experimental verification of the design was demonstrated with a single, dual pencil beams and a simultaneous OAM and pencil beam generation. The computational time to calculate multiple pencil beams was addressed in this chapter with a DFT synthesis method. The ability to control the polarization of multiple pencil beams can prove to be useful in advance 5G telecommunication technologies, as well as future 6G technologies. The PMSF can steer multiple beams in a programmable manner, to track multiple users in a cellular topology. Users that can adapt their receiver to various polarizations can take advantage of the increased signal power offered by the directed beam, but can also benefit from increased isolation from other users that employ different polarizations. This polarization agility can increase data rates in future telecommunication technologies. Not to mention that the absorption capabilities of the PMSF design provide the possibility of blocking individual malicious users at the physical layer, thus increasing cybersecurity. Furthermore, the PMSF design's dual polarization, magnitude and phase control can be utilized in near-field generation applications such as holography and imaging.

Chapter 8

Conclusion

A complete design methodology leading to an experimentally validated ASIC-equipped programmable metasurface (PMSF) design has been presented. The incorporation and design of ASICs in MSF designs is a challenging task that required a multidisciplinary approach. Like any other new technology, this MSF technology requires balancing of design performance, power consumption and cost. An example design was presented that can arbitrarily tailor wavefronts for the near field and far field.

8.1 Summary

In the development of this technology, a PMSF system level architecture was developed which embeds an ASIC within each of the PMSF's unit cells to address power, scalability and performance constraints. The feasibility of this architecture was presented with the exploration of three economically affordable semiconductor processes and an example PMSF unit cell geometry. The ASICs incorporate four complex impedance LEs, eight DACs and an asynchronous control circuit. The performance of this design has been evaluated in view of implementing tunable complex impedance LEs. A low cost and low power 180 nm silicon CMOS process was selected with a nominal supply voltage of 1.8 V. This technology demonstrated perfect absorption for TE and TM polarizations for a wide angle range at the design frequency of 5 GHz.

This process became commercially available in the late '90s. In it's second decade (at the time), it's PDK became mature and stable enough to implement the

ASIC as a system. The technology could meet the requirements of the ASIC's sub-components, the asynchronous circuits and the DACs, while satisfying the LEs' RF performance. The selected technology was validated through an MPW and on-wafer measurements. The LEs were designed with an innovative design methodology that increases the LE's achievable *RC* range and consequently improving the PMSF's performance. Each LE draws negligible current in the pA range, and its small size enables it to be incorporated with the DAC and control circuit in a small die. Therefore, the increased PMSF performance was feasible without compromising power or cost.

A second innovative ASIC-enabled PMSF was designed with advanced functionality. Its unit cell geometry was designed and optimized for multiple reconfigurable functions in the S-band around 3.6 GHz. The optimization was based on the experimentally measured effective *RC* range of the integrated MSF LE. The unit cell's top textured side consists of a cross-like structure which is rotationally symmetry. Due to this symmetry, the unit cell achieved independent and simultaneous control of the absorption of both TE and TM polarized waves with incident angles ranging from 0° up to 60°. With four complex impedance LEs in each ASIC, simultaneous and independent control of both TE and TM polarizations can be achieved.

This dual polarization amplitude and phase control was utilized to produce complex wavefronts. Complex wavefronts such as multiple pencil beams with flexible polarization control. Four pencil beams were demonstrated, where each pencil beam has a different polarization. A combination of linear, RHCP and LHCP polarizations was demonstrated. Furthermore, arbitrary wavefronts can be generated, and an example consisting of OAM and pencil beam pattern was produced.

A study was conducted on the effects of mismatch on this design. The mismatch effect was modelled as a normal distribution around the nominal or set varactor and varistor's *RC* values. A standard deviation ranging from 0% to 40% was considered. A 0% standard deviation is the ideal case, while a 40% (σ) is an extreme case, and a standard deviation of 10% is the expected mismatch variations in commercially available silicon technologies. For this standard deviation of 10%, the design degrades by 15% in its perfect absorption operation, while for dual-beam generation the results show only a minor sidelobe level increase. These results provide the confidence that manufactured PMSFs that use ASICs will perform well under normal mismatch variations.

The ASIC's key sub-components were verified in a second MPW intermediate step. After this verification, and a cautious contingency plan, eight ASICs were formed. These eight designs were the first family of low-cost, low-power, high-speed scalable ASICs for complex impedance adaptation at microwave frequencies. The ASICs' were manufactured on a full wafer scale and diced. On the diced ASIC's pads a UBM layer was deposited on which solder ball spheres were placed. The now WLCSP-ASICs were populated on PCBs and measured. The ASICs' static/dynamic power, maximum bit rate and *RC* range were measured. An ASIC design was selected, and using its measured *RC* range a multifunctional reconfigurable PMSF was designed. The design was optimized for improved magnitude, phase and incident angle range for both TE and TM polarizations. The design was manufactured and its magnitude and phase control were experimentally verified. Utilizing this control, perfect absorption was demonstrated for a wide incident angle range. Furthermore, this control was utilized for complex wavefronts generation. Complex wavefronts such as, polarization agile multi-pencil beam patterns and a combination of OAM and pencil beams. These complex wavefronts were experimentally verified using a custom near field system.

With this amplitude and phase control, the design finds applications in future programmable wireless environments. In these environments the PMSF can be installed in strategic locations, flush on the walls of surrounding buildings and can redirect an incident wave towards a user or absorb an interfering incident wave. Furthermore, the wavefront manipulation capabilities of the PMSF give it the ability to be incorporated into the transmitting antenna. In this scenario, the antenna can create arbitrary wavefronts, such as OAM beams, and multiple pencil beams, while controlling the polarization of each pencil beam. For this scenario, the computational time required to derive the amplitude and phase distribution on the PMSF is improved with a presented DFT synthesis method.

8.2 Contributions

The multidisciplinary work presented in this thesis has contributed to the RF-IC, the MSF, wavefront synthesis and telecommunication areas. This new technology had also contributions from the asynchronous control circuit and the ASIC's networking, which is not included in this thesis. This thesis only focuses on the author's

contributions. A list of the main contributions are listed below, the contributions are itemized starting with the bottom level contributions listed first, leading to the system operation contributions.

- Loading element (LE) design [22]: The author developed the first PMSF LE which was low cost and low power. These two requirements necessitated the design to be implemented in an economically affordable silicon process where it could be integrated with DACs and a control circuit. Ideally, in order to realize high-quality RF LEs, the whole integrated circuit would be designed in a high-frequency SiGe or GaAs process, however the large number of integrated circuits necessary to implement a large PMSF would render the cost prohibitively high. The design methodology of the LE reduced its losses, pushing the capabilities of silicon to the point where its tuning range could satisfy PMSF applications. The LE's size was compact enough so four LEs could be integrated along with DACs and a control circuit in a 2×2 mm^2 die. With four LEs integrated within the same IC, a planar MSF consisting of exponential tapers arranged in a cross-like structure could achieve independent and simultaneous control of the absorption of both TE and TM polarized waves with incident angles ranging from 0° to 60° by taking advantage of the IC.

- Programmable metasurface (PMSF) architecture [107]: Utilizing the four LE configuration as a foundation within each ASIC, the system architecture was implemented, the theoretical and practical framework towards the implementation of ASIC-enabled PMSFs was set. The system architecture can be applied in the future to other PMSF designs, and this is expected as more groups move to an ASIC-based solution instead of a COTS-based architecture.

- ASIC family for PMSFs [114]: This thesis describes the process and the steps taken to deliver the first family of ASICs that support the PMSF architecture. This PMSF architecture utilizes the complex impedance control provided by the LE at microwave frequencies as an enabler to countless multifunctional PMSF designs.

- Multifunctional and reconfigurable PMSF demonstration [43–45, 115, 116, 141, 142]: Utilizing the ASIC family, an example PMSF was manufactured and demonstrated amplitude and phase control over both TE and TM polarizations. With

this ability, the design experimentally demonstrated dual polarization perfect absorption and NF and FF arbitrary wavefront synthesis with polarization agility. The PMSF's dual polarization, magnitude and phase control can be utilized in near-field generation applications such as holography, imaging, in smart indoor/outdoor wireless environments, and 5G and future (6G) base-station applications.

- DFT multiple pencil beam synthesis [142] : Electrically large PMSFs often consist of hundreds of unit cells. The computational time to derive the amplitude and phase distribution on these planar PMSFs is significant and proportional to the number of beams calculated. A DFT synthesis method was developed whose computational time is not proportional to the number of beams, and compared to other work in the literature is significantly faster.

From this short list the most important contribution was the demonstration of the first ever multifunctional and reconfigurable PMSF. This contribution proves the validity of the designs through experimental validation and provided final justification. Of course this couldn't have been achieved without the previous contributions.

8.3 Discussion and Future Work

This ambitious and multidisciplinary project, with the goal to create ASIC-enabled PMSFs, delivered a working prototype. The prototype has increased functionality over its COTS-based PMSFs counterparts, while still addressing cost, reliability and scalability constraints. The prototype can control the reflection coefficients' amplitude and phase for both TE and TM polarizations. With this control embedded within each of the PMSF's unit cell, the prototype can perform multiple reconfigurable functions and finds numerous applications. Applications in imaging, sensing holography, indoor and outdoor smart wireless environments, arbitrary wavefront generation just to name a few.

The presented all-round solution's architecture is expected to be adapted in future systems but also retrofitted into current systems, in all these applications. MSFs are expected to reciprocally co-evolve along with all areas of science in the near future. Similarly, integrated technologies are expected to be assimilated in all

these PMSF designs to satisfy the growing need for increased functionality, low-power and low-cost electronics. As the PMSFs' functionality increases, the demand for electronics will increase and other groups will adapt the presented architecture.

In the adaptation of the presented architecture to an application, the general constraints (functionality, cost, reliability and scalability) can also be adapted. One constraint can be alleviated, while the weight among others will get redistributed. In a PMSF basestation antenna application, where the size of the planar structure is relatively small, scalability constraints will be alleviated and the need for networking within the PMSF diminished. This is not the case for all applications, for smart wireless environment, where PMSFs cover whole walls, scalability is crucial. Furthermore, in PMSF basestation antenna applications, the power consumption of the PMSF is negligible compared to the total power of the whole RF chain, so an opted solution might be to invest or improve in some other aspect, such as the efficiency of the high-power amplifier.

This adaptation will spark many areas of research in all of the PMSF's levels. From the device level to the system level, a short list of areas of research follows:

- Integrated RF/MW components: Integrated RF and MW components come with advantages and disadvantages. RF/MW components even in mature semiconductor processes need improvement, and component accuracy and reproducibility need to be addressed. Cost and sustainability is expected to drive silicon processes to increase their cut-off frequencies. Other semiconductor process like SiGe or GaAs can potentially be adopted in PMSF designs as they become more economically affordable. All the component in the RF-IC designer's arsenal will find their way into various PMSF designs depending on the application, components like micro-electromechanical switches and schottky diodes just to name a few. This arsenal is also expected to increase with some potential candidates being memory components [151], but their development at RF and MW frequencies is still at its infancy.

- Integrated analog and digital components: Other approaches in the digital and analog part of the ASIC can be explored to increase speed and reduce power consumption. Analog-to-digital converters can be incorporated within the ASIC and provide feedback in future ASICs on the LE state.

- Three-dimensional IC: Three-dimensional IC processes can be explored as they

become more economically viable. These processes provide the possibility to isolate the RF substrate from the low frequency digital and analogue substrate.

- Analytical electromagnetic modelling: Analytical modelling of periodic structures like the unit cells of a PMSF become inaccurate when their complexity increases and deviates from the well understood shapes (e.g. wires, rectangular and spheres). This inaccuracy is further amplified when the unit cell is loaded with either a time-invariant or periodical variable or even time variable load. Analytical modelling of these electromagnetic structures in periodic and semi-periodic environments hasn't progressed much in the past decade. Work in this direction will help increase the PMSF's performance.

- Metasurface wavefront synthesis: A plethora of wavefront types have been generated from a metasurface design. Wavefront synthesis is generally an abstract layer that is detached from the physical layer, in this case the metasurface. Very little work has been done at the moment in which this layer is aware of constraints implied by the MSF layer. An exploration of synthesis methods tailored to the metasurface constraints can be explored.

- Smart programmable wireless environments: Smart programmable wireless environments are a relatively new concept. Its commercial implementation still requires significant effort, which can be explored.

- Implementations in the high GHz and THz region: With the constant trend towards higher operation frequency, an investigation of a PMSF operating in the high GHz to THz region is strongly advised.

- Transparent PMSFs: Transparent to the visible electromagnetic spectrum PMSFs are ideal for the implementation of smart programmable wireless environments, since they can occupy large surfaces without compromising windows on building or vehicles.

These ideas are just a sample on possible courses for the continuation of this work. The exploration in more than one area will yield a far greater improvement, open new roads and possibly new applications. The applications of PMSFs in all their areas are promising, as they provide new opportunities. Already, many companies

have pushed toward PMSF commercialization and the market share for PMSFs is growing [152–156].

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Appendix A

Near Field Measurement System

The custom near field (NF) measurement system that was developed for the experimental validation of this thesis, is briefly described in this appendix. The system was developed to have the flexibility to perform the measurement for the MSF prototype presented in Chapter 6 and Chapter 7.

In order to satisfy the experimental validation of the produced PMSF, the NF measurement system needed to perform:

- Bistatic measurements, these are needed for the PMSF's reflection coefficients measurement, and
- Planar NF measurements, as to implement the simplest NF to FF transformation in order to obtain the produced FF complex wavefronts.

In order to incorporate some extra degree of freedom, and be able to perform more complex measurement in the future, cylindrical and spherical NF measurements were added. These were optional requirements on the NF system, since the PMSF experimental validation can be satisfied without them. The bistatic measurement for a PMSF operating at 3.6 GHz, dictated the minimum volume of the chamber. In order to accommodate planar, cylindrical, and spherical NF measurements, five axes of movement are needed. For the plane measurement, three axes are needed, two for the x and y movement, and one for rotating the measurement probe, as needed to measure the two orthogonal fields E_x and E_y (see Fig. 2.25). This can be implemented by a plane stage and a rotational module mounted on the plane stage. The spherical NF measurements need also tree axes, two for a spherical movement (θ and ϕ) and one for the probe rotation (see Fig. 2.27). The probe rotation can be shared between the planar and spherical measurement. This brings the total axes to five. The remaining, cylindrical measurement can use one linear axis from the planar stage for the z axis movement, and one rotation axis from the spherical stage for the ϕ rotation (see Fig. 2.26).

A.1 System Overview

The electrical top-level diagram of the NF measurement system can be seen in Fig. A.1. It consists of three mechanical actuator modules, a spherical stage module, a rotation probe module, and a plane stage module. On a laptop, a control program is executed to control these modules through a microcontroller, while collecting the measurement points with the use of a VNA.

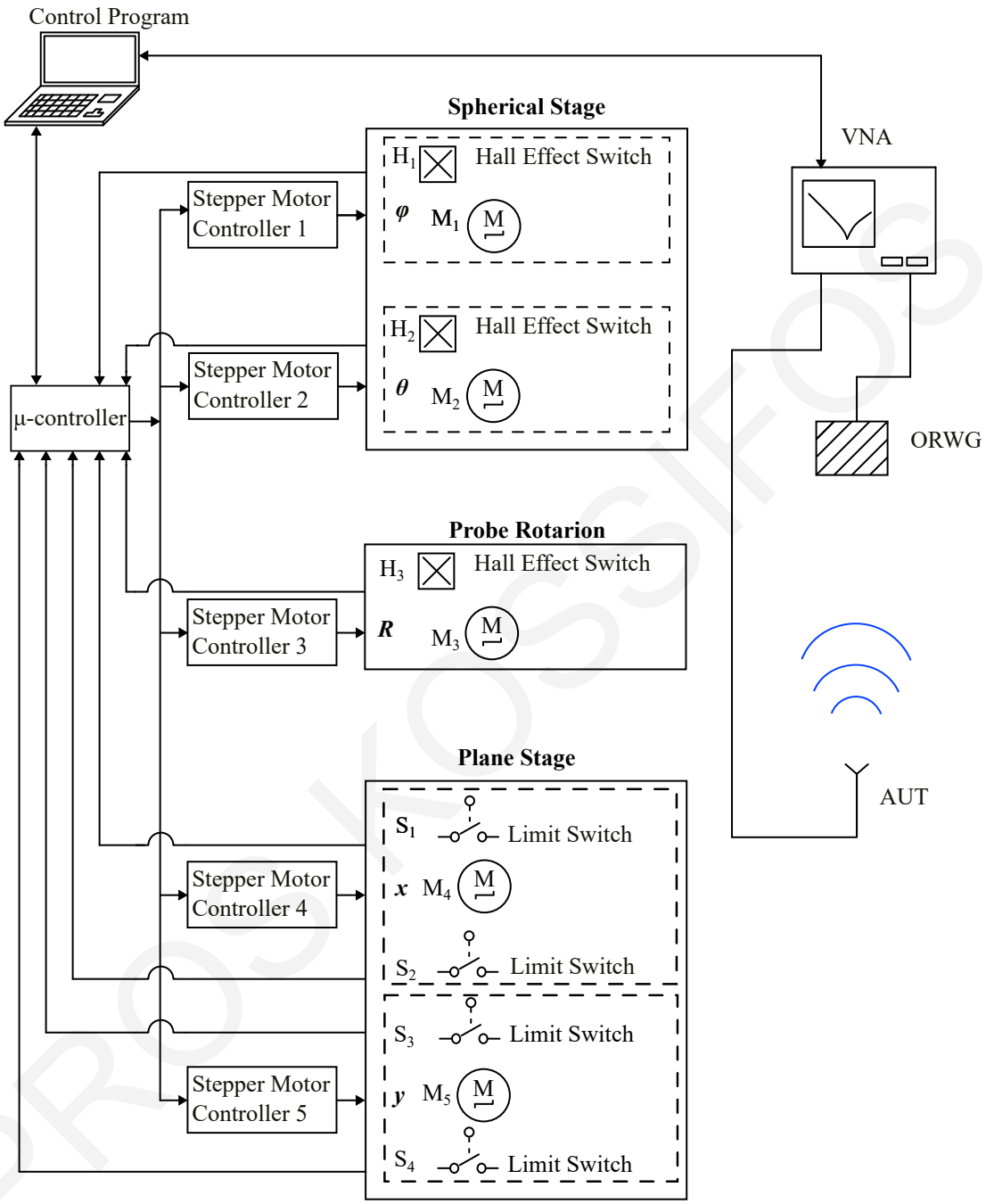
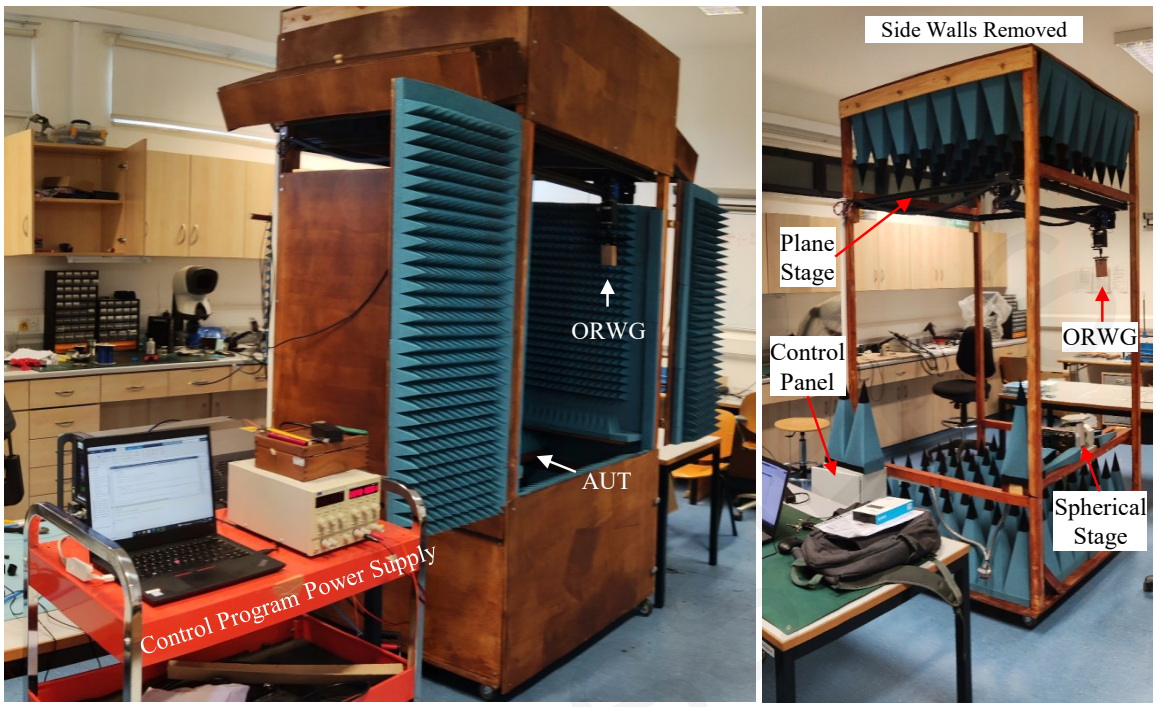


Figure A.1: Top-level diagram of the custom near field (NF) measurement system.

A control function was build in MATLAB. This function was used to control a stepper motor though a microcontroller while monitoring a HOME position with the use of a switch. HOME alignment subroutine was developed for the initialization of this function. This control and HOME alignment functions were used in the actuation and HOME alignment of all the actuator modules by incorporating stepper motor, stepper motor controller, and sensor settings as variables in the code. These variables are used for to calculate the number of pulses needed to be sent to the stepper motor controller in order to obtain the physical rotation or linear movement. A variable is also used for the sensor voltage translation to its corresponding ON or OFF setting.

This control and initialization function, was first adapted to the probe rotation module. This module is controlled by stepper motors M_3, and its HOME position is monitored by a Hall effect switch H_3. The spherical stage module is actuated by



(a) (b)

Figure A.2: Realised custom near field (NF)-measurement system (a) with, and (b) without its side walls.

two axes, one for θ and one for ϕ. The two corresponding stepper motors for θ and one for ϕ are M_1 and M_2, respectively. Their home position is monitored by two Hall effect switches H_1 and H_2. The plane stage movement to the x and to the y axis direction, is actuated by stepper motors M_4 and M_4, respectively. Two switches are used in both linear actuators to determiner their beginning and end, S_1 and S_2 for the x axis and S_3 and S_4 for the y axis.

Two ports of the VNA are used in this NF measurement system. One is connected to a ORWG, while the other is connected to the AUT. The VNA's settings, like frequency range, power level, IF bandwidth etc. are controlled from the laptop.

With the control over five axes provided by the plane stage, spherical stage, and probe rotation modules, spherical, cylindrical and planar NF scanning can be implemented. This NF scans can be then transformed into the far field (FF) with the use of well the NF-FF transformations methods, which were described in Section 2.3.2.

A.2 NF Measurement System, Realization

The realised measurement system can be seen in Fig. A.2. The system stands over 2.5 m tall, and is 1.75 m in width. In Fig. A.2(a), the front windows are open to show the NF system's interior, which is covered with pyramidal absorbers. The ORWG probe can be seen in the same figure, mounted on the plane stage. The AUT is placed below the plane stage (on the spherical stage), and is indicated in the figure. The control program was executed on a laptop, and a bench-top power supply was used to power the system.

In Fig. A.2(b), the system can be seen without its side walls, during its development. In Fig. A.2(b), the spherical stage is move to the front so it can be seen clearly, and as mentioned earlier, is where the AUT is mounted in this system. A control

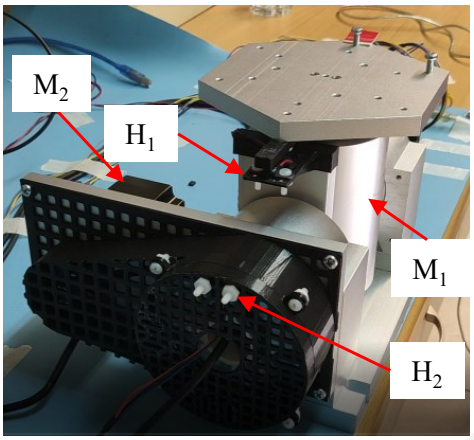
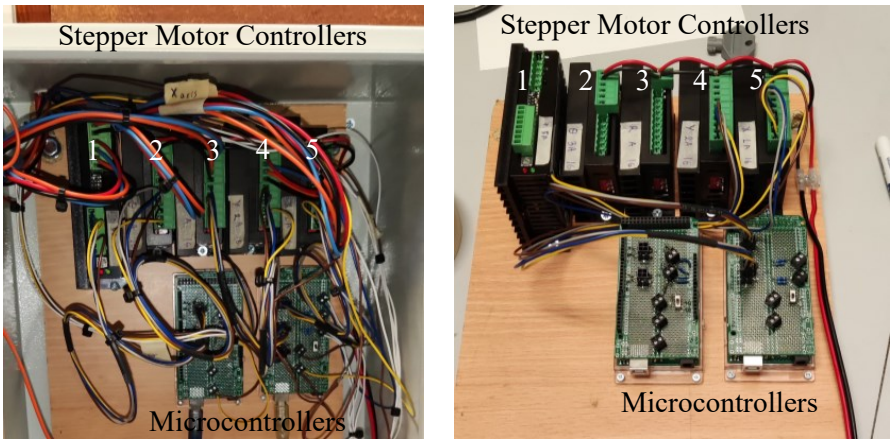


Figure A.3: Spherical stage implementation.

panel was developed and its location can be seen in Fig. A.2(b). The spherical stage can be see in Fig. A.3, and the location of the stepper motors M_1 and M_2 is indicated. These motors are used for the ϕ and θ rotations, respectively (see Fig. A.1). The motors are Nema23, 3.5 A, 78 mm in length, 2.2 Nm stepper motors. M_1 is directly couple to the ϕ axis while M_2 goes to a 1:8 synchronous pulley induction. The home switches, H_1 and H_2 can be seen in the same figure mounted on 3D printed part, screwed on the original stage [157].

The plane stage was a generic two axes CNC stage, it was converted by mounting on it probe stage and adding limit switches at the start and stop locations of both axes (x and y) [158]. The x axis is actuated by a Nema24 stepper motor, while the y axis with two Nema24 stepper motors wired to rotate in opposite directions.

The control panel houses all five stepper motor controllers and the microcontroller module. It can be seen in Fig. A.4(a), where the stepper motor controllers are numbered as indicated in the top level diagram in Fig. A.1. The microcontroller module was implemented using two ARDUINO MEGA 2560 boards, and custom shields to connect various cables headers. The control panel can also be seen in Fig. A.4(b) with the majority of the cables removed.



(a) (b)

Figure A.4: Control panel implementation. (a) The wired control panel, and (b) wires and connectors removed.

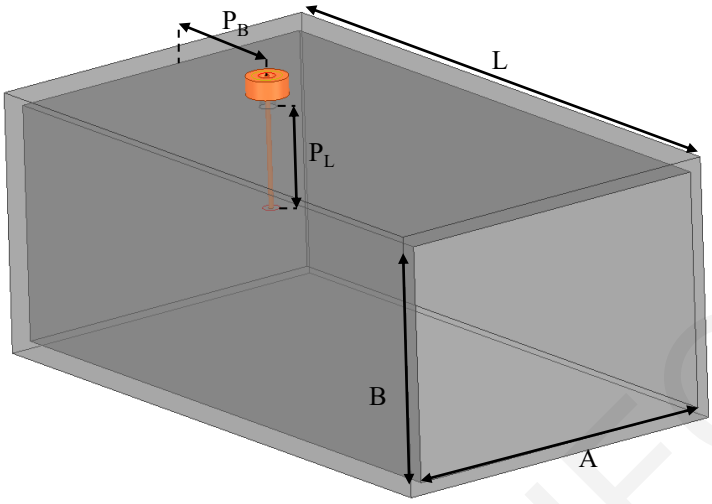


Figure A.5: Designed ORWG probe geometry to operate at 3.6 GHz.

Table A.1: ORWG probe geometry parameters.

Geometric Parameter	Dimension (mm)	Description
A	54	Probe Width
B	38	Probe Height
L	100	Probe Length
P_B	26.5	Port Distance
P_L	16.3	Port Wire Length

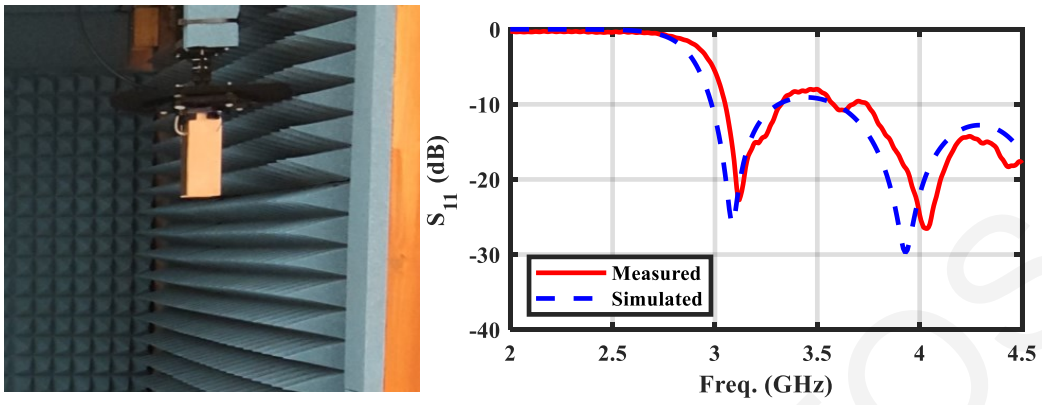
A.3 Open-Rectangular-Waveguide Probe

The ORWG probe was designed to satisfy the measurements for the PMSF prototype presented in this thesis. The PMSF was designed to operate at 3.6 GHz, and therefore the probe needed to operate at that frequency range. The ORWG probe was designed and optimized in ANSYS HFSS, its geometry can be found in Fig. A.5 while its geometric parameters can be found in Table A.1.

The probe rotation module is shown in Fig. A.6(a). A 3D printed housing was implemented to mount M_3, and attach to the plane stage. On the M_3 motor's axle, a second 3D printed part was connected where the ORWG probe can be installed. The two parts are covered with absorber sheets to reduce their reflections in the NF system. In the same figure, the manufactured ORWG probe can be seen installed on the probe rotation module.

The ORWG probe was manufactured with readily available copper sheets that were cut to the right dimensions and soldered. A semi-rigid coaxial cable was used to implement the copper wire with length P_L insight the probe. The cable's outer conductor was striped at a length P_L, and soldered at a hole that was drilled at the center of the larger dimension of the probe A, and at a distance P_B from its back wall.

The measured S_{11} of the ORWG probe can be seen in Fig. A.6(b) and overlaid with the simulated S_{11}. There is good agreement between measurement and simulated S_{11}. The probes lower cut-off frequency was measured at 3.1 GHz, while in simulation it was at 3 GHz. The ORWG operates for the remaining measurement frequency bandwidth in Fig. A.6(b), 3.1 GHz to 4.5 GHz, with an S_{11} which is below -10dB.



(a) (b)

Figure A.6: (a) Probe rotation module, and (b) measured S_{11} in dB of ORWG probe.

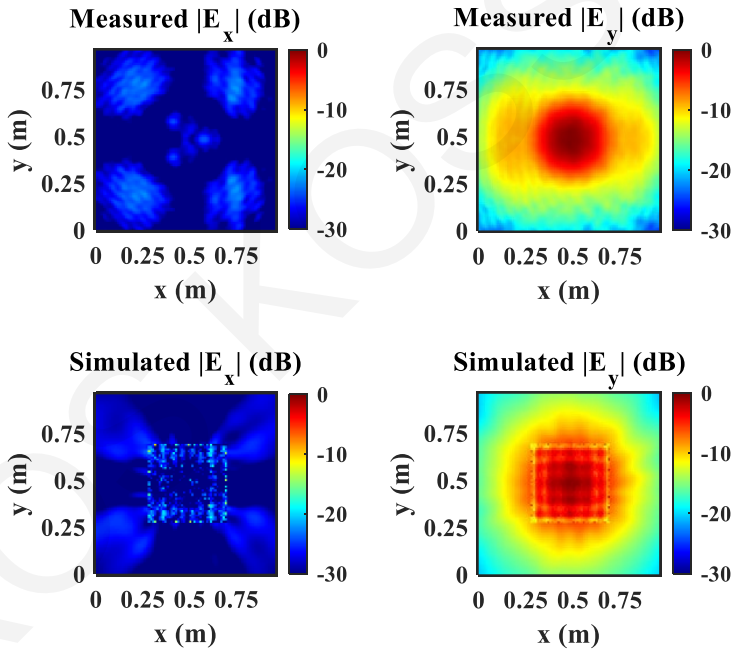


Figure A.7: Measured and simulated electric field at z_{obs} = 29.3 cm for ORWG probe shown in Fig. A.6 at 3.6 GHz. The sampling steps Δ_x and Δ_y were set to $\lambda/4$ at the higher measured frequency, 4.5 GHz.

Two "identical" ORWG probes were build for the purpose of performing a planar NF measurement. By placing one ORWG probe in the AUT position, and a second in the probe rotation module, the ORWG probe planar NF data was measured. The distance of the AUT and the measurement plane was set to 29.3 cm, while the discrete sampling steps (Δ_x and Δ_y) were set to $\lambda/4$ at the higher measured frequency of 4.5 GHz. The measured two orthogonal electric field components (E_x and E_y) are plotted in Fig. A.7 along with the simulated NF data. There are differences in the measured data, which are expected and originate from the probe's response.

This probe effect can be removed or compensated in the FF. Since both the AUT and the measurement probe are "identical", in this case we can adapt the "probe-square-root" method [159] to compensate the measured FF patterns. The simulated and measured E_x and E_y fields (Fig. A.7) were transformed to the FF. This transformed FF patterns are plotted in Fig. A.8 along with simulated FF patterns.

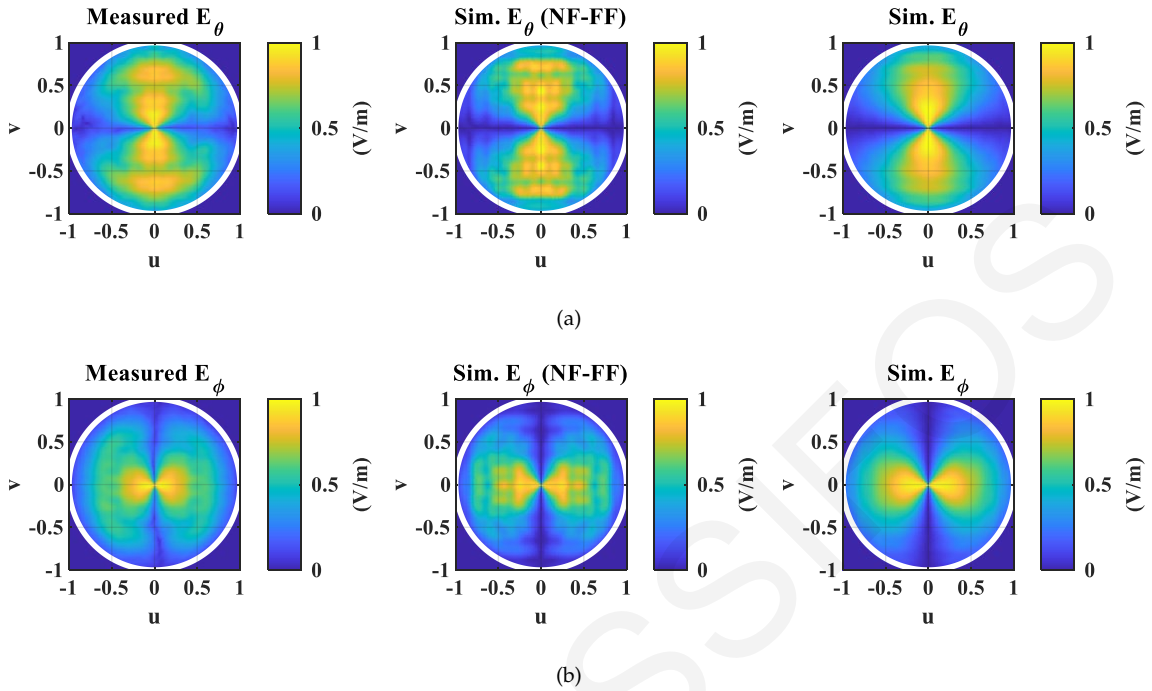


Figure A.8: Electric field comparison between measured, simulated NF data that have been transformed to the FF (NF-FF) and simulated FF data. (a) E_θ, and (b) E_ϕ in (V/m).

In this comparison, the simulated FF are the ideal case, in the simulated NF data that were transformed to the FF ("Sim. NF-FF", in Fig. A.8), were truncated and discretized. This truncaiton and discretization, is also present in the measurement, and therefore, the "Sim. NF-FF", aid in the evaluation of the measured FF. By measured FF patterns, the FF pattern obtained when performing a planar NF to FF transformation on the measured E_x and E_y plotted in Fig. A.7 is considered. By plotting the simulated NF-FF we can identify the effect, or contribution of the truncation and the discretization errors in the NF to FF transformation.

In Fig. A.8(a) and Fig. A.8(b) the normalised E_θ and E_ϕ are plotted, respectively. There is good agreement in the measured FF and the simulated NF-FF patterns. There is some discrepancy between simulated NF-FF and simulated FF data and subsequently with the measured data. This discrepancy is mostly due to the truncation of the measurement to a finite plane area (as shown in Fig. A.7), and not to the discetization since the sampling steps Δx and Δy were set to be well below the $\lambda/2$, to avoid discretization errors (Section 2.3.2.2).

The small differences between measured and simulated NF-FF can be caused by variations in the manufactured probe, or from the measurement set-up. These deviations can be caused by small imperfections in the manufactured probes or any mechanical misalignment and positioning errors, just to name a phew possible reasons. The measurement of the probe was considered a success and the NF measurement system functioned which was encouraging.

A.4 NF System Verification

An antenna was designed and manufactured for the purpose of being the illuminator of the PMSF in various wavefront manipulation scenarios. The initial testing of this antenna would also serve as a verification of the NF measurement system.

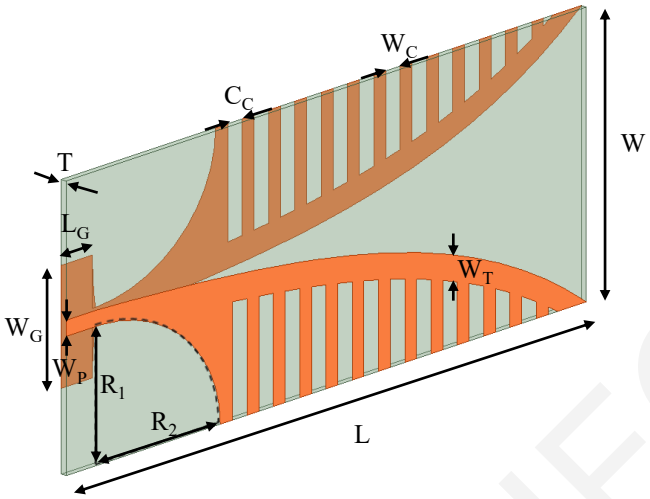


Figure A.9: Antipodal Vivaldi antenna geometry.

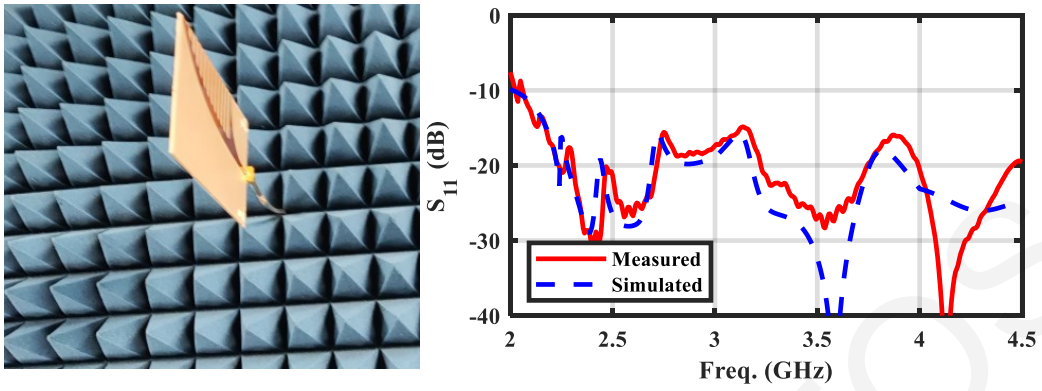
These tests, even though they are not exhaustive to the abilities of the NF system, they are essential, and were needed to be performed before any other measurement. A lightweight antipodal Vivaldi antenna was chosen for this purpose [160, 161].

The antenna was designed in ANSYS HFSS, and its geometry is shown in Fig. A.9. The antenna manufactured on a Rogers RT duroid 6202 laminate with a thickness equal to 1.524 mm. This dielectric has a relative permittivity (ε_r) of 2.9 and a dielectric loss tangent ($\tan\delta$) equal to 0.0015. The antenna's geometric parameters can be found in Table A.2.

The manufactured antenna can be seen in Fig. A.10(a). The antenna was installed in the NF measurement's AUT position. Its vertical distance ($z_{obs.}$) from the probe was adjusted to 29.3 cm. The measured S_{11} of the antenna can be seen in Fig. A.10(b) overlaid with the simulated S_{11}, and they are in good agreement. The measured and simulated S_{11} are below -10 dB from 2.1 GHz and covers the remaining measurement range, upto 4.5 GHz.

Table A.2: Antipodal Vivaldi antenna geometry parameters.

Geometric Parameter	Dimension (mm)	Description
T	1.524	Substrate Thickness
L	170	PCB Length
W	72	PCB Width
W_P	3.9	Port Width
W_C	3.85	Corrugation Width
C_C	4.7	Corrugation Cut
W_T	6.5	Taper Width
W_G	0.15	Ground Width
L_G	2.00	Ground Length
R_1	34	Eclipse First Radius
R_2	40.3	Eclipse Second Radius



(a) (b)

Figure A.10: (a) Manufactured Vivaldi antenna installed as a AUT. (b) Measured and simulated S_{11} in dB of Vivaldi antenna.

The measured electric field for both orthogonal components (E_x and E_y) is shown in Fig. A.11. The measured E_x compared to the simulated E_x is wider along the y direction. This is most likely due to a manufacturing imperfection of the antenna. A beam being narrower can be attributed to the probe effect on the NF data.

The measured and simulated data of Fig. A.11 were transformed to the FF and the transformed data can be found in Fig. A.12, plotted over the uv coordinates. The normalised E_θ and E_ϕ are plotted in Fig. A.8(a) and Fig. A.8(b), respectively. Simulated FF patters are also plotted for comparison. The patterns are in good agreement with each other.

Polar plots of the data in Fig. A.12 are plotted in Fig. A.13. The normalised E_θ is plotted in Fig. A.8(a) for a $\phi = 0°$, and normalised E_ϕ is plotted in Fig. A.8(a) for

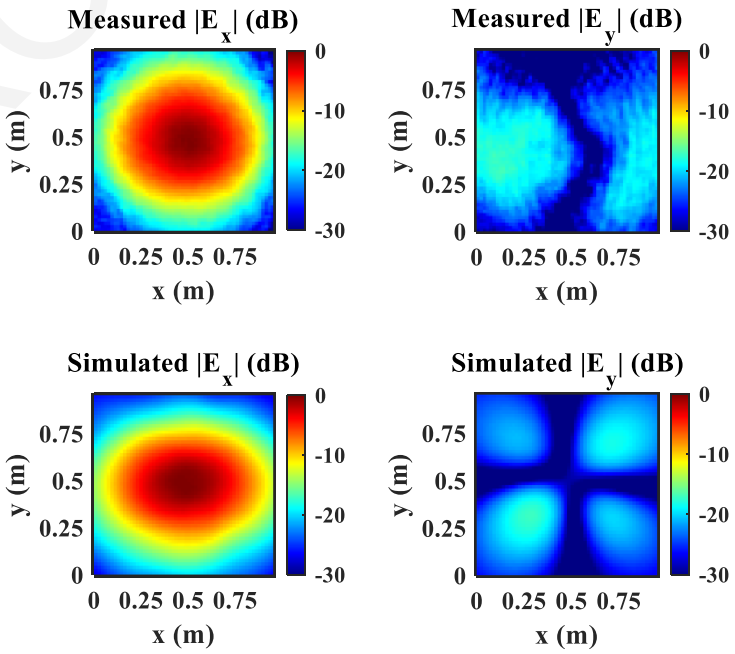
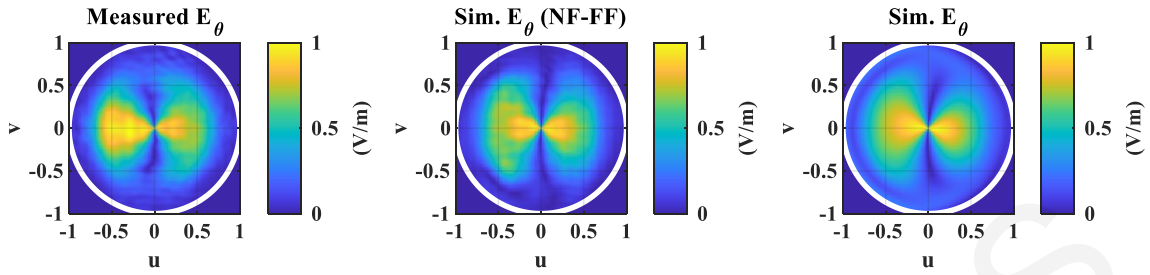
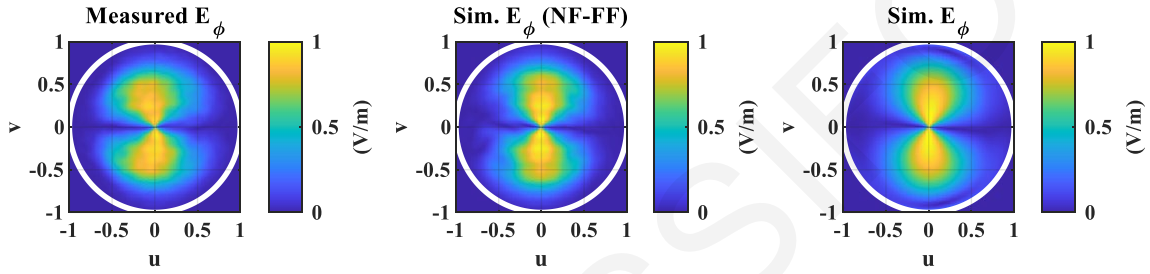


Figure A.11: Measured and simulated electric field for antipodal vivaldi antenna shown in Fig. A.10. Both orthogonal components, E_x and E_y are plotted. The distance was $z_{obs} = 29.3$ cm, the plot frequency is 3.6 GHz, and the sampling steps Δ_x and Δ_y are set to $\lambda/4$ at the higher measured frequency, 4.5 GHz.



(a)



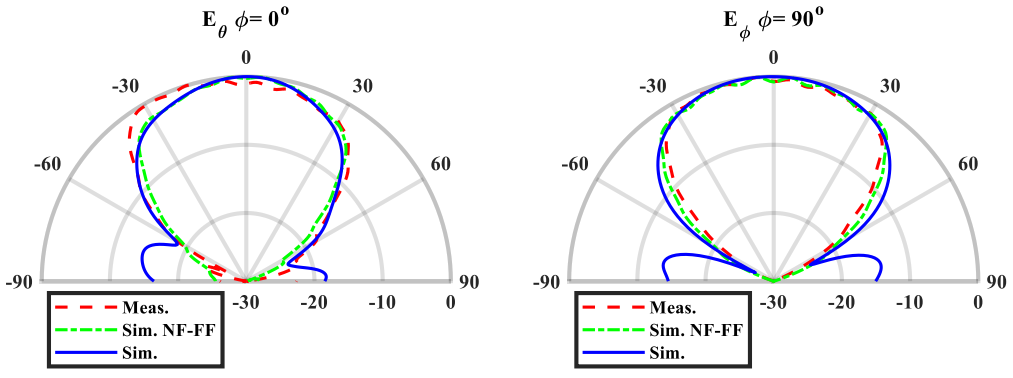
(b)

Figure A.12: Electric field plots of the verification antenna. For comparison, measured, simulated NF data that have been transformed to the FF and simulated FF data are compared. (a) E_θ, and (b) E_ϕ.

a $\phi = 90°$. Other than the deviation of the beam at $\theta = -30°$, the measured data are in very good agreement.

A.5 Discussion and Conclusion

The design and a basic verification of the custom NF system was presented in this appendix. The system was intended to measure the PMSF prototype presented in this thesis. Even though that the system wasn't intended for accurate antenna measurements, the system exceeded its expectation. The system was shown to be able to deliver acceptable FF patterns. Furthermore, the cost of the system, is just a fraction compared to the commercially available NF systems. The author hope this appendix helps future researchers developed their own measurement system.



(a) (b)

Figure A.13: Normalised electric field plots of the Vivaldi antenna. Measured, simulated NF data that have been transformed to the FF and simulated FF data are compared. (a) E_θ, and (b) E_ϕ.